PowerLogic™ P7

Protection and control device

User Manual

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Hardware version: B



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About this manual

Safety information

Important information

Read these instructions carefully and look at the equipment to become familiar with the device before trying to install, operate, service or maintain it. The following special messages may appear throughout this manual or on the equipment to warn of potential hazards or to call attention to information that clarifies or simplifies a procedure.



The addition of either symbol to a “Danger” or “Warning” safety label indicates that an electrical hazard exists which will result in personal injury if the instructions are not followed.



This is the safety alert symbol. It is used to alert you to potential personal injury hazards. Obey all safety messages that follow this symbol to avoid possible injury or death.

⚠DANGER

DANGER indicates a hazardous situation which, if not avoided, **will result in** death or serious injury

⚠WARNING

WARNING indicates a hazardous situation which, if not avoided, **can result in** death or serious injury.

⚠CAUTION

CAUTION indicates a hazardous situation which, if not avoided, **can result in** minor or moderate injury.

NOTICE

NOTICE is used to address practices not related to physical injury.

User qualification

Electrical equipment should be installed, operated, serviced, and maintained only by qualified personnel. No responsibility is assumed by Schneider Electric for any consequences arising out of the use of this material.

A qualified person is one who has skills and knowledge related to the construction, installation, and operation of electrical equipment and has received safety training to recognize and avoid the hazards involved.

Use the password protection feature in order to help prevent untrained and non-authorized personnel interacting with the PowerLogic P7.

Disclaimer

No responsibility is assumed by Schneider Electric for any consequences arising out of the use of this document. This document is not intended as an instruction manual for untrained persons. This document gives instructions on device installation, commissioning and operation. However, the manual cannot cover all conceivable circumstances or include detailed information on all topics. In the event of questions or specific issues, contact Schneider Electric and request the necessary information.

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Purpose

PowerLogic™ P7 protection and control device (PowerLogic P7) user manual is for people who are experts on electrical power engineering, panel builders, commissioning engineers, and experienced users, communication specialists or general users.

The complete manual is arranged as follows:

- Preliminary sections, with the details of the manual (how to use it, glossary) and technical data.
- Functions of the PowerLogic P7.
  Explanations, diagrams and settings of the protection, control, monitoring and maintenance, measurement, recording and programmable logic functions are introduced in these sections.
- Installation and commissioning.
- Local control panel use, troubleshooting and maintenance instructions.

Following documents complete this manual:

- Instruction sheet, delivered in the device package, summarizes instructions for installation.
- PowerLogic P7 Communication User Manual, for the understanding and the setup of the communication protocols with the PowerLogic P7.
- PowerLogic Engineering Suite User Manual, gives instructions on how to set up project and use the tool to create configurations for Intelligent Electronic Device (IED).

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http://www.se.com/CCC

PowerLogic P7 overview

The PowerLogic P7 range is a platform of digital protection and control devices for modern Power Systems that provides hardware and firmware flexibility. This allows selection of hardware modules and firmware application levels to meet specific requirements. The product selection includes choice of required hardware modules and accessories like analog boards, input/output modules, Ethernet ports and so on. Application packages and corresponding application levels can be selected from a comprehensive list.

PowerLogic P7 devices are expandable and support additional hardware and functional requirements during installation or future system expansion. A license upgrade is required depending upon what functionality is required to be added.

The PowerLogic P7 platform provides wide range of functionality supported by the engineering tool, PowerLogic Engineering Suite. This is a versatile tool that guides the user through the lifecycle of the product from design up to operation.

PowerLogic P7 devices can be applied in a wide range of electrical domains.

Utilities	Industry	Buildings
Generation Distribution Transmission	Oil and Gas Mining, Mineral and Metals Electro-intensive	Data Centers

Properties of the PowerLogic P7

The PowerLogic P7 platform is built on technology concepts developed in close cooperation with customers to help ensure the safety of the Power Systems. PowerLogic P7 devices can be tailored to suit customer applications over the entire life cycle of the product. The ease of use, hardware modularity and firmware flexibility of the range means that the PowerLogic P7 can be upgraded or modified to suit the latest needs of the application at any time.

Features

- Scalable hardware and firmware platform.
- Firmware flexibility and hardware modularity with extensive protection functionality and HMI with 7” graphical color touchscreen.
- Digital substation ready with IEC 61850 Edition 2.1.
- EcoStruxure™ connected product for asset management and condition monitoring.
- IEC 62443-4-2 Security Level 2 compliant cybersecurity.

Hardware modularity

Modular and expandable structure of the PowerLogic P7 supports various configuration items to suit the application through the lifecycle of the product.

- 40TE case with nine slots including three fixed and six user selectable slots. It provides increased reliability and high operational safety with a design meeting extreme environmental condition.
- Fixed slots are fitted with the processor/communication modules, power supply module, and a power supply auxiliary module respectively.
- Platform flexibility, each user selectable slot is able to support all types of input module.

- Precision Time Protocol (PTP) time synchronization is available as standard but additional Inter-Range Instrumentation Group-B (IRIG-B) and temperature measurement (RTD) modules are supported as accessories that are interfaced with the PowerLogic P7 through an extension port.
- Standardized analog, binary I/O modules, communication modules and accessories for the entire range facilitates easy replacement and minimizes spares stock.
- Various Ethernet Small Form-factor Pluggable (SFP) modules, available as accessories, enhance the flexibility for demanding Ethernet architectures.

Firmware flexibility

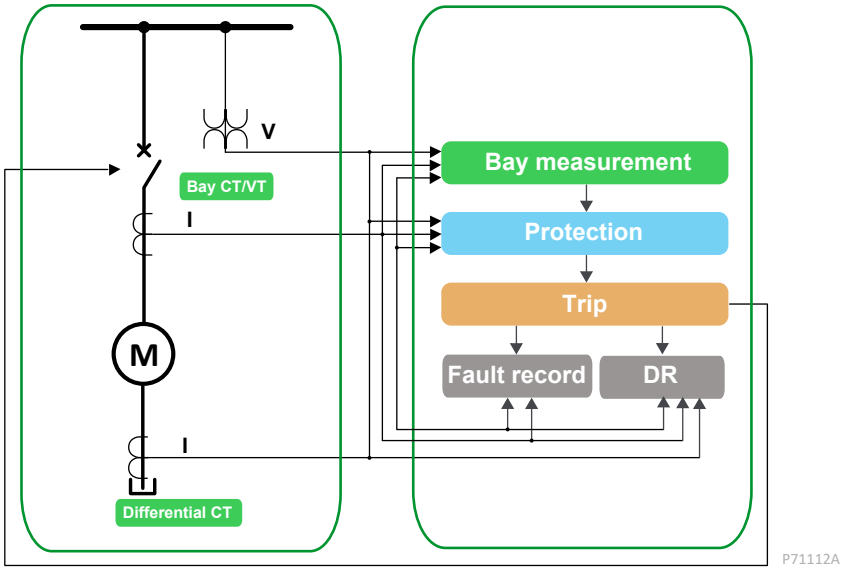
PowerLogic P7 devices are capable of adapting to customized device functionality. An approach towards flexibility through different licensing levels allows the user to select an application level and benefit from the functionality offered by the corresponding level.

Within the chosen application level, the user can freely configure the available functions and features in the corresponding application templates.

- The main application selected defines the pre-installed protection functions.
  - M – Motor protection
  - G – Generator protection
  - F – Feeder protection
  - T – Transformer protection
  - S – Stand Alone Merging Unit
- The application level defines the available functions in a bay depending on the main application.
  - Basic Level applications (Level 0)
  - Standard Level applications (Level 1)
- Bay is used to group equipment, functions, measurements, and records used by the application. Equipment and functions can be added with minimal user configuration and include default signal routing for operation. Signal routing includes routing of analog signals like single and three phase currents and voltages to the corresponding analog modules, binary signals like Trip, trigger for Disturbance recorder.
  - Current Transformer (CT) and Voltage Transformer (VT) sources are part of a bay which are routed to physical CT inputs in accordance with the selected user analog modules. A single CT and VT source are defined as the bay measurements used for load monitoring. This CT source is also used as the reference for 3ph VT supervision.
  - One Circuit Breaker (CB) and multiple switches are added to a bay. Associated functions such as interlocking and breaker failure are automatically associated.
  - Protection and control functions are available depending on the main application and license level. Most functions will operate based on the bay measurements while functions such as differential will require additional sources.

    Some simple functions such as current and voltage protection allow the source CT or VT to be changed from the default bay measurement to a different source as required by the application.
  - Bay measurements depend on the main application and installed functions. For example, adding motor thermal protection function will add thermal to the bay measurements.
  - Records (Fault and Disturbance) are automatically created for the bay. These records include any additional equipment or function signals that are added to the bay.

Figure 1 - Example of bay representation for motor protection



Protection	Includes protection functions based on bay measurements and functions based on other CTs and VTs connected to the bay.
Bay measurement	Includes load measurements (Hz, W, Wh) from the bay CT and VT.

Color graphical user interface

- 7” graphical color touchscreen display with mimic.
- **Home** and **Reset** physical buttons and 4 fixed Light Emitting Diode (LED)s to indicate the status of power supply, trip, alarm and out of service.
- 24 user configurable virtual LEDs, 12 function keys on the touchscreen.
- Customizable user displays for efficient viewing of data through graph or meters, standard control, annunciations.
- Universal Serial Bus (USB) (Type B, Mini) interface access for the PowerLogic Engineering Suite.

Substation communication

- The processor module includes an integrated single Ethernet RJ45 port that can be used for engineering access and/or Supervisory Control And Data Acquisition (SCADA).
- Additional redundant interface through SFP ports (RJ45, Fiber Optic (FO) Multimode, FO Singlemode) for Ethernet architectures supporting redundancy protocols such as High availability Seamless Redundancy (HSR), Parallel Redundancy Protocol (PRP), Rapid Spanning Tree Protocol (RSTP) and Failover. A single SFP can also be used as an additional non redundant interface.
- Time synchronization through Ethernet using Simple Network Time Protocol (SNTP) or IEEE 1588 PTP is supported. IRIG-B time synchronization is supported via an external module using the extension port.
- IEC 61850 Edition 2.1, Distributed Network Protocol 3 (DNP3) and Modbus server (slave) communication protocols through any of the Ethernet ports.
- DNP3, Modbus server protocols through an RS485 serial port.
- Additional Internet Protocol (IP)s and Virtual Local Area Network (VLAN)s can be added for Local Area Network (LAN) segregation.

- VLAN and out of band management (port hardening for different protocols) parameters on single Ethernet RJ45 port and redundant SFP ports are configurable.

Selection guide

Table 1 - PowerLogic P7 selection guide

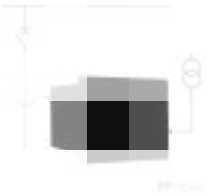
		
Characteristics		
Analog inputs	Standard current	1/5 A CT (4 per 5 CT analog module, 6 per 6 CT analog module. Maximum 2 analog modules.)
	Core balance current	1 A (1 per 5 CT analog module. Maximum 2 analog modules.)
	Voltage	57.7...300 V (4 per 5 CT analog module, 3 per 6 CT analog module. Maximum 2 analog modules.)
Binary I/O	Inputs	Min: 8 (1TIO) Max: 40 (4 Mixed binary Input/Output (MIO))
	Outputs	Min: 8 + watchdog; (1TIO + 1PSU) Max: 32 + watchdog; (1TIO + 1PSU + 4MIO)
Temperature sensor inputs		Max: 8 (8 RTDs per MET148-2 module.)
Front ports	Mini-USB port	■ For accessing the PowerLogic Engineering Suite
	USB-A port	For future use (not currently functional)
Communication		
Rear ports	Extension port	■ For connection of MET148-2 module, IRIG-B module, and CLIO module.
	RS485 serial port	■
	Ethernet port RJ45	■
	Redundant Ethernet port (1 or 2 SFPs)	■
Protocols	IEC 61850 Ed.2.1	■
	DNP3 serial and Ethernet	■
	Modbus server serial and Ethernet	■
Redundancy protocols	HSR	■
	PRP	■
	RSTP	■
	Failover	■
Other		
Time synchronization source	SNTP	■
	IRIG-B	■ External IRIG-B adapter required
	IEEE 1588 PTP	■

Table 1 - PowerLogic P7 selection guide (Continued)

Control		Level 0: 1 CB and 5 switches Level 1: 1 CB and 9 switches
Logic	Matrix	■
	Logic equations	■
Cybersecurity		RBAC according to IEC 62351 standard

NOTE: ■ represents that the device is equipped with this feature.

Function table

The function table describes the full functions and stages instantiated for **Level 0** (basic function) and **Level 1** (standard function) for different applications. The two levels specify the fixed functions and stages in applications.

In this table,

- ***** represents that the function will be available from the higher application level.
- **-** represents that the function is not available for the application type.

  NOTE: In later releases, the flexibility of the functions and stages can be supported in different applications.

The functional routing of each stage of the protections can be accessed and configured from the PowerLogic Engineering Suite. Functional routing refers to the option to modify the connection between the functions of the PowerLogic P7 device, for example, to select which current transformer is used for the overcurrent protection stage.

NOTE: To avoid an invalid configuration, not all connections can be modified. When the default functional routing of the PowerLogic P7 application is modified, verify that the behavior is logical via testing of the application.

Table 2 - PowerLogic P7 function selection table for applications

	IEC 61850 Logical node	ANSI code	Motor		Generator		Feeder		Trans-former		SAMU		Func-tional routing
			L0	L1	L0	L1	L0	L1	L0	L1	L0	L1	
Current protection functions													
Phase overcurrent	*PH**PTOC***	50/51	2	2	2	4	4	8	2	6	2	6	True
Directional phase overcurrent	*PH**RDIR***	67	*	1	*	1	1	2	*	3	*	2	True
Ground fault overcurrent	*EF**PTOC***	50N/ 51N	2	2	2	4	4	8	2	6	-	-	True
Directional ground fault overcurrent	*EF**RDIR***	67N	*	1	*	1	1	2	*	3	-	-	True
Sensitive ground fault overcurrent	*VSEF**PTOC***	50SG/ 51SG	2	2	2	2	4	8	2	3	-	-	True
Negative sequence overcurrent	*NPS**PTOC***	46	2	2	2	2	4	8	2	3	-	-	True
Inrush detection	*ID**PHAR***	68ID	2	2	*	2	2	2	2	3	-	-	True
Selective overcurrent logic (SOL)	*SOL**GAPC***	N/A	1	1	1	1	1	1	1	1	-	-	False
Phase undercurrent	*PH**PTUC***	37	2	2	-	-	-	-	-	-	-	-	True
Voltage dependent overcurrent	*PH**PVOC***	51V	-	-	1	2	1	2	*	2	-	-	True
Sensitive directional earthfault	***PSDE***	32N	*	2	*	2	1	2	1	3	-	-	True
Switch-onto-fault V2.2.1	***PSOF***	50HS	-	-	-	-	*	2	-	-	-	-	True
Ground admittance	*EF**PADM***	21N	-	-	*	2	*	2	*	2	-	-	True

Table 2 - PowerLogic P7 function selection table for applications (Continued)

	IEC 61850 Logical node	ANSI code	Motor		Generator		Feeder		Trans-former		SAMU		Func-tional routing
			L0	L1	L0	L1	L0	L1	L0	L1	L0	L1	
Voltage protection functions													
Undervoltage	*PH**PTUV***	27	2	2	2	2	4	4	2	2	*	2	True
Overvoltage	*PH**PTOV***	59	2	2	2	2	4	4	2	2	*	2	True
Positive phase sequence undervoltage	*PPS**PTUV***	27P	1	1	*	2	2	2	-	-	-	-	True
Positive phase sequence overvoltage	*PPS**PTOV***	59	*	2	*	2	2	2	-	-	-	-	True
Neutral overvoltage	*EF**PTOV***	59N	1	3	1	2	4	4	2	2	-	-	True
Negative phase sequence overvoltage	*NPS**PTOV***	47	1	1	1	1	2	2	-	-	-	-	True
Inter-turn overvoltage	*IT**PTOV***	59IT	-	-	*	1	-	-	-	-	-	-	True
Overfluxing	***PVPH***	24	-	-	*	1	-	-	1	2	-	-	True
Frequency protection functions													
Overfrequency	***PTOF***	81O	*	2	2	2	2	2	2	2	-	-	False
Underfrequency	***PTUF***	81U	*	4	4	4	4	4	4	4	-	-	False
Underfrequency load shedding V2.2.1	*LS**PTUF***	81LS	-	-	-	-	*	1	-	-	-	-	False
Rate of change of frequency	***PFRC***	81R	*	4	*	4	4	10	4	10	-	-	False
Differential protection functions													
High impedance differential	*HIZ**PDIF***	87/ 64REF	*	1	*	1	*	1	*	1	-	-	True
Biased differential	*PH**PDIF***	87	*	1	*	1	-	-	-	-	-	-	True
Low impedance differential	*RGF**PDIF***	64REF	*	1	*	1	*	1	2	3	-	-	True
Basic transformer differential V2.2.1	*TR2**PDIF***	87T	-	-	-	-	-	-	1	-	-	-	True
Advanced transformer differential V2.2.1	*TR3**PDIF***	87T	-	-	-	-	-	-	-	1	-	-	True
Temperature protection functions													
Motor thermal overload	*THM**PTTR***	49	1	1	1	1	-	-	-	-	-	-	True
Thermal overload	*THF**PTTR***	49F	-	-	-	-	1	1	*	1	-	-	True
Overtemperature	***STMP***	38/49T	8	8	8	8	*	8	*	8	*	8	False
Machine unbalance	*NPS**PTTR***	46	1	1	1	1	-	-	-	-	-	-	True
Motor protection functions													
Motor monitoring	***ZMOT***	N/A	1	1	-	-	-	-	-	-	-	-	True
Motor start-up supervision, locked rotor	***PMSS***	48	1	1	-	-	-	-	-	-	-	-	True
Locked rotor	*JAM**PTOC***	51LR	1	1	-	-	-	-	-	-	-	-	True
Motor restart inhibition	***PMRI***	66	1	1	-	-	-	-	-	-	-	-	False
Voltage check	*VC**PTUV***	47	1	1	-	-	-	-	-	-	-	-	True
Generator protection functions													
Third harmonic undervoltage	*ST**PTUV***	27TN	-	-	*	1	-	-	-	-	-	-	True
Inter-turn protection based on split phase	*IT**PDIF***	87G	-	-	*	1	-	-	-	-	-	-	True
Inadvertent energization	*IE**PIOC***	50/27	-	-	1	1	-	-	-	-	-	-	True
Speed protection functions													

Table 2 - PowerLogic P7 function selection table for applications (Continued)

	IEC 61850 Logical node	ANSI code	Motor		Generator		Feeder		Trans-former		SAMU		Func-tional routing
			L0	L1	L0	L1	L0	L1	L0	L1	L0	L1	
Overspeed	***POVS***	12	*	2	*	2	-	-	-	-	-	-	False
Underspeed[1]	***PZSU***	14	*	2	*	2	-	-	-	-	-	-	False
Speed detection	***TRTN***	N/A	1	1	*	1	-	-	-	-	*	1	False
Distance/impedance protection functions													
Field failure	*FF**PDIS***	40	*	1	*	1	-	-	-	-	-	-	True
Underimpedance	*UZ**PDIS***	21	-	-	*	1	-	-	*	1	-	-	True
Out of step	*OOS**PPAM***	78	*	1	*	1	-	-	-	-	-	-	True
Power protection functions													
Overpower	***PPDOP***	32P	-	-	2	4	2	2	*	2	-	-	False
Reactive overpower	***QPDOP***	32Q	2	2	1	2	2	2	*	2	-	-	False
Underpower	***PPDUP***	37P	2	2	1	2	2	2	*	2	-	-	False
Monitoring functions													
Trip conditioner	***PTRC***	86	1	2	1	4	1	4	2	6	1	4	False
CT supervision	*CTS**SCTR***	60	1	2	1	2	1	3	2	3	1	2	False
VT supervision	*VTS**SVTR***	60FL	1	1	1	2	1	2	1	2	1	2	False
Circuit breaker supervision	*CB**SCBR***	N/A	1	1	1	1	1	2	1	3	1	2	True
Switch monitoring	*SW**SSWI***	N/A	5	9	5	9	5	9	5	9	5	9	False
DC battery voltage monitoring	***ZBAT***	N/A	1	1	1	1	1	1	1	1	1	1	False
Bay dead	*PD**GAPC***	N/A	1	1	1	1	1	1	1	1	1	1	True
Temperature	*RTD**TTMP***	N/A	1	1	1	1	*	1	*	1	*	1	False
Voltage variation	***QVVR***	N/A	*	1	*	1	*	1	*	1	-	-	True
Current loop (mA) input V2.2.1	*CL**TGSN***	N/A	*	4	*	4	*	4	*	4	*	4	False
Programmable stage V2.2.1	*PS**GAPC***	N/A	*	4	*	4	*	4	*	4	*	4	False
Control functions													
Circuit breaker proxy	*CB**XCBR***	N/A	1	1	1	1	1	2	1	3	1	2	True
Circuit breaker control	*CB**CSWI***	N/A	1	1	1	1	1	2	1	3	1	2	False
Circuit breaker interlocking	*CB**CILO***	N/A	1	1	1	1	1	2	1	3	1	2	False
Circuit breaker failure	***RBRF***	50BF	1	1	1	1	1	2	1	3	1	2	True
Switch proxy	*SW**XSWI***	N/A	5	9	5	9	5	9	5	9	5	9	False
Switch control	*SW**CSWI***	N/A	5	9	5	9	5	9	5	9	5	9	False
Switch interlocking	*SW**CILO***	N/A	5	9	5	9	5	9	5	9	5	9	False
Synchro-check	***RSYN***	25	-	-	1	1	1	2	*	2	-	-	True
Auto-recloser	*TRI**RREC***	79	-	-	-	-	1	2	-	-	-	-	False
Logs and records													
Sequence of event record	*GEN**GLOG***	N/A	1	1	1	1	1	1	1	1	1	1	False
Disturbance record	*DR**RDRE***	N/A	1	1	1	1	1	1	1	1	1	1	False
Fault record	*TCR**GLOG***	N/A	1	1	1	1	1	1	1	1	1	1	False
Operation log	*GEN**GLOG***	N/A	1	1	1	1	1	1	1	1	1	1	False

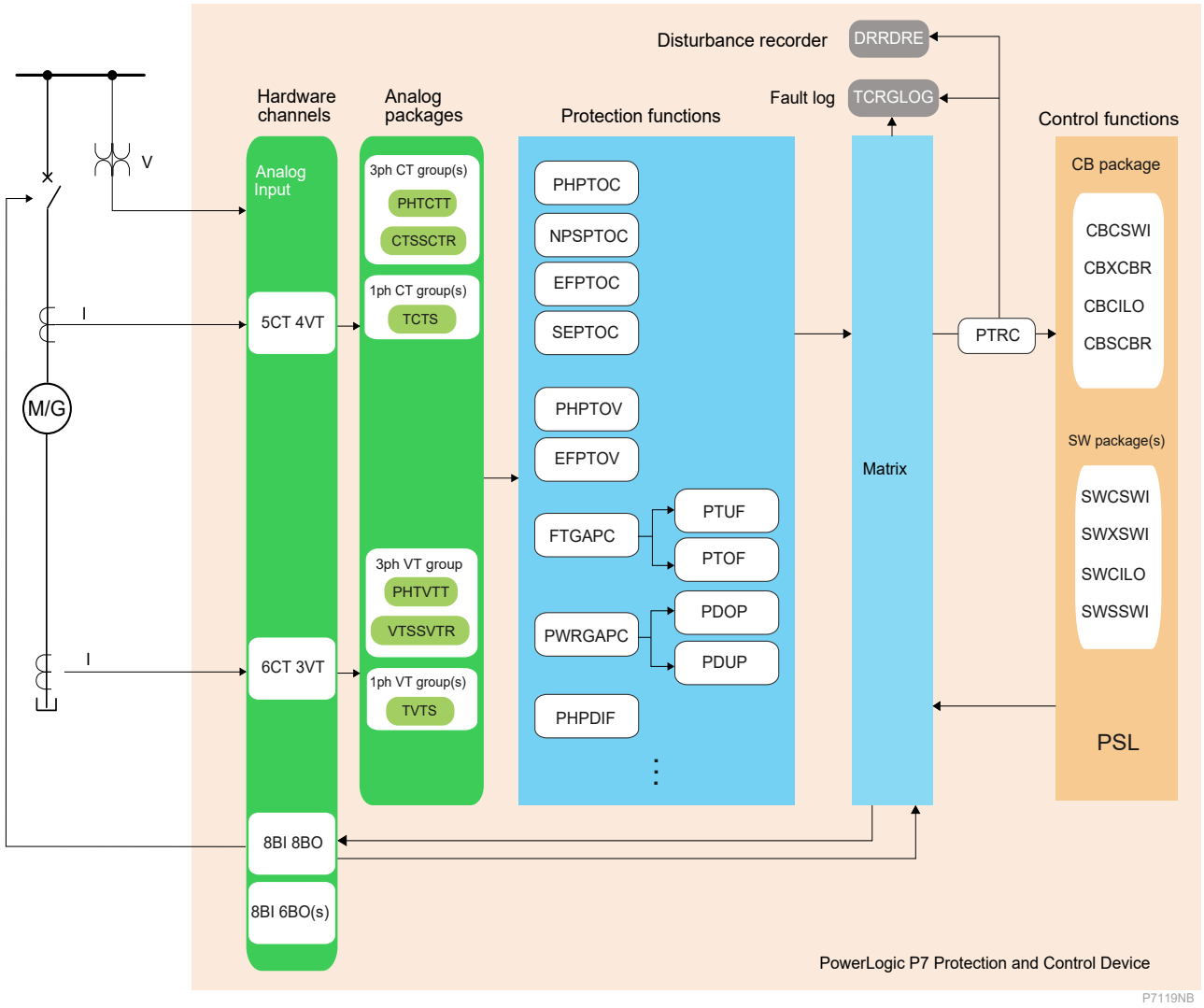
1. One *PZSU* stage is dedicated to Zerospeed *ZEROPZSU*.

Table 2 - PowerLogic P7 function selection table for applications (Continued)

	IEC 61850 Logical node	ANSI code	Motor		Generator		Feeder		Trans-former		SAMU		Func-tional routing
			L0	L1	L0	L1	L0	L1	L0	L1	L0	L1	
Power quality record	*PQ**GLOG***	N/A	*	1	*	1	*	1	*	1	-	-	False
Fault locator V2.2.1	*RFLO*	21FL	-	-	-	-	*	1	-	-	-	-	False
Overhead Line V2.2.1	*ZLIN*	N/A	-	-	-	-	*	1	-	-	-	-	False
CT group measurement													
3ph current	*VECA**MMXU***	N/A	1	2	1	2	1	3	2	3	1	2	False
3ph RMS current	*RMSA**MMXU***	N/A	1	2	1	2	1	3	2	3	1	2	False
Sequence current	***AMSQI***	N/A	1	2	1	2	1	3	2	3	1	2	False
1ph current	*VECAX**MMXU***	N/A	1	2	1	2	1	3	2	3	1	2	False
1ph RMS current	*RMSAX**MMXU***	N/A	1	2	1	2	1	3	2	3	1	2	False
VT group measurement													
3ph voltage	*VECV**MMXU***	N/A	1	1	1	2	1	2	1	2	1	2	False
3ph RMS voltage	*RMSV**MMXU***	N/A	1	1	1	2	1	2	1	2	1	2	False
Sequence voltage	***VMSQI***	N/A	1	1	1	2	1	2	1	2	1	2	False
1ph voltage	*VECVX**MMXU***	N/A	*	2	1	2	1	2	1	2	*	2	False
1ph RMS voltage	*RMSVX**MMXU***	N/A	*	2	1	2	1	2	1	2	*	2	False
Bay measurement													
Fundamental frequency active, reactive and apparent power values, power factor	*BAY**MMXU***	N/A	1	1	1	1	1	1	1	1	1	1	False
RMS active, reactive and apparent power	*BAY**MMXU***	N/A	1	1	1	1	1	1	1	1	1	1	False
Minimum and maximum demand values: RMS phase currents	*DVAL**MMXU***	N/A	1	1	1	1	1	1	1	1	1	1	False
Minimum and maximum demand values: active, reactive, apparent power and power factor	*DVAL**MMXU***	N/A	1	1	1	1	1	1	1	1	1	1	False
Active and reactive of energy values	***EMMTR***	N/A	1	1	1	1	1	1	1	1	1	1	False
Bay Fourier current	*BAY**MMXU***	N/A	1	1	1	1	1	1	1	1	1	1	False
Bay RMS current	*BAY**MMXU***	N/A	1	1	1	1	1	1	1	1	1	1	False
Bay sequence current	*BAY**MMXU***	N/A	1	1	1	1	1	1	1	1	1	1	False
Bay Fourier voltage	*BAY**MMXU***	N/A	1	1	1	1	1	1	1	1	1	1	False
Bay RMS voltage	*BAY**MMXU***	N/A	1	1	1	1	1	1	1	1	1	1	False
Bay sequence voltage	*BAY**MMXU***	N/A	1	1	1	1	1	1	1	1	1	1	False
Harmonics	***MHAI***	N/A	*	1	*	1	*	1	*	1	-	-	False
Process bus functions													
SV publication V2.2.1	***LSVP***	N/A	*	1	*	1	*	1	*	1	1	3	False
SV subscription V2.2.1	***LSVS***	N/A	*	2	*	2	*	2	*	2	-	-	False

Application overview

Figure 2 - Functional diagram of the PowerLogic P7



Technical characteristics

Table 3 - PowerLogic P7 technical characteristics

Characteristic	Value
Power system frequency	
Rated frequency	50 Hz or 60 Hz
Operation frequency	
Operation frequency range	10...70 Hz
Frequency range (at claimed accuracy)	40...70 Hz
Power supply	
Operating range	Low range: DC: 24...34 V DC, ±20% Medium range: DC: 48...125 V DC, ±20% High range: DC: 110...250 V DC, -20%...+20% AC: 110...250 V AC, -27%...+15%
AC frequency operating range	50 Hz, ±10%; 60 Hz, ±10%

Table 3 - PowerLogic P7 technical characteristics (Continued)

Characteristic	Value
MCB recommendation	DC: 6 A; AC: 10 A
Burden DC	Typical: 24 W, maximum: 45 W
Burden AC	Typical: 60 VA, maximum: 112 VA at 230 V AC Typical: 48 VA, maximum: 75 VA at 100 V AC
RTC retention time	
RTC retention time	1 month typical, 1 week guaranteed[2]
Standard CT inputs	
CT secondary phase current	1 A or 5 A
Dynamic range	64 x CT rated current (or 32 x CT rated current + 32 x CT rated current DC offset)
Thermal withstand	Continuous: 20 A 1 s: 500 A Half period: 1250 A
Input impedance	< 0.01 Ω
Burden	< 0.03 VA at 1 A; < 0.5 VA at 5 A
Core balance CT	
CT rated secondary current	1 A
Dynamic range	20 A
Thermal withstand	Continuous: 4 A 1 s: 100 A Half period: 250 A
Input impedance	< 0.05 Ω
Burden	< 0.05 VA
VT inputs	
VT rated secondary voltage	50...480 V RMS (phase-to-phase). Phase-to-neutral connection must be used below 300 V.
Voltage withstand	Continuous: 600 Vrms 1 min: 2200 Vrms
Input impedance	2200 kΩ to ground per pin 4400 kΩ between 2 pins, resistive
Rated frequency	Rated: 50 Hz or 60 Hz DC tolerant: 10...1000 Hz
Burden	< 0.05 VA
Binary inputs	
Operating nominal voltage	24...250 V DC 220...250 V AC
Voltage withstand	300 V DC, 300 Vrms
Pulsed current	30 mA for 20 ms (DC)
Constant current	1 mA
Pick-up threshold	40% to 80% in 1% steps of nominal voltage
Drop-off threshold	50% to 90% in 1% steps of pick-up voltage
Threshold accuracy	< 1%
Filter time	20 µs...100 ms in 20 µs steps fixed value for speed detection function: 60 µs
Recognition time	< 1 ms (DC) < 20 ms (AC), excluding filter time
Reset time	< 1 ms (DC) < 20 ms (AC)

2. This value can be affected by high temperatures.

Table 3 - PowerLogic P7 technical characteristics (Continued)

Characteristic	Value
Burden current	AC: < 15 mA DC: < 2 mA
Voltage withstand	2 kV AC for 1 min to ground and other circuits including other binary input pairs on the same board
Standard binary output	
Contact rated voltage	250 V DC or 250 V AC, 50 Hz or 60 Hz
Voltage withstand	300 V DC, 300 V rms
Continuous current	Max: 8 A (UL: 5 A)
Short duration withstand carry	30 A, 3 s 250 A, 30 ms
Make and break capacity	DC: 50 W resistive DC: 62.5 W inductive (L/R = 50 ms) AC: 2500 VA resistive (cosΦ = unity) AC: 2500 VA inductive (cosΦ = 0.7)
Make and carry	30 A for 3s, DC resistive 10,000 operations (subject to the above limits of make/break capacity and rated voltage)
Make carry and break	30 A for 200 ms, AC resistive 2,000 operations (subject to the above limits of make/break capacity & rated voltage) 4 A for 1.5 s, DC resistive 10,000 operations (subject to the above limits of make/break capacity & rated voltage) 0.5 A for 1 s, DC inductive 10,000 operations (subject to the above limits of make/break capacity & rated voltage) 10 A for 1.5 s, AC resistive/inductive 10,000 operations (subject to the above limits of make/break capacity & rated voltage)
Operate time	< 5 ms, bounce time not included
Reset time	< 5 ms, bounce time not included
Contact material	Ag alloy
Loaded contact	10,000 operations minimum
Unloaded contact	100,000 operations minimum
High break (HSHB) binary output	
Contact rated voltage	250 V DC
Continuous current	Max: 10 A
Short duration withstand carry	30 A, 3 s 250 A, 30 ms
Mark and Break capacity	DC: 7500 W resistive DC: 2500 W inductive (L/R = 40 ms)
Make carry and break	30 A for 200 ms, DC resistive 10,000 operations (subject to the above limits of make/break capacity & rated voltage) 10 A for 1s, DC inductive 10,000 operations (subject to the above limits of make/break capacity & rated voltage)
Loaded contact	10,000 operations minimum
Unloaded contact	100,000 operations minimum
Operating time	< 0.2 ms
Reset time	< 8 ms
Watchdog binary output	
Contact rated voltage	240 V DC or 240 V AC, 50 Hz or 60 Hz
Voltage withstand	300 V DC, 300 Vrms
Continuous current	2 A

Table 3 - PowerLogic P7 technical characteristics (Continued)

Characteristic	Value
Short duration withstand carry	30 A, 0.2 s
Minimum making current	10 mA with 50 mW minimum
Make and carry	1000 W with L/R = 40 ms 250 V DC 1150 VA 230 V AC Duty cycle 1 s ON, 9 s OFF
Make , Carry & Break	30 W with L/R = 40 ms 250 V DC 1150 VA 230 V AC Duty cycle 1 s ON, 9 s OFF
Contact material	Ag alloy
Loaded contact	10,000 operations minimum
Unloaded contact	100,000 operations minimum
Size and weight	
40TE Case size (Width x Height x Depth)	205 × 180 × 280 mm (8 × 7 × 11 in) 250 mm depth in panel 205 × 180 × 254 mm (8 × 7 × 10 in) for no HMI option
Weight	Maximum weight: 8.8 kg (19.4 lb) (two analog boards and two mixed I/O boards)

Table 4 - CLIO technical characteristics

Characteristic	Value
Power supply	
Operating range	DC: 24...250 V DC, ±20% AC: 100...250 V AC, ±20%
AC frequency operating range	50 Hz, ±10%; 60 Hz, ±10%
MCB recommendation	DC: 6 A; AC: 10 A
Burden DC	Typical: 3 W, maximum: 12 W
Burden AC	Typical: 7.5 VA, maximum: 30 VA at 250 V AC Typical: 6 VA, maximum: 24 VA at 100 V AC
Number of channels	
Number of channels for current loop input	4
Number of channels for current loop output	4
Ranges	
Ranges of current loop input	-20…+20 mA -10…+10 mA -1…+1mA 0…20mA 4…20mA
Ranges of current loop output	0…1 mA 0…10 mA 0…20 mA 4…20 mA
Accuracy	
Accuracy of current loop input	±0.2% desirable ±0.5% of full scale compulsory
Accuracy of current loop output	±0.5% of full scale
Interval	
Sampling interval of current loop input	50 ms
Conversion interval of current loop output	50 ms
Other characteristic	
Latency of current loop output	< 100 ms

Table 4 - CLIO technical characteristics (Continued)

Characteristic	Value
Load resistance of current loop input	< 300 Ω
Maximum output load	600 Ω

Environmental characteristics

⚠WARNING

UNINTENDED EQUIPMENT OPERATION

Install the PowerLogic P7 according to the environmental characteristics.

Failure to follow these instructions can result in death, serious injury, or equipment damage.

All the binary inputs have been tested with 3 ms filter time.

Table 5 - PowerLogic P7 environmental characteristics

Characteristic	Description/Value		
Power Supply			
Characteristics	**Standard**	**Level**	**Value**
Voltage dips (DC)	IEC 61000-4-29 IEC 60255-26		200 ms voltage dips 0%, 250 V DC and above, Criteria A 100 ms voltage dips 0%, 110 V DC 50 ms voltage dips 0%, 48 V DC 50 ms voltage dips 0%, 24 V DC
Ripple (DC)	IEC 61000-4-17 IEC 60255-26		15%; 100 Hz/120 Hz, Criteria A
Voltage dips (AC)	IEC 61000-4-11 IEC 60255-26		Criteria A 10 cycles, voltage dips 0%, 250 V AC 5 cycles, voltage dips 0%, 110 V AC
Power Supply (CLIO module)			
Characteristics	**Standard**	**Level**	**Value**
Voltage dips (DC)	IEC 61000-4-29 IEC 60255-26		1000 ms voltage dips 0%, 250 V DC and above, Criteria A 300 ms voltage dips 0%, 24 V DC
Voltage dips (AC)	IEC 61000-4-11 IEC 60255-26		Criteria A 50 cycles, voltage dips 0%, 250 V AC 25 cycles, voltage dips 0%, 100 V AC
Product Safety			
Characteristics	**Standard**		**Value**
Insulation characteristics	IEC 60255-27		Insulation resistance > 100 MΩ at 500 V DC (except VT port). Using only electronic/brushless insulation tester.
Creepage distances and clearances	IEC 60255-27		Pollution degree 2, Overvoltage category III
Altitude	IEC 60255-27		Up to 2000 m
High voltages withstand (dielectric)	IEC 60255-27		2 kV rms AC, 1 min: • between all case terminals connected together, and the case ground 2 kV rms AC, 1 min: • between all terminals of independent circuits 1 kV rms AC for 1 min: • across normally open control and signaling contacts 1 kV rms AC for 1 min: • between RJ45 ports and the case ground

Table 5 - PowerLogic P7 environmental characteristics (Continued)

Characteristic	Description/Value		
			None for internal connection IRIG-B port. None for high speed, high break control relay output due to solid state devices across normally open contact. No test should be applied across contacts when BO1-BO3 for TCS1-TCS3 of TIO board for transient suppression devices are fitted.
	IEEE C37.90		1.5 kV rms, 1 min: across open tripping contacts
Impulse voltage	IEC 60255-27		1.2 µs, 50 µs, 5 kV, 0.5 J • between all terminals of independent circuits. • between all terminals and case ground. 1.2 µs, 50 µs, 1.5 kV, 0.5 J • between RJ45 ports and the case ground.
Product Safety (CLIO module)			
Characteristics	**Standard**		**Value**
Insulation characteristics	IEC 60255-27		Insulation resistance > 1 MΩ at 500 V DC.
Dielectric withstand	IEC 60255-27 IEEE C37.90		3.25 kV AC, 1 min • between power port and case. • between power port and all other circuits connected together (except earth). 2.2 kV AC, 1 min • between power port and earth port. 1 kV AC, 1 min • between CAN ports and I/O ports connected together, and case. • between each I/O port and all other circuits connected together.
Impulse voltage withstand	IEC 60255-27 IEEE C37.90		1.5 kV peak value, 1.2/50 µs, 0.5 J • between CAN ports and I/O ports, and case. • between each I/O port or each CAN port, and all other circuits. 6 kV peak value, 1.2/50 µs, 0.5 J • between power port and case. • between power port and all I/O ports. 5 kV peak value, 1.2/50 µs, 0.5 J • across power port. • between power port and CAN ports or earth.
Electromagnetic Compatibility			
Characteristics	**Standard**	**Level**	**Value**
Emission test			
Radiated disturbances	CISPR 32 CISPR 11 IEC 60255-26	Class A	
	FCC part 18		This device complies with part 18 of the FCC Rules.
Conducted disturbances	CISPR 32 IEC 60255-26	Class A	
	FCC part 18		This device complies with part 18 of the FCC Rules.
Radiated disturbances immunity tests			
Radiated radio frequency fields	IEC 61000-4-3 IEC 60255-26	Level 3	10 V/m, 80 MHz...6 GHz, 80% AM (1 kHz) 30 V/m, 800 MHz...960 MHz/1.4 GHz...2 GHz, 80% AM (1 kHz)
	ANSI C37.90.2		20 V/m, 80 MHz...1GHz, 80% AM (1 kHz) 35 V/m, 80 MHz...1GHz, 100% pulse
Electrostatic discharges	IEC 61000-4-2 IEC 60255-26	Level 4	15 kV air, 8 kV contact

Table 5 - PowerLogic P7 environmental characteristics (Continued)

Characteristic	Description/Value		
	ANSI C37.90.3		15 kV air, 8 kV contact
Magnetic field at power frequency	IEC 61000-4-8 IEC 60255-26	Level 5	100 A/m continuous; 1000 A/m, 1...3 s[3]
Pulse magnetic fields	IEC 61000-4-9	Level 5	1000 A/m
Oscillatory magnetic fields	IEC 61000-4-10	Level 5	100 A/m, 100 kHz and 1 MHz
Conducted Radio Frequency disturbances			
Conducted Radio Frequency disturbance	IEC 61000-4-6 IEC 60255-26	Level 3	10 V rms common mode, 0.15 MHz...80 MHz, 80% AM (1 kHz)
Fast transient bursts	IEC 61000-4-4 IEC 60255-26	Level 4	4 kV common mode, 5 kHz, 100 kHz
	ANSI C37.90.1		4 kV, 5 kHz, common mode and transversal mode
Slow damped oscillatory waves	IEC 61000-4-18 IEC 60255-26	Level 3	2.5 kV common mode 1 kV differential mode, 100 kHz, 1 MHz
	ANSI C37.90.1		2.5 kV, 1 MHz, common mode and transversal mode
	IEC 61000-4-12	Level 3	2 kV common mode; 1 kV, differential mode, 100 kHz Source impedance: 12 Ω
Fast damped oscillatory waves	IEC 61000-4-18 IEC 60255-26	Level 3	2 kV common mode, 3 MHz, 10 MHz, 30 MHz
Conducted disturbances 0 to 150 kHz	IEC 60255-26	Zone A	150 V rms, differential mode; 300 V rms, common mode
	IEC 61000-4-16	Level 4	$16^{2/3}$ Hz, 50 Hz or 60 Hz: • continuous disturbance, 30 V • short duration disturbance, 300 V 15 Hz...150 kHz: • 15 Hz...150 Hz, 30...3 V • 150 Hz...1,5 kHz, 3 V • 1.5 kHz...15 kHz, 3...30V • 15 kHz...150 kHz, 30 V
Surges[4]	IEC 61000-4-5 IEC 60255-26	Level 4	4 kV, common mode; 2 kV, differential mode
Harmonics and interharmonics (AC)	IEC 61000-4-13	Level 3	Criteria A
Environmental conditions			
Characteristics	**Standard**	**Test Method**	**Value**
Operation			
Exposure to cold	IEC 60068-2-1	Ae	-40°C (-40°F), 96 hours.
Exposure to dry heat	IEC 60068-2-2	Be	70°C (158°F), 96 hours
UL test	UL 508	–	55°C (131°F), device operated continuously with 50% of contacts energized at 5 A
Exposure to damp heat	IEC 60068-2-78	Cab	93% ± 3% RH; 40°C (104 °F), 56 days, without condensation
Temperature variation	IEC 60068-2-14	Nb	-40...70°C (-40...158°F), 1°C/min (1.8°F/min) 5 cycles
Damp heat cyclic test	IEC 60068-2-30	Db Variant 1	55°C/93% ± 3% RH and 25°C/97% -2% +3% RH, with condensation, 6 cycles (12 h + 12 h)
Transport and Storage			
Exposure to cold	IEC 60068-2-1	Ab	-40°C (-40°F), 96 hours

3. A minimum threshold of 0.025 pu (standard CT) or 0.005 pu (core-balance CT) is recommended in applications where a magnetic field of 1000 A/m is possible. Lower settings may be used if required; however, a trip delay of at least 5 s will be required to avoid risk for false tripping during a heavy magnetic field.
4. It is recommended to use operation time of at least 30 ms at the lowest pickup value setting.

Table 5 - PowerLogic P7 environmental characteristics (Continued)

Characteristic	Description/Value		
Exposure to dry heat	IEC 60068-2-2	Bb	85°C (185°F), 96 hours
Exposure to damp heat	IEC 60068-2-78	Cab	93% ± 3% RH; 40°C (104°F), 56 days, without condensation
Corrosive atmosphere			
Salt mist	IEC 60068-2-52	Kb/1	4 spraying periods of 2 hours with a storage of 7 days after each
2 Gas	IEC 60068-2-60	Ke	25°C (77°F), 75% RH, 21 days method 1: 0.5 ppm SO_2; 0.1 ppm H_2S
4 Gas	IEC 60068-2-60	Ke	25°C (77°F), 75% RH, 21 days method 4: 0.11 ppm SO_2; 0.071 ppm H_2S; 0.034 ppm Cl_2, 0.26 ppm NO_2. (according to IEC 60721-3-3 level 3C2 concentration)
Mechanical Robustness			
Characteristics	**Standard**	**Level**	**Value**
Vibration response	IEC 60255-21-1	Class 2	1 Gn, 10...150 Hz
Vibration endurance	IEC 60255-21-1	Class 2	2 Gn, 10...150 Hz
Shock response	IEC 60255-21-2	Class 2	10 Gn, 11 ms
Shock withstand	IEC 60255-21-2	Class 1	15 Gn, 11 ms
Bump	IEC 60255-21-2	Class 1	10 Gn, 16 ms
Seismic test	IEC 60255-21-3	Class 2	2 Gn horizontal; 1 Gn vertical
Enclosure			
Front panel	IEC 62262	IK07	Degree of protection against mechanical impacts
	IEC 60529	IP54	Front panel
	NEMA	Type 12	
Rear panel	IEC 60529	IP20	With IP20 protective cover
Case	IEC 60529	IP30	Except area with rear terminals
CLIO module	IEC 62262	IK06	
Fire resistance			
Fire resistance	IEC 60695-2-11		650°C (1202°F)
Packaging			
Resistance to shocks by free fall (with packaging)	IEC 68068-2-31		1 m (3.28 ft)
Certification/declaration			
CE European Commission's directives	EN 60255-26:2013		Electromagnetic Compatibility Directive (EMCD) 2014/30/EU
	EN 60255-27:2014		Low Voltage Directive (LVD) 2014/35/EU
	EN IEC 63000:2018		Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (ROHS) Directive 2015/863/EU
UK CA United Kingdom regulations	BS EN 60255-26:2013		Electromagnetic Compatibility (EMC) Regulations SI 2016 No. 1091
	BS EN 60255-27:2014		Electrical equipment (safety) regulations SI 2016 No. 1101
	BS EN IEC 63000:2018		Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) regulations SI 2012 No.3032
c UL us UL Standards	UL 508 ANSI/IEEE C37.90 CAN/CSA C22.2 No.14		File E518585, NRGU
Ex II(2) GD [Ex tb Db] [Ex eb Gb]	EN 50495: 2010		Potentially Explosive Atmospheres Directive (ATEX) 2014/34/EU

Installation

Safety instructions

This page contains important safety instructions that must be followed precisely before attempting to install, repair, service or maintain electrical equipment. Carefully read and follow the safety instructions described below. Only qualified personnel, equipped with appropriate personal protection equipment, may work on or operate the equipment. Qualified personnel are individuals who are:

- familiar with the installation, commissioning, and operation of the equipment and of the system to which it is being connected.
- able to safely perform switching operations in accordance with accepted safety engineering practices and are authorized to energize and de-energize equipment and to isolate, ground, and label it.
- trained in the care and use of safety apparatus in accordance with safety engineering practices.
- trained in emergency procedures (first aid).

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

- Turn off all power supplying the protection and control device and the equipment in which it is installed before working on it.
- Verify that all power is off using a properly rated voltage sensing device.
- Replace all devices, doors and covers before turning on power to this equipment.
- Apply appropriate personal protective equipment and follow safe electrical work practices. See local regulation.
- Do not install this product in ATEX class 0, 1 and 2 areas unless certified for this application.

Failure to follow these instructions will result in death or serious injury.

⚠DANGER

FIRE HAZARD

- Apply proper tightening torque to all wire connections.
- Disconnect the power supply before removing or replacing a module.
- Never touch electronic parts.

Failure to follow these instructions will result in death or serious injury.

⚠WARNING

UNINTENDED EQUIPMENT OPERATION

Do not energize the primary circuit before the protection device is properly configured.

Failure to follow these instructions can result in death, serious injury, or equipment damage.

⚠CAUTION
HEAVY OBJECT Lift the device with care. **Failure to follow these instructions can result in injury or equipment damage.**

Protection Class I equipment

Before energizing the equipment, it must be grounded using the protective conductor terminal.

The protective conductor (ground) connection must not be removed as the protection against electric shock provided by the equipment would be lost.

When the protective (ground) conductor terminal (PCT) is also used to terminate cable screens, etc., it is essential that the integrity of the protective (ground) conductor is checked after the addition or removal of such functional ground connections. For M4 stud PCTs, the integrity of the protective (ground) connections should be ensured by using of a locknut or similar.

The recommended minimum protective conductor (ground) wire size is 2.5 mm² or AWG 12 unless otherwise stated in the technical data section of the equipment documentation, or required by local or country wiring regulations.

The protective conductor (ground) connection must be low-inductance and as short as possible.

All connections to the equipment must have a defined potential. Connections that are pre-wired, but not used, should preferably be grounded when binary inputs and output relays are isolated. When binary inputs and output relays are connected to common potential, the pre-wired but unused connections should be connected to the common potential of the grouped connections.

Transport, handling, storage and unpacking

Transport

In its original packing, a PowerLogic P7 can be shipped to any destination by all usual means of transport.

If installed in a cubicle, a PowerLogic P7 can be transported by all usual means of transport in the customary conditions used for cubicles. Storage conditions should be taken into consideration for a long period of transport.

Handling

The PowerLogic P7 requires careful handling.

Handle it in the original packing to protect it from damage.

Check the condition of the device by visual inspection and energizing if it is installed in a cubicle.

Storage

NOTICE

WATER DAMAGE

- Do not expose the products to sustained humidity during storage.
- Electrically energize the products within three months of unpacking.
- Where electrical equipment is being installed, allow sufficient time for acclimatization to the ambient temperature of the environment before powering on.
- Supply power to the protection device every two years for at least one hour.

Failure to follow these instructions can reduce the product life span.

If PowerLogic P7 devices are not to be installed immediately upon receipt, they should be stored in a place free from dust, humidity and moisture in their original packaging. The PowerLogic P7 can be stored in its original packaging, in an appropriate location for several years:

- Temperature from -40°C to 85°C (from -40°F to 185°F)
- Humidity < 90%

Care should be taken on subsequent unpacking so that any dust collected on the carton does not fall inside. In locations of high humidity, the carton and packing may become impregnated with moisture that the de-humidifier crystals will lose their efficiency.

Periodically, on yearly basis checking of the environment and the packaging condition is recommended. It is recommended to power on the PowerLogic P7 for one hour every two years.

After the PowerLogic P7 is unpacked, it is recommended to energize the device immediately in an appropriate environment in terms of temperature, humidity and pollution.

If it is installed in a cubicle, keep the cubicle protection packing as long as possible. It should not be stored in a damp environment for more than a month. It should be energized as quickly as possible. If this is not possible, the cubicle reheating system should be activated.

Unpacking

Equipment receipt

NOTICE

PRODUCT TAMPERING

Our products leave our factory in closed, sealed original packaging. At delivery, if the packaging is opened or the seal is broken, the confidentiality and authenticity of the information contained in the products cannot be ensured.

Failure to follow these instructions can result in compromised confidentiality and authenticity of the information contained in the products.

The PowerLogic P7 is shipped in a cardboard box which helps protect it against the shocks received in transport.

PowerLogic P7 devices that are supplied unmounted and not intended for immediate installation should be returned to original boxes.

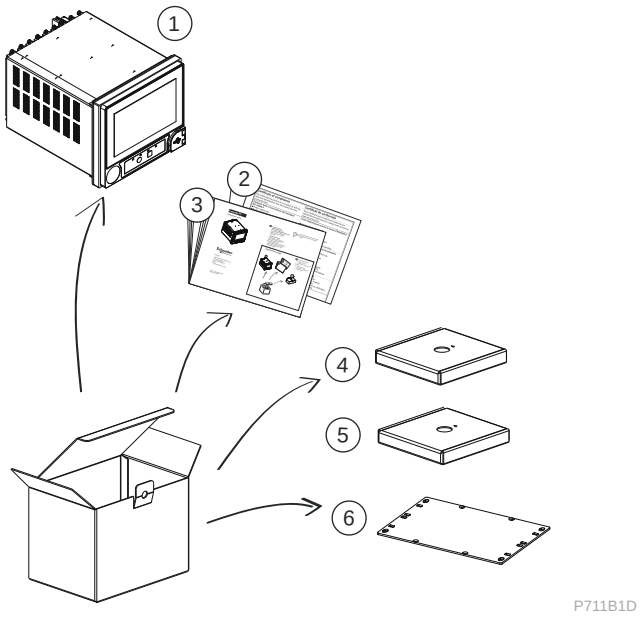
Package contents

Each PowerLogic P7 is delivered in an independent package containing:

- A PowerLogic P7 (max. weight: 8.8 kg) ①

  NOTE: The availability of HMI depends on the order option.
- A certificate of conformity ②
- An instruction sheet ③ providing main information about installation and use
- A top accessory box ④ including the following:
  - 4-teminal serial plug
  - CT/VT screws
  - CT/VT jumpers
  - Mounting screws
  - Optional Ethernet (SFP) module(s)
  - Optional PSU ring terminal and IP20 cover
- A bottom IP20 accessory box ⑤ including the following:
  - IP20 cover for CT/VT
  - Barrier
- A wall mounting adapter plate ⑥

Figure 3 - PowerLogic P7 package contents

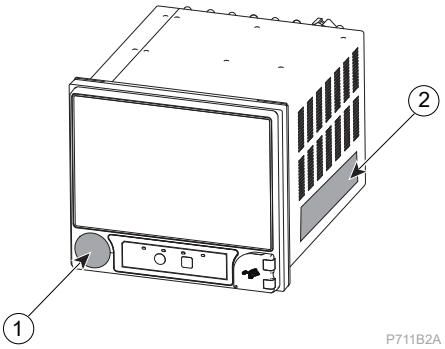


Accessories, such as the IRIG-B module, RTD module can be delivered in a separate package.

Equipment identification

Different kinds of labels are used on the PowerLogic P7 to identify the model type and the safety instructions.

Figure 4 - Label examples on the PowerLogic P7



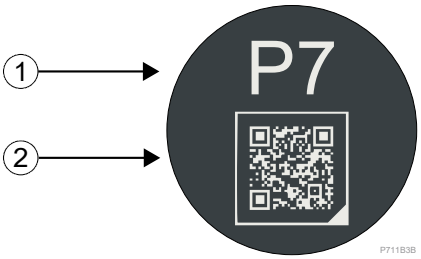
1 Reference label

2 Product label

Reference label

Scan the QR code with the application *mySchneider* or other scanners to access the specific product website.

Figure 5 - Reference label on the PowerLogic P7



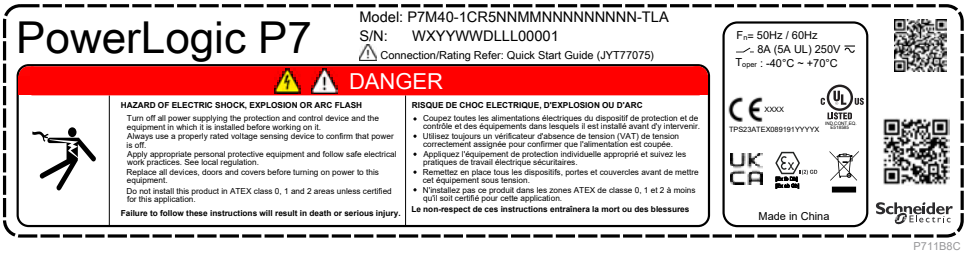
1 Reference

2 Access to product website

Product label

The product label contains the serial number, the model number and the safety instructions for operations on the PowerLogic P7.

Figure 6 - Example of a product label



Operating environment

Operating temperature and humidity

NOTICE
POTENTIAL DAMAGE FROM ENVIRONMENTAL CONDITIONS The device must be installed in an environment within the specified operation temperature and humidity. **Failure to follow these instructions can result in equipment damage.**

The PowerLogic P7 is intended for indoor installation and use only. If it is required for use in an outdoor environment, it must be mounted in a specific cabinet. The USB door must be closed in both cases, which qualifies the device to meet the requirements of IEC 60529 with the classification of protection degree IP54 (dust and splashing water protected).

The temperature/relative humidity factors must be compatible with the environmental withstand characteristics of the PowerLogic P7:

- Recommended operating range of temperature: -10...55°C (14...131°F).
- Maximum operating temperature: -40...70°C (-40...158°F).
- Average humidity: < 75% RH over the year.
- Temporary permissible humidity: < 93% RH (less than 80 hours per year)
- No condensation.

If the operating conditions are outside the normal range, special arrangements should be made before commissioning, such as air conditioning of the premises.

Operation in a polluted atmosphere

A contaminated industrial atmosphere (such as the presence of chlorine, hydrofluoric acid, sulphur, solvents, etc.) can cause corrosion of the electronic components and terminals, in which case environmental control arrangements should be made (such as pressurized premises with filtered air, etc.) before commissioning.

To improve robustness of PowerLogic P7 devices against such environment, all the electronic boards including CPU have a conformal coating.

Mounting

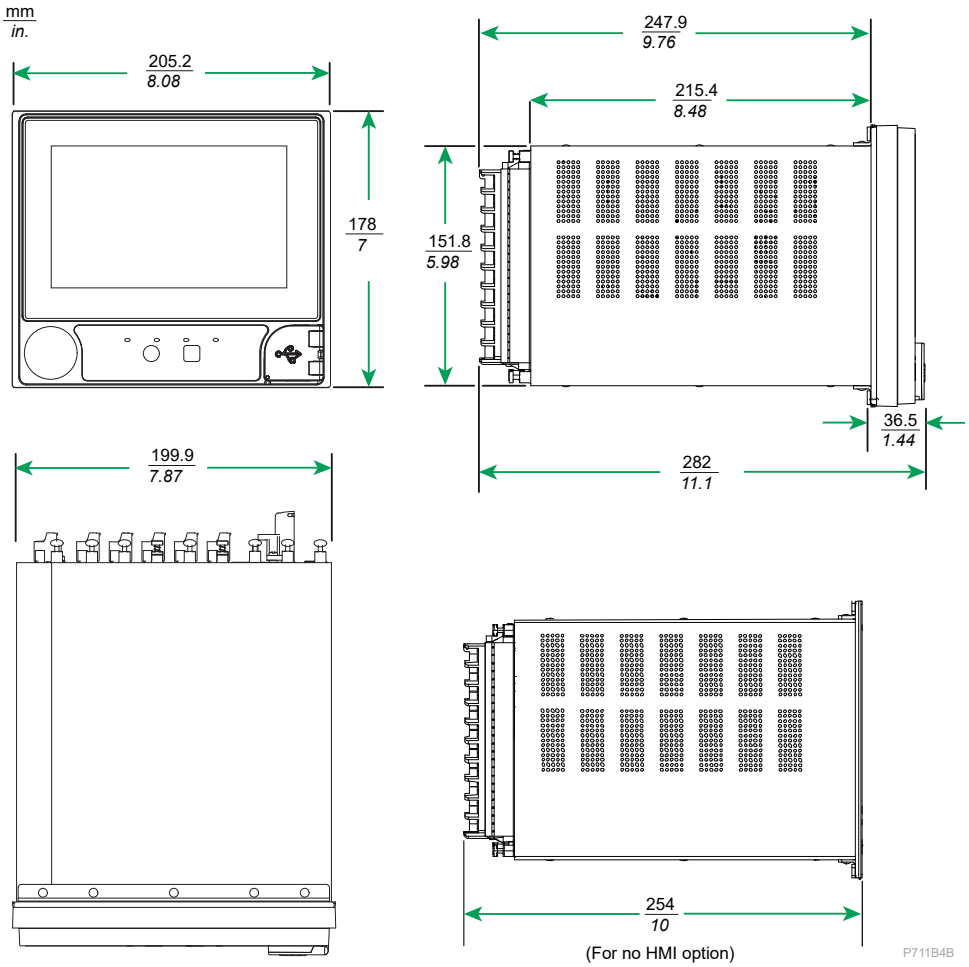
Dimensions

Product dimensions

Dimensions of the PowerLogic P7 are shown below:

NOTE: The PowerLogic P7 (no HMI option) has the same dimensions as the PowerLogic P7 except the depth, which is separately illustrated in the following image.

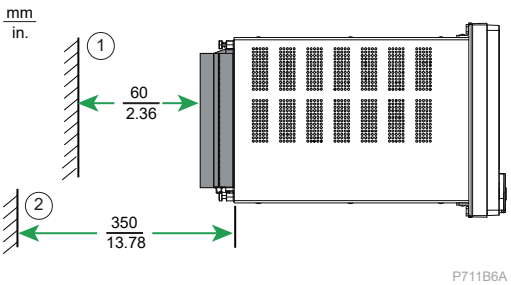
Figure 7 - PowerLogic P7 dimensions



Rear clearances

For easy access to the rear panel, the rear clearances illustrated below are recommended:

Figure 8 - Rear clearances illustrated



① This clearance must be available permanently for the PowerLogic P7 wiring and installation.

② This clearance should be transiently available during maintenance operations when the CPU and modules are replaced.

Flush mounting

⚠CAUTION

CUTS AND PHYSICAL IMPACT

- Wear gloves and safety shoes.
- Trim the edge of the panel cut-out to remove any jagged edges.

Failure to follow these instructions can result in injury or equipment damage.

NOTICE

EQUIPMENT DAMAGE

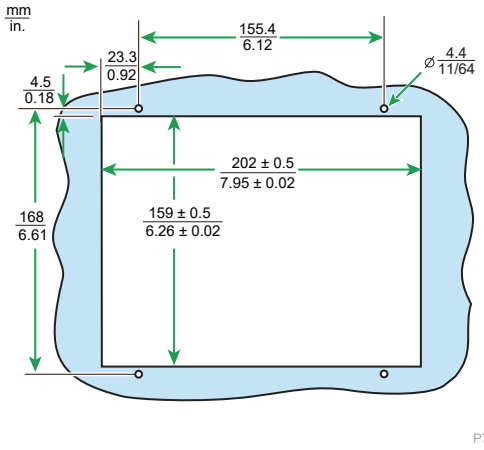
Do not fasten the fixing screws directly to the device without the panel between the fixing screws and the device.

Failure to follow these instructions can result in equipment damage.

Flush mounting the PowerLogic P7

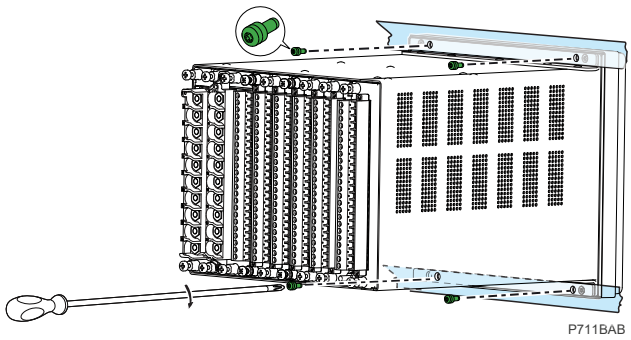
The PowerLogic P7 can be directly mounted onto panels without any accessory.

1. Prepare the cut-out in the panel for flush mounting according to the following dimensions.
   The thickness of the panel plate should be in a range of 2 to 4 mm (0.078...0.157 in.).



NOTE: The cut-out height (159 mm) takes into account the protrusion of screws fixing the L-shaped plate to the top cover of the device.

2. Fasten the device in its position with four provided M4 self-tapping screws at lower and upper parts.

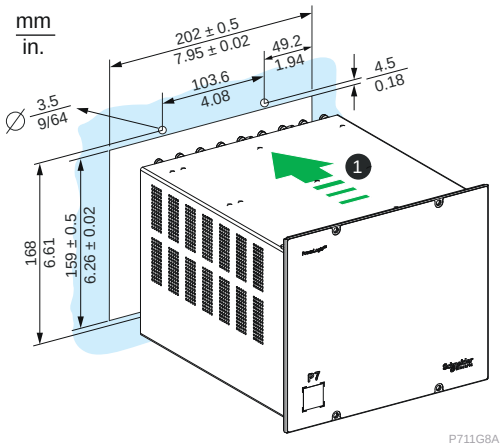


Screw	M4 x 12 mm (0.472 in.) taptite self-tapping screws integrated with washers x 4 included in the package
Tightening torque	3...3.5 N·m (26.55...30.98 lb-in)
Tool	T20 (Torx) screwdriver

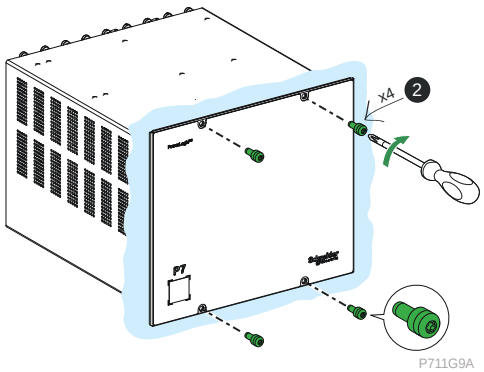
Flush mounting the PowerLogic P7 (no HMI option)

The PowerLogic P7 (no HMI option) can be flush mounted onto a panel plate that is 2 to 4 mm (0.078...0.157 in.) thick.

1. Push the device into the panel plate that has the following cut-out and holes prepared:



2. Fasten the device to the panel plate with four provided M4 self-tapping screws.



Screw	M4 x 12 mm (0.472 in.) taptite self-tapping screws integrated with washers x 4 included in the package
Tightening torque	3...3.5 N·m (26.55...30.98 lb-in)
Tool	T20 (Torx) screwdriver

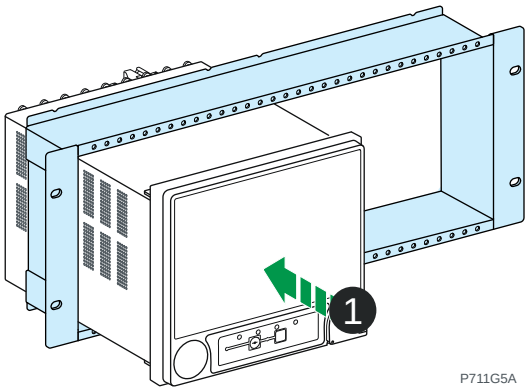
Rack mounting

Rack mounting the PowerLogic P7

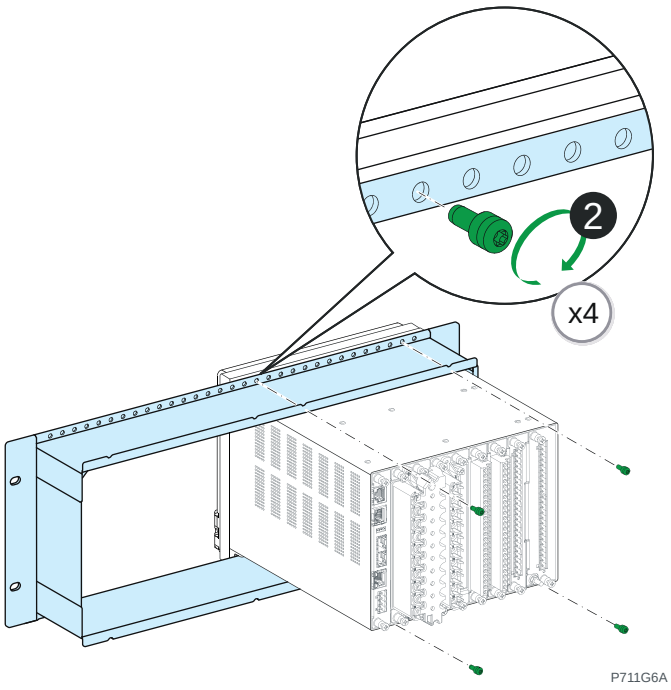
The PowerLogic P7 can be rack mounted using a rack frame (reference REL70076).

NOTE: Refer to the rack mounting guide for installation instructions.

1. Insert the PowerLogic P7 into the rack frame.

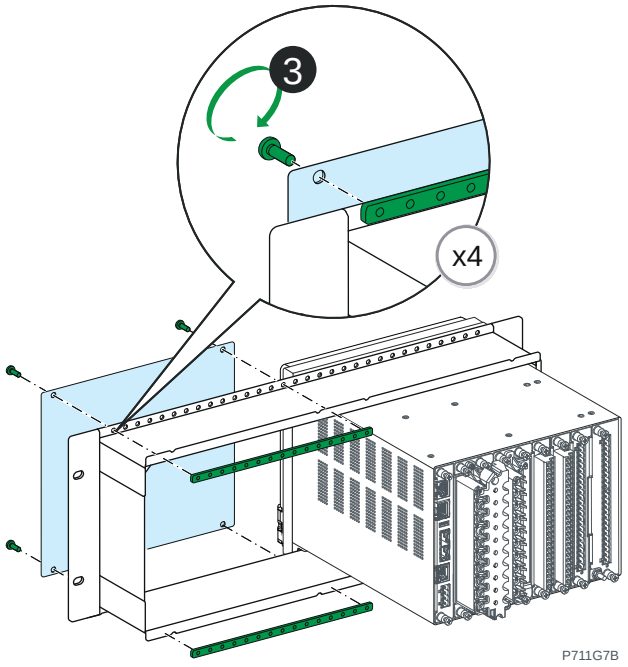


2. Attach the device to the rack frame with four provided M4 self-tapping screws.



Screw	M4 x 12 mm (0.472 in.) taptite self-tapping screws integrated washers × 4 as included in the device package
Tightening torque	3...3.5 N·m (26.55...30.98 lb-in)
Tool	T20 (Torx) screwdriver

3. Cover up the gaps left in the rack frame with blanking plates if there are still space left for future installation of other devices.



NOTE: If another device less than 40TE is to be installed in the same rack, install it at the opposite end of the rack and leave a gap to the PowerLogic P7.

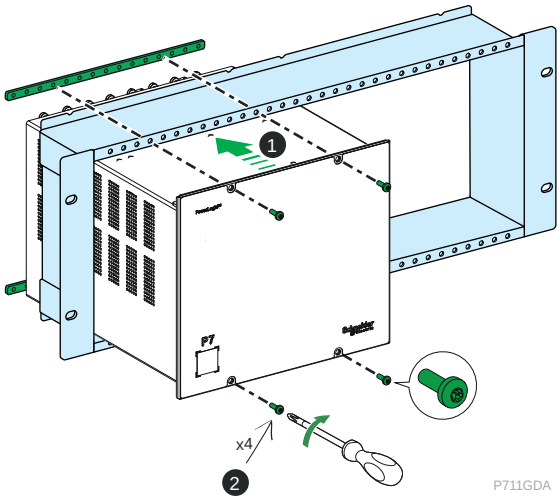
Blanking plate	Appropriate blanking pate as included in the rack frame package
Screw	M4 Torx screws and screw bars as included in the rack frame package
Tightening torque	1.17...1.43 N·m (10.36...12.66 lb-in)
Tool	T20 (Torx) screwdriver

Rack mounting the PowerLogic P7 (no HMI option)

The PowerLogic P7 (no HMI option) can be rack mounted using a rack frame (reference REL70076).

1. Insert the device into the rack frame.

2. Attach the device to the rack frame with four provided M4 machine screws and two screw bars.



Screw	M4 x 12 mm (0.472 in.) machine screws x 4 as included in the rack frame package
Tightening torque	1.17...1.43 N·m (10.36...12.66 lb-in)
Tool	T20 (Torx) screwdriver

3. As in Rack mounting the PowerLogic P7, page 43, cover up the gaps left in the rack frame with blanking plates if there are still space left for future installation of other devices.

Surface mounting

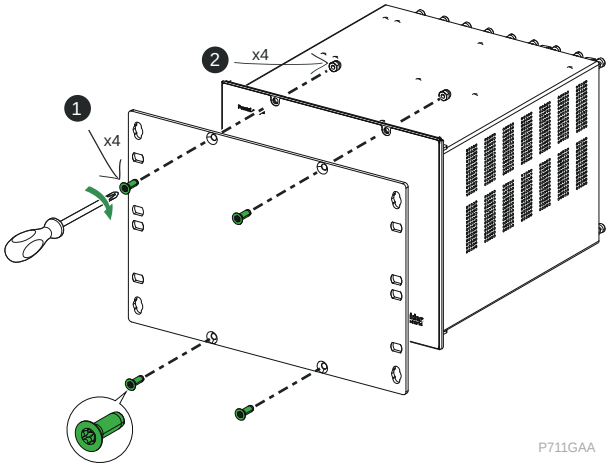
Surface mounting the PowerLogic P7 (no HMI option) with adapter plate

The PowerLogic P7 (no HMI option) can be mounted on a wall or compatible rack using the provided wall mounting adapter plate.

1. Fit the adapter plate to the device with four provided countersunk screws.

Screw	M5 x 14 mm (0.551 in.) countersunk screws x 4 as included in the package
Tightening torque	7...8.5 N·m (61.96...75.23 lb-in)
Tool	T20 (Torx) screwdriver

2. Fasten the four provided cap-nuts to the end of the countersunk screws.

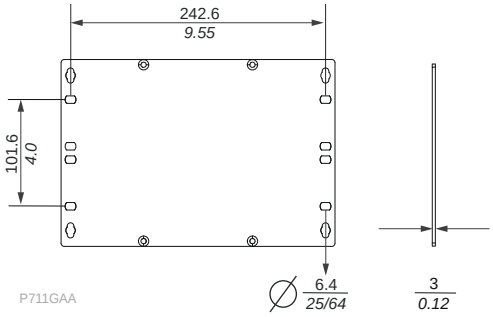


Tightening torque	1.5...2 N·m (13.28...17.70 lb-in)

3. Attach the device to a wall or mounting rack.

NOTE:

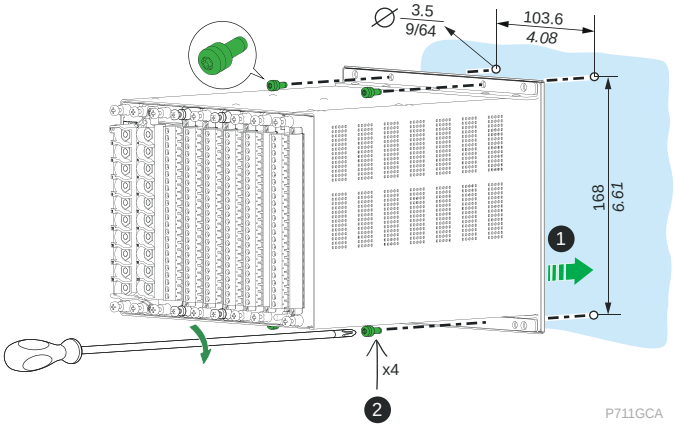
- For optimal installation, select four appropriate screw holes on the adapter plate: one pair positioned on the upper half and the other pair on the lower half. The screws used must be M6 or larger.
- The following image shows one recommended selection of holes and the thickness of the plate.



Surface mounting the PowerLogic P7 (no HMI option) without adapter plate

The PowerLogic P7 (no HMI option) can be directly mounted on a surface that is at least 2 mm (0.078 in.) thick.

1. Push the device tightly against the surface that has the following holes prepared.
2. Fasten the device with four provided M4 self-tapping screws to the surface.



Screw	M4 x 12 mm (0.472 in.) taptite self-tapping screws integrated with washers x 4 included in the package
Tightening torque	3...3.5 N·m (26.55...30.98 lb-in)
Tool	T20 (Torx) screwdriver

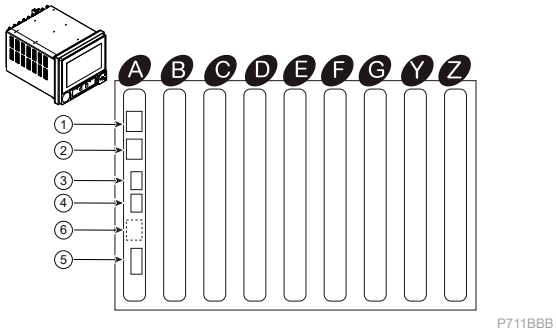
Wiring

PowerLogic P7 rear panel

Rear panel layout

The rear panel of the PowerLogic P7 contains the following modules installed in slots and identified by the callout letters.

Figure 9 - Rear panel layout



PowerLogic P7	Slot: Module and port
✓	A: CPU • ① EXT: CAN bus port for connection with additional accessories like IRIG-B module, RTD module, CLIO module. • ② Port 1: Ethernet port for single RJ45 • ③ Port 2: Ethernet port for optional SFP with HSR/PRP/RSTP/ Failover redundancy • ④ Port 3: Ethernet port for optional SFP with HSR/PRP/RSTP/ Failover redundancy • ⑤ Serial port: 2-wire RS485 • ⑥ DHMI port (only available on the no HMI option): for connection with a detachable HMI or the PowerLogic Engineering Suite
✓	B-C (2 slots): CT/VT analog input module (6CT + 3VT or 5CT + 4VT);
Optional	D-E (2 slots): CT/VT analog input module (6CT + 3VT or 5CT + 4VT); D/E/F/G: MIO (mixed binary input/output module) or DMC (direct motor control module).
✓	Y: TIO (auxiliary power supply unit)
✓	Z: PSU (power supply unit)

PowerLogic P7 rear panel terminals

Figure 10 - PowerLogic P7 rear panel terminals

(Example with slots B and C for CT/VT analog input module, slots D to G for mixed I/O or DMC modules)

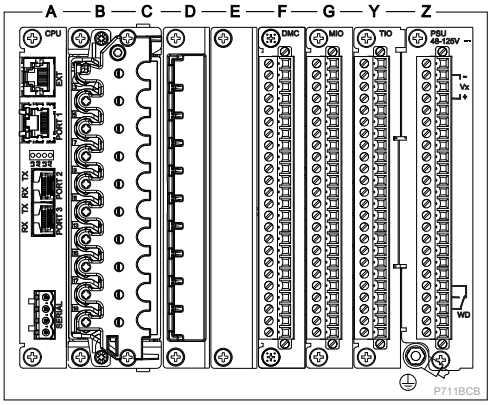
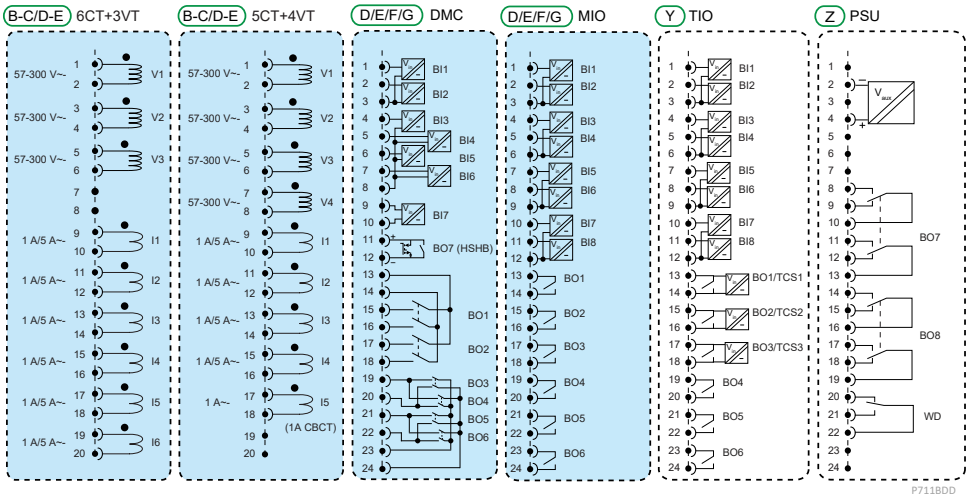


Figure 11 - PowerLogic P7 rear terminal designations



	Optional		
Ix	Current	Vx	Voltage
BIx	Binary input	CBCT	Core balance current transformer
BOx	Binary output	WD	Watchdog contact
TCS	Trip Circuit Supervision		

Default BI/BO configuration of the PSU and TIO terminals

The following table lists the default configuration of the binary input and binary output terminals in PSU and TIO of the PowerLogic P7.

Table 6 - Default BI/BO configuration of the PSU and TIO terminals

Terminal	BI/BO	Default configuration
Y1, Y3	BI1	52b
Y2, Y3	BI2	52a
Y13, Y14	BO1	Trip
Y15, Y16	BO2	Close
Y17, Y18	BO3	CB fail
Y13, Y14	TCS1	Trip CCT OK
Y15, Y16	TCS2	Close CCT OK
Z8-Z13	BO7	2pole trip
Z14-Z19	BO8	2pole close
Z20, Z21, Z22	WD	Watchdog (not configurable)

Typical application diagrams

The following sections describe typical application diagrams.

NOTE: Due to the flexible hardware configuration of the PowerLogic P7, the slot number and terminal number of the binary I/O modules in the following diagrams are just for an example. The actual number should be based on the location of other modules such as CT/VT, I/O.

CT typical application

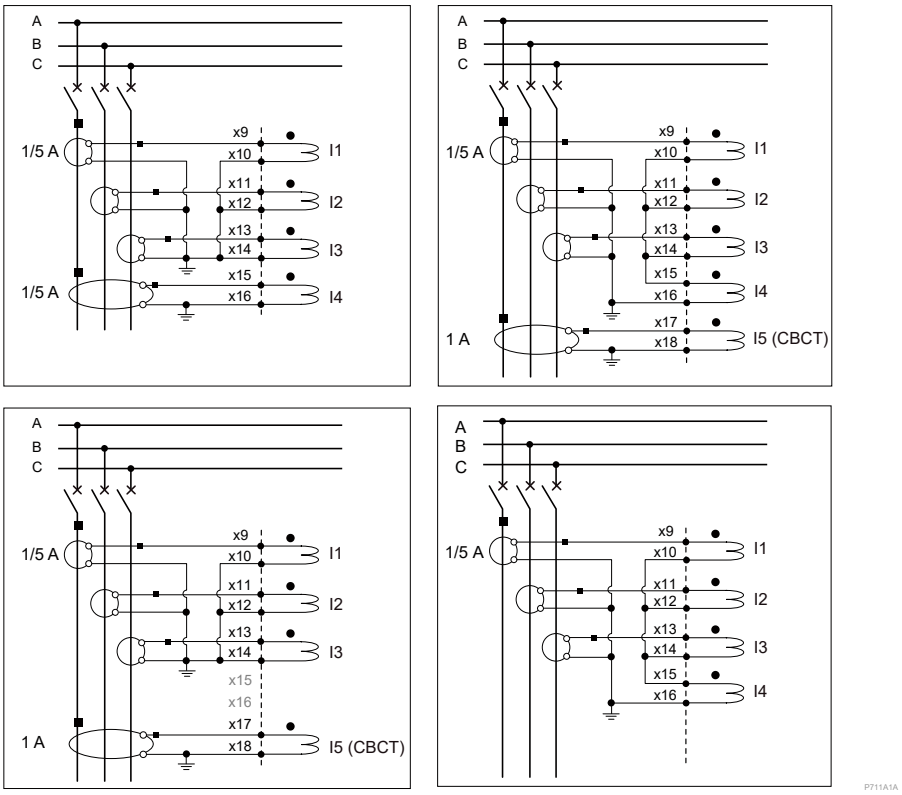
The current input physical channels are mapped to the bays and subsequent protection functions using CT groups.

These groups can be configured to suit the application needs. The number and type available depend on the ordered application level of the product.

In the example below, the first application shown in Three phase and ground connection, page 49, one three-phase CT group and one single phase CT group are used with the three-phase CT group set to *3ph* and the single phase group set to *IN*.

A similar mechanism is used for VT's. Refer to CT group, page 336 and VT group, page 341 for more mapping details.

Figure 12 - Three phase and ground connection



■ P1

■ S1

CBCT: Core balance current transformer

x: The first slot used by the CT/VT analog module which takes 2 slots. For example, if the analog module is fitted in slots B & C then x9 becomes B9.

For two-phase CT connections, only IA and IC are used by the PowerLogic P7 (see the figure below).

Figure 13 - Two phase and ground connection

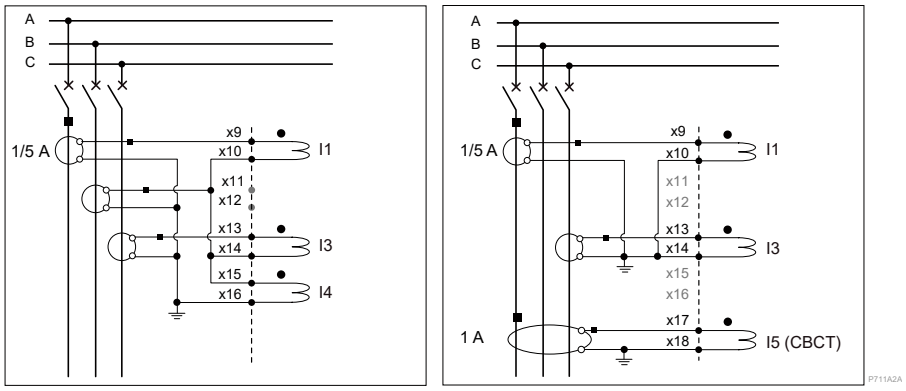
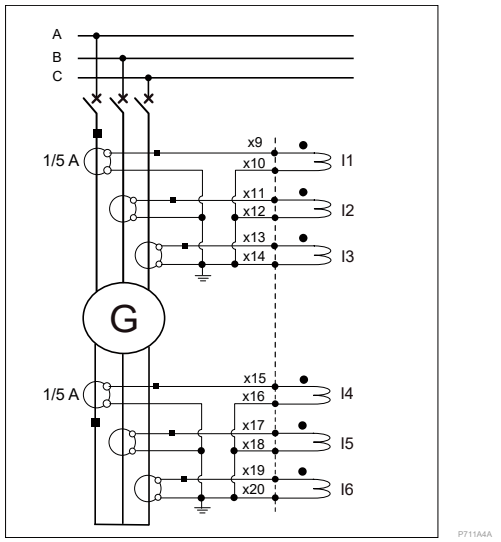
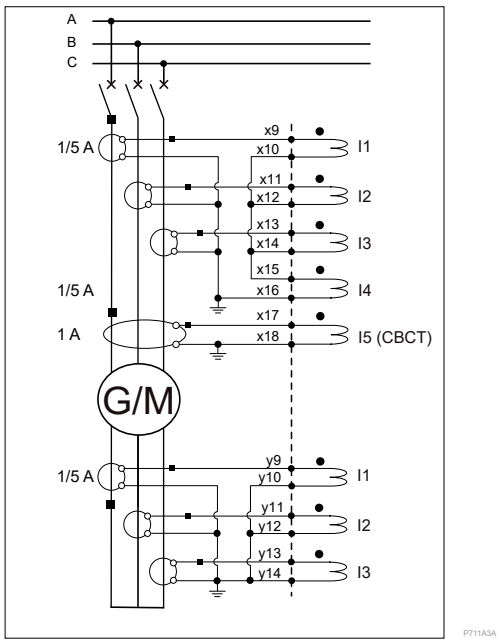


Figure 14 - Three phase connection for differential application





y: The CT/VT analog module takes 2 slots. For example, if the analog module is fitted in slots D & E then y9 becomes D9.

VT typical application

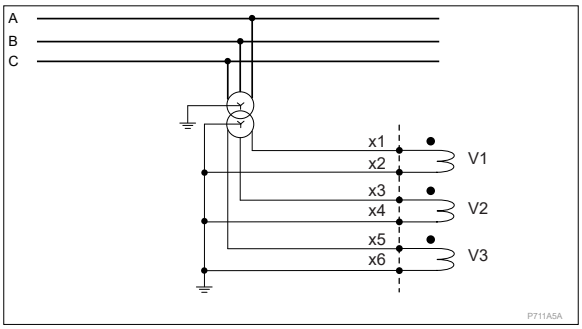
The voltage input physical channels are mapped to the bays and subsequent protection functions using VT groups.

These groups can be configured to suit the application needs. The number and type available depend on the application level available to the product.

In the example below, shown in Three phase-to-ground voltages and one phase-to-ground voltage, page 51, one three-phase VT group and one single phase VT group are used with the three-phase VT group set to *3ph* and the single phase group set to *Aph*.

Refer to VT group, page 341 for more mapping details.

Figure 15 - Three phase-to-ground voltages



x: The first slot used by the CT/VT analog module which takes 2 slots. For example, if the analog module is fitted in slots B & C then x1 becomes B1.

Figure 16 - Three phase-to-ground voltages and one neutral voltage

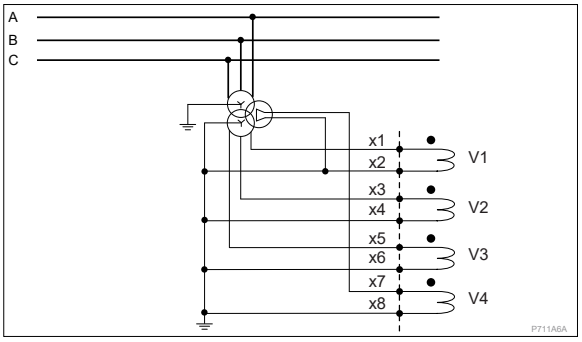


Figure 17 - Three phase-to-ground voltages and one phase-to-ground voltage

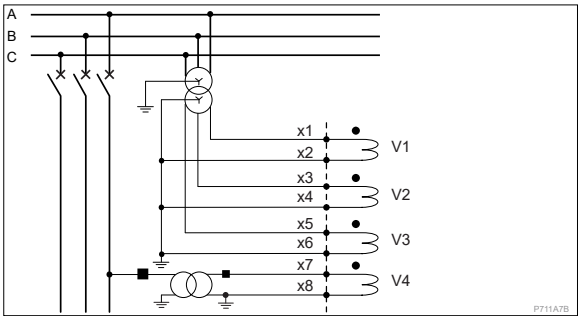


Figure 18 - Three phase-to-ground voltages and one phase-to-phase voltage

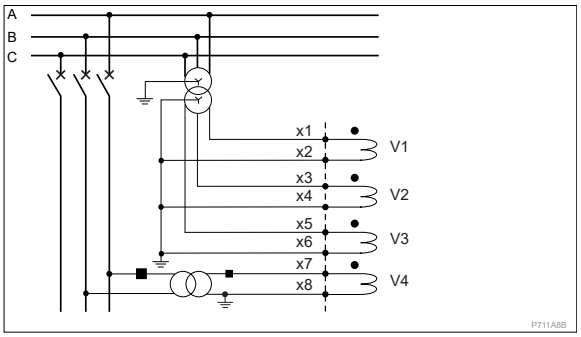


Figure 19 - Two phase-to-phase voltages

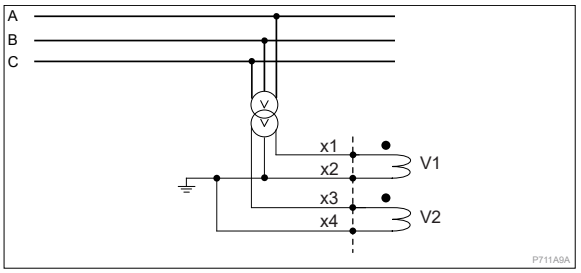


Figure 20 - Two phase-to-phase voltages and one neutral voltage

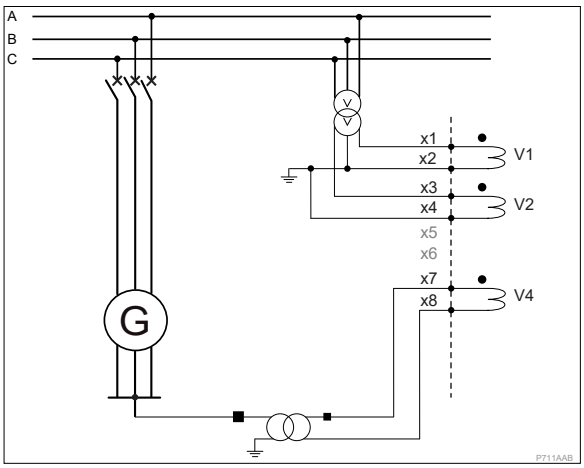
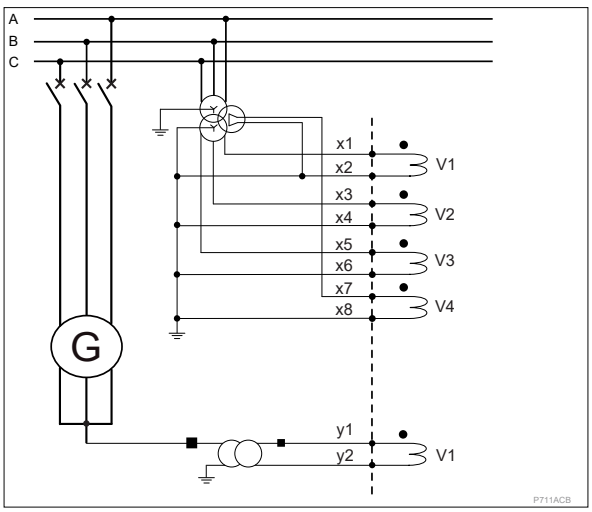


Figure 21 - Three phase-to-ground voltages and two neutral voltages



y: The CT/VT analog module takes 2 slots. For example, if the analog module is fitted in slots D & E then y1 becomes D1.

Direct LV connection (up to 480 V)

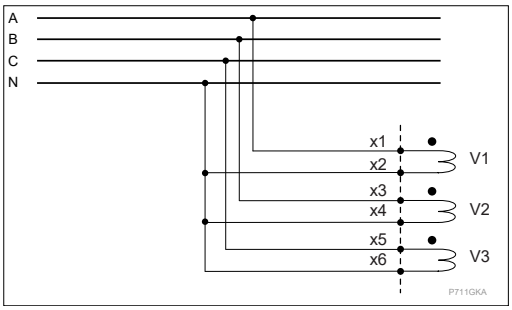
Low-voltage systems (up to 480 V) can be directly connected to the voltage input physical channels without VTs using phase to neutral connections.

The voltage input physical channels are mapped to the bays and subsequent protection functions using VT groups.

These groups can be configured to suit the application needs. The number and type available depend on the application level available to the product.

Refer to VT group, page 341 for more mapping details.

Figure 22 - Direct LV connection



Wiring on the rear panel

⚠DANGER

FIRE HAZARD

Apply proper tightening torque to all wire connections.

Failure to follow these instructions will result in death or serious injury.

Slot B-C/D-E: CT/VT analog module

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

- Do not open the secondary circuit of a live CT.
- The secondary of the line CT must be shorted before opening any connections to it.
- A maximum of two ring terminals can be used for each terminal on the CT/VT module only on the lower row. Do not connect more than two ring terminals on a single terminal.

Failure to follow these instructions will result in death or serious injury.

⚠WARNING

UNINTENDED EQUIPMENT OPERATION

- Protect the rear connector of CT/VT analog module with the CT/VT IP20 transparent cover after cabling.

Failure to follow these instructions can result in death, serious injury, or equipment damage.

The external ring terminal blocks have integral short circuiting for the CT circuits and can be removed from the device without the secondary side open-circuit.

Screws and jumpers for CT/VT terminals

PowerLogic P7 devices are delivered with screws and jumpers for CT/VT terminals. Screws and jumpers are included in the accessory box.

The 3-terminal jumper is provided to support a common connection.

Figure 23 - Screws and jumpers for CT/VT terminals



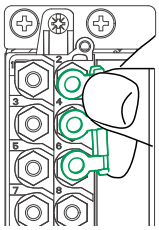
P711BEA

- Three-terminal jumpers ①
- Terminal screws integrated with washers ②

General cabling operation on connector of CT/VT module

The following procedure presents the general mounting and cabling operation on the connector of CT/VT module:

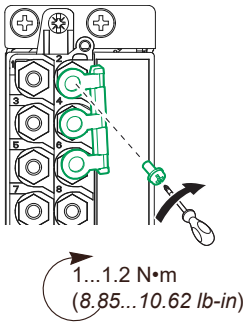
1. Insert and connect the terminal jumper for common connections.



P711BYA

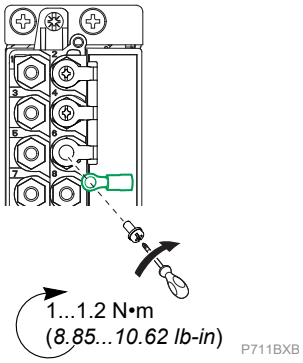
Tools	Application connection diagram

2. Fasten the terminal jumper with the provided terminal screws.



Fasteners	Terminal screws included in the accessory box
Tightening torque	1...1.2 N·m (*8.85...10.62 lb-in*)
Tool	6.5 mm flat or PH2 screwdriver

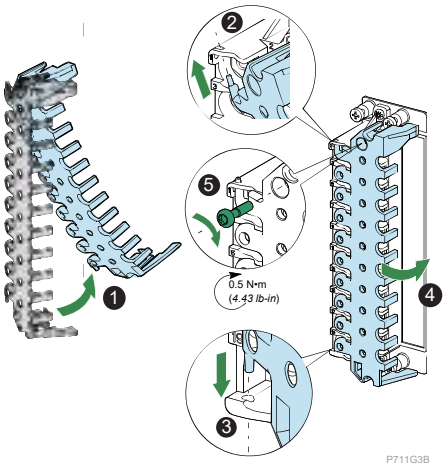
3. Connect the ring lug end of the cables to the terminal using the provided terminal screws.



Fasteners	Terminal screws included in the accessory box
Tightening torque	1...1.2 N·m (*8.85...10.62 lb-in*)
Tool	6.5 mm flat or PH2 screwdriver

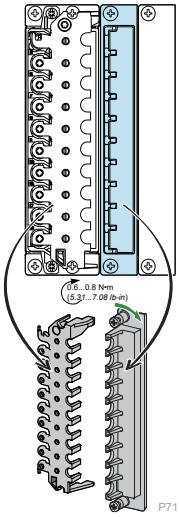
NOTE: See Wiring details, page 58 for the wire size.

4. Optionally, place and insert the CTVT IP20 transparent cover on the terminal to prevent contacting with the terminal after cabling.



Screws	ST3 x 12 mm (in.) taptite self-tapping screws
Tightening torque	0.5 N·m (*4.43 lb-in*)
Tool	T10 (Torx) screwdriver

5. Optionally, replace the blankplate with the assembly barrier cover to prevent the side access to the terminal if any blankplate is equipped immediately to the right of a CT/VT module.



Tightening torque	0.6...0.8 N·m (*5.31...7.08 lb-in*)
Tool	#2 Phillips screwdriver

Phase voltage with VT inputs

The phase voltage inputs are situated in the upper part of the connector of CT/VT analog input module, terminals 1 to 8 (5 CT+4 VT) or terminals 1 to 6 (6 CT+3 VT). The voltage measuring inputs are the following:

Figure 24 - Phase voltage inputs on the connector of CT/VT analog input module (5 CT+4 VT)

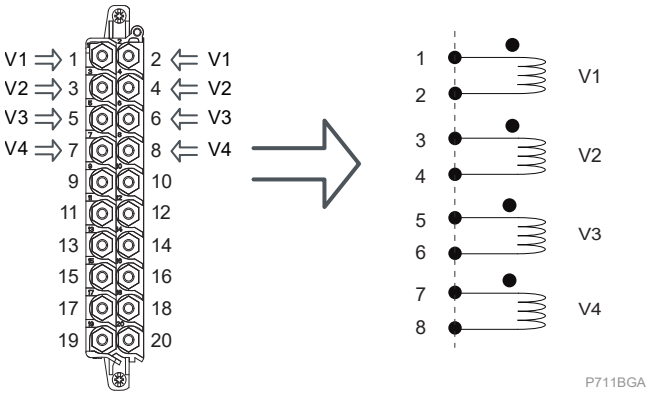
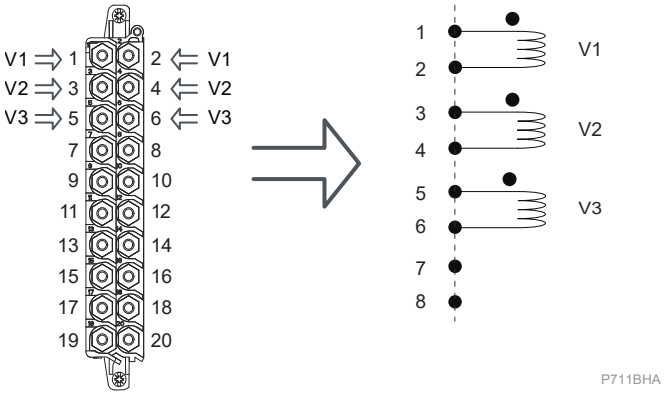


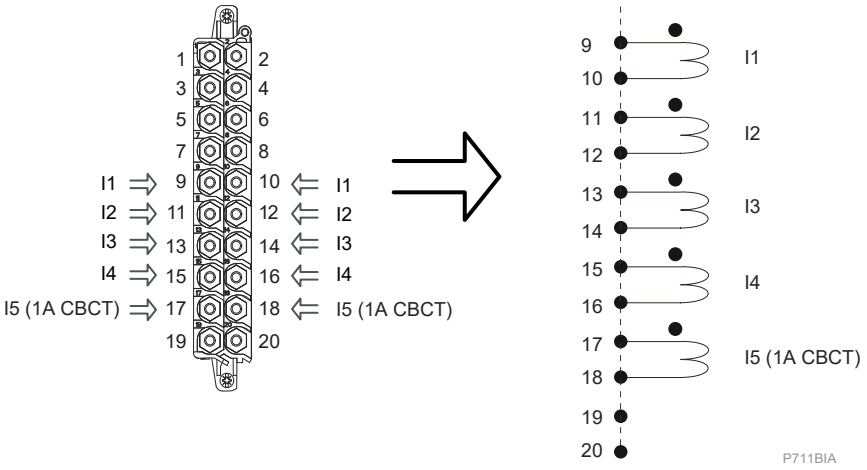
Figure 25 - Phase voltage inputs on the connector of CT/VT analog input module (6 CT+3 VT)



Phase currents with CT inputs and ground fault current inputs

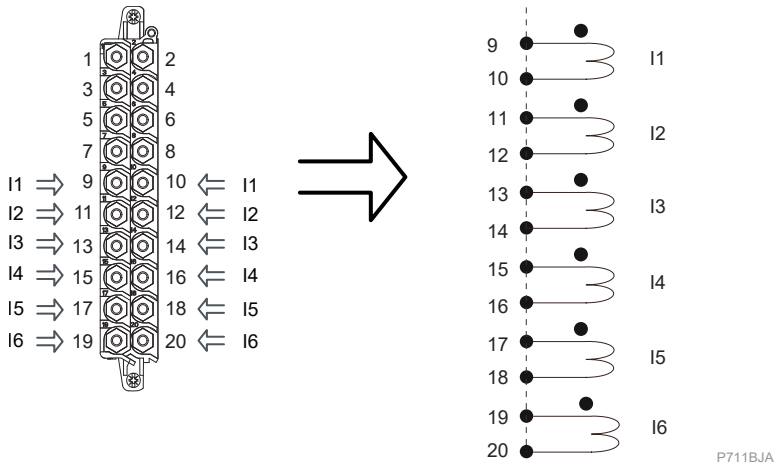
The current inputs are located in the lower part of the connector of CT/VT analog input module, terminals 9 to 18 (5 CT+4 VT) or terminals 9 to 20 (6 CT+3 VT). The current measuring inputs are the following:

Figure 26 - Current inputs on the connector of CT/VT analog input module (5 CT+4 VT)



CBCT: Core balance current transformer

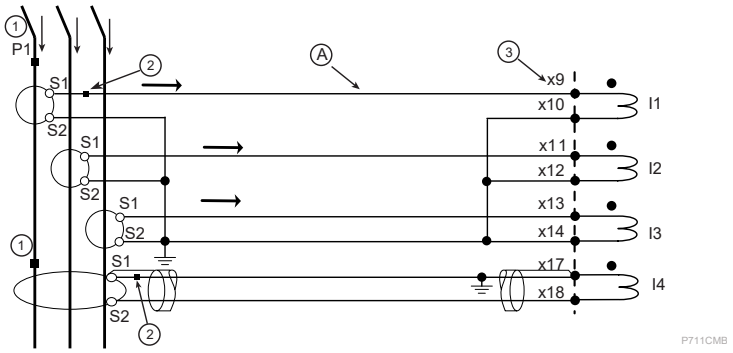
Figure 27 - Current inputs on the connector of CT/VT analog input module (6 CT+3 VT)



Current Transformer Connections

PowerLogic P7 devices use current transformers to measure phase or residual currents. The current transformer connections are as follows.

Figure 28 - Connecting the current transformers with example of ground fault connection (shielded)



where:

- ① Terminal P1[5] (primary current).
- ② Terminal S1/S2[6] (secondary current).
- ③ Terminal x[7] + terminal number.
- Ⓐ Cabling between the CTs and the terminal.

NOTE: CBCT - Conductors contained in the same strand, in a sheath

Wiring details

Refer to the table below for the detailed information on wiring the screw-type input connectors of the CT/VT analog input module:

Applicable cable end	Wire gauge	Tightening torque	Tool	
Ø1 Ø2 P711BKB Ø1 = 4 mm (*0.16 in.*) Ø2 < 10 mm (*0.39 in.*)	0.5 ... 1.5 mm² (AWG 20 ... 16) 1.5 ... 2.5 mm² (AWG 16 ... 14) 2.5 ... 6 mm² (AWG 14 ... 10)	1...1.2 N·m (*8.85...10.6 lb-in*)	(-) 6.5 mm (*1/4 in.*) screwdriver	(+) PH2 screwdriver

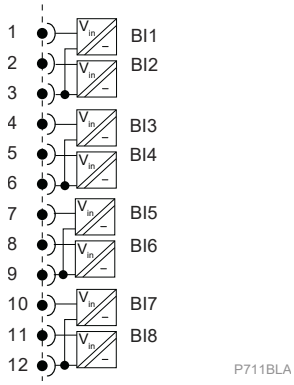
NOTE: Use only single strand-wire or stranded wire with insulated crimp terminals.

Binary input connections

The PowerLogic P7 provides binary inputs isolated from ground, with a common connection point, for instance, BI1 and BI2.

5. Markings of current transformer terminals P1 and P2 according to IEC 60044-1 Standard.
6. Markings of current transformer terminals S1 and S2 according to IEC 60044-1 Standard.
7. The terminal reference x refers to the first slot used by the first analog module which takes 2 slots. For example, if the first analog module is fitted in slots B & C then x9 becomes B9.

Figure 29 - Binary input connections



The isolated binary inputs with a common connection point are isolated from ground, but two of them are grouped together using the same common return and therefore not isolated to each other. They should be used to acquire data from the following digital sensors:

- Isolated sensors.
- Sensors that are not isolated but come from the same zone of an installation with equipotential bonding.
- Sensors that preferably come from the same equipment. The different binary inputs are contained in the same cable.

The electrical conductors connected to the binary inputs of PowerLogic P7 devices should run along the metal structures of the cubicle to reduce ground loops. The conductors are contained in the same strand and, if possible twisted, to avoid the creation of cabling loops.

NOTICE

UNINTENDED EQUIPMENT OPERATION

- Avoid large cabling loops in the various power supplies when connecting the binary inputs.
- Do not short-circuit any of the galvanic insulation.

Failure to follow these instructions can result in improper operation or equipment damage.

When the environmental and installation conditions are highly unfavorable for the PowerLogic P7, a shielded twisted pair should be used. In such cases, the cable shielding is connected to the local ground at both ends (provided that the installation has an equipotential bonding network).

Slot Z: power supply + 2 Double Pole C/O Contact (DPCO) + WD (PSU module)

Power supply

⚠DANGER

FIRE HAZARD

- Protect the power supplying circuit of the PowerLogic P7 against overcurrents. (MCB recommendation - DC: 6 A; AC: 10 A)
- For breaking capacity higher than 40 W with L/R = 40 ms, protect the binary output contacts with an additional customer protection (RC or zener diode).

Failure to follow these instructions will result in death or serious injury.

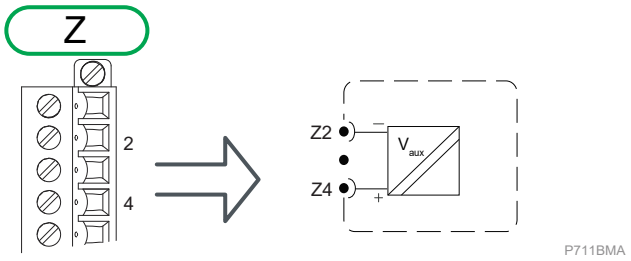
The power supply available for the PowerLogic P7 is:

- 24...34 V DC
- 48...125 V DC
- 110...250 V DC/AC

The nominal voltage range of the PowerLogic P7 is specified on the slot Z board.

NOTICE
POWER SUPPLY DAMAGE Make sure that the nominal value of the auxiliary device voltage corresponds with the nominal value of the auxiliary system voltage before connecting the auxiliary voltage to the PowerLogic P7. **Failure to follow these instructions can result in equipment damage.**

Figure 30 - Power supply terminals on connector Z

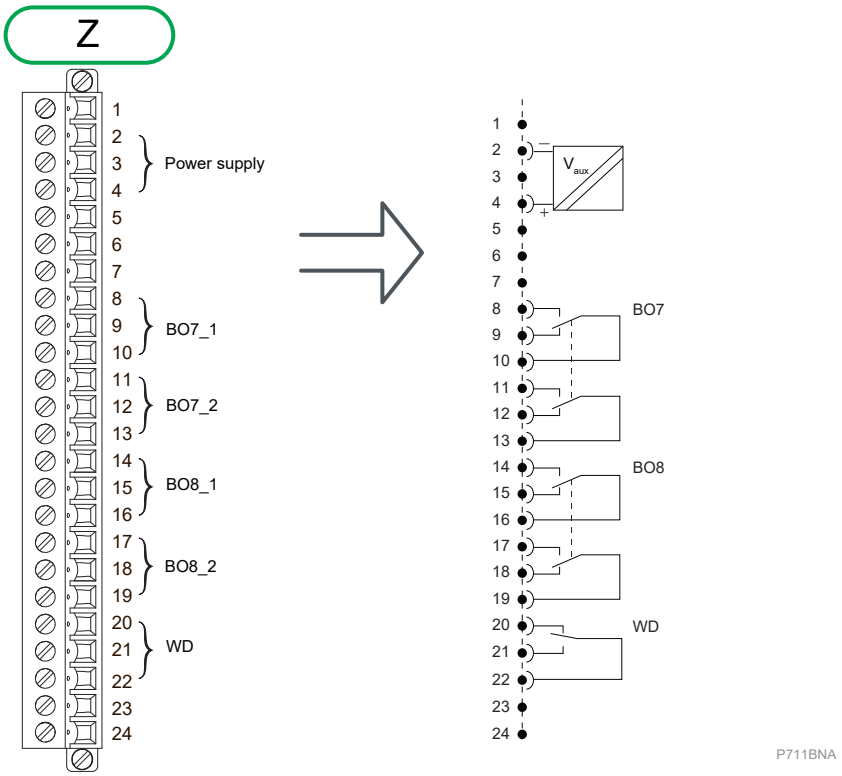


Binary Outputs

The binary output module (WD + 2DPCO) is mounted in slot Z. BO7 and BO8 are equipped with a 2-pole switching contact to control a circuit breaker. Binary output WD is defined as a Watchdog contact. The contacts are referred to BO7 and BO8 as they are driven from the TIO board. The setting and operation of these contacts is part of Slot Y configuration

The configuration of the 24-terminal connector of the module is shown in the following figure:

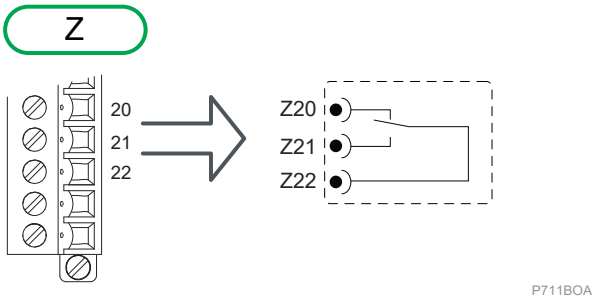
Figure 31 - Configuration of connector Z



Watchdog

The watchdog (self-monitoring) is a changeover contact provided on slot Z, binary output WD, to indicate the health of the device (refer to Watchdog relay, page 459). Schneider Electric strongly recommends that these contacts are hard-wired into the substation's automation system for alarm purposes.

Figure 32 - Watchdog terminals on connector Z



NOTE: Refer to Wiring accessories for the PSU, TIO, MIO or DMC modules, page 64 for the detailed information on wiring the terminals of this module.

Slot Y: auxiliary power supply module (TIO)

The PowerLogic P7 is equipped with an auxiliary power supply module (with 8 binary inputs, 6 binary outputs) in slot Y. Binary outputs BO1, BO2, BO3 have parallel inputs to allow supervision of trip and close circuits.

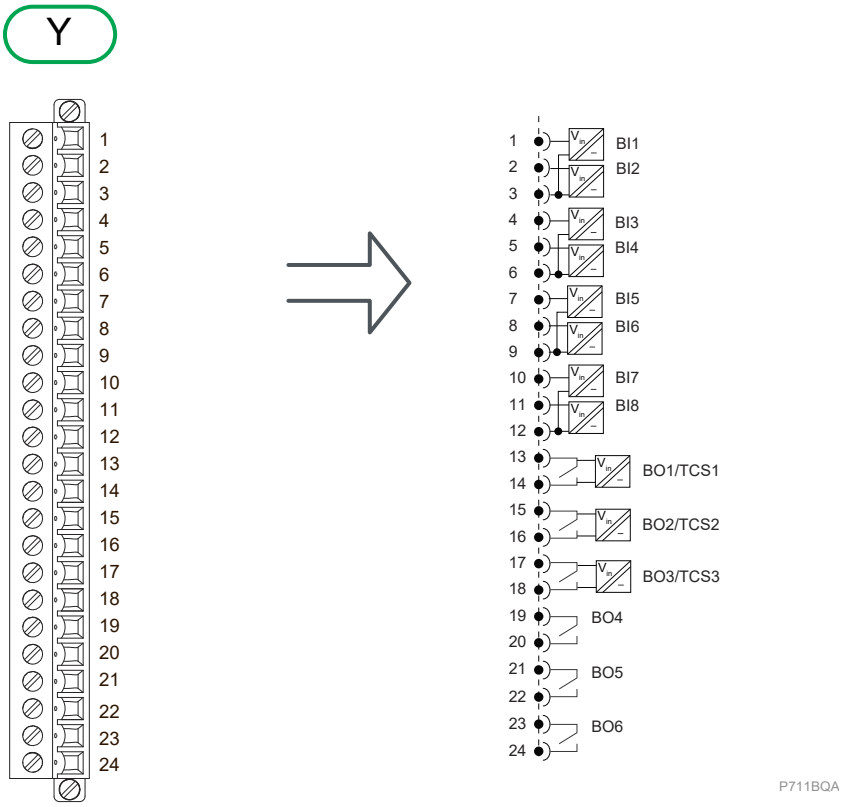
NOTE: Due to the opto connected across the output of contacts BO1 to BO3, then test equipment can incorrectly interpret that the contact remains operated even after resetting. Reversing the connection polarity can avoid this issue.

The operating nominal voltage for binary inputs is:

- 24...250 V DC
- 220...250 V AC

The configuration of the 24-terminal connector of the auxiliary power supply module is shown in the following figures:

Figure 33 - Configuration of terminals in slot Y



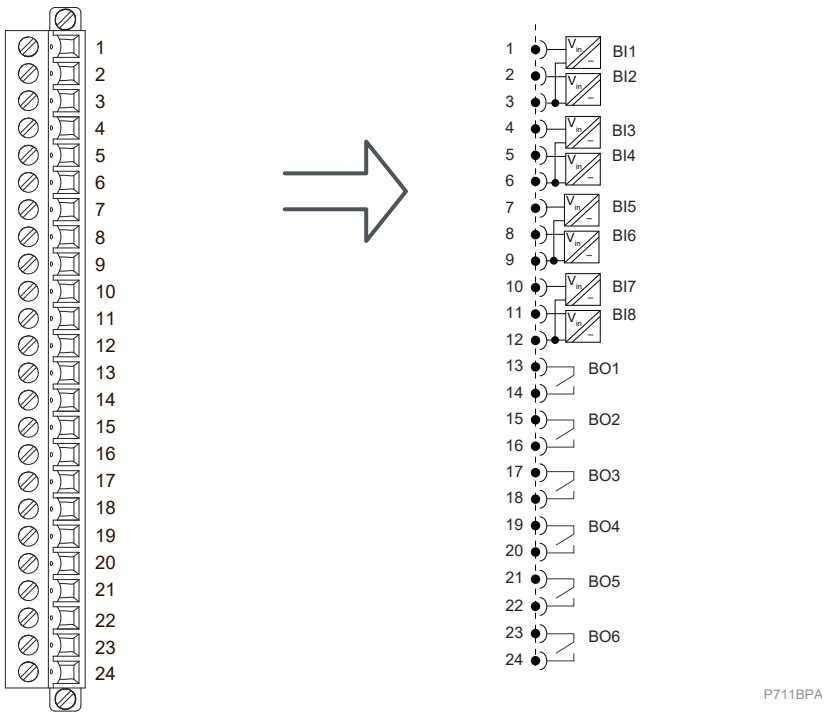
NOTE: Refer to Wiring accessories for the PSU, TIO, MIO or DMC modules, page 64 for the detailed information on wiring the terminals of this module.

Slot D, E, F, G: additional mixed binary input/output (MIO) modules (8I6O)

The PowerLogic P7 can be provided with additional MIO modules (8I6O) in slot D, E, F and G. The configuration of the 24-terminal connector of the module is shown in the following figures.

Figure 34 - Configuration of connector

D/E/F/G



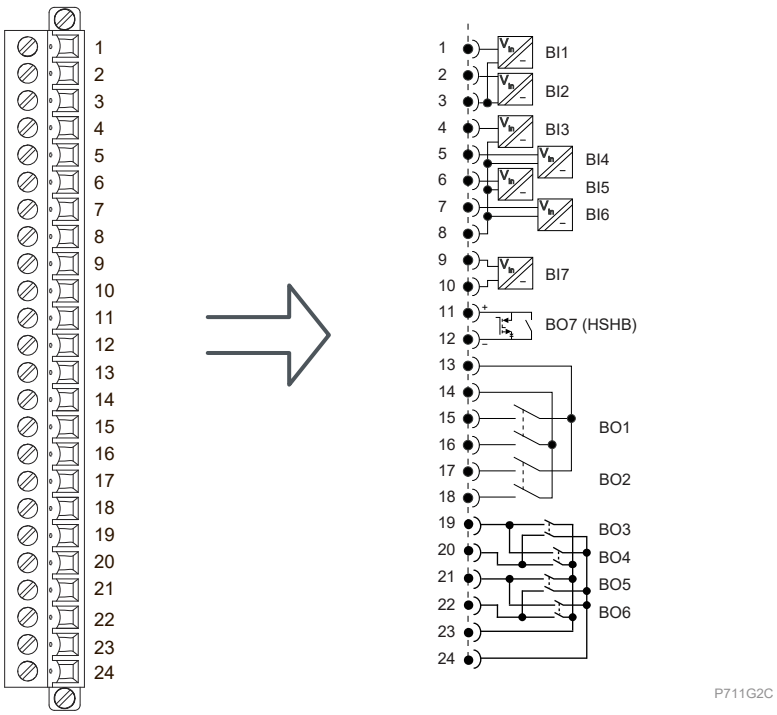
NOTE: Refer to Wiring accessories for the PSU, TIO, MIO or DMC modules, page 64 for the detailed information on wiring the terminals of this module.

Slot D, E, F, G: additional direct motor control (DMC) module (7I7O)

The PowerLogic P7 can be provided with an additional DMC module (7I7O) in slot D, E, F or G. This module provides outputs which can be used to provide reversible voltage direct to equipment motors to open or close the isolator. The configuration of the 24-terminal connector of the module is shown in the following figure.

Figure 35 - Configuration of connector

D/E/F/G



BO1~BO6 are equipped with 4 Double Pole C/O Contacts for motor control.

NOTE: Refer to Wiring accessories for the PSU, TIO, MIO or DMC modules, page 64 for the detailed information on wiring the terminals of this module.

Wiring accessories for the PSU, TIO, MIO or DMC modules

Wiring the screw-type terminals

The detailed information for wiring the screw-type BI/BO terminals in PSU (slot Z), TIO (slot Y), MIO or DMC (slot D/E/F/G) is listed in the table below:

Table 7 - Wiring specification

Cable end	Wire gauge	Tightening torque	Tool
 P711AGA Contact tip length L = 12 mm (*0.5 in.*)	Single wire: 0.2...2.5 mm² (AWG 24...14) Double wires: 0.2...1.5 mm² (AWG 24...16)	0.5...0.6 N·m (*4.4...5.3 lb-in*)	⊖ 3.5 mm (*9/64 in.*) flat blade screwdriver

NOTE: Use only single strand-wire or stranded wire with insulated crimp terminals.

Connecting ground

⚠⚠DANGER

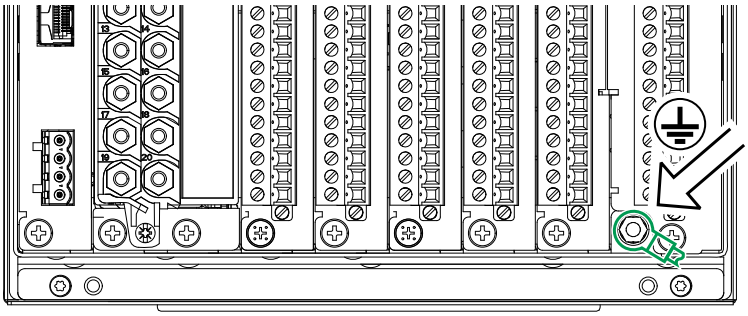
HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

- Connect the device to the ground with a nut and a washer using the indicated stud terminals.
- Check the equipotential grounding network and test the grounding during installation.

Failure to follow these instructions will result in death or serious injury.

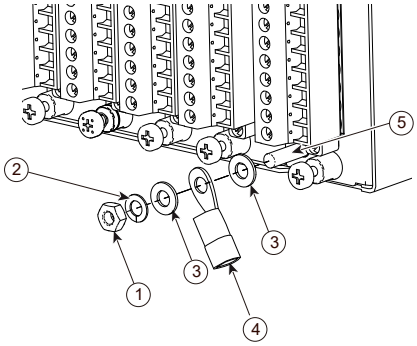
The ground connections are accessible on the rear panel of the devices. For the PowerLogic P7, there is one connector located in the bottom right corner of the device.

Figure 36 - Ground studs on the PowerLogic P7



P711BRA

Figure 37 - Fixing the grounding cable to the PowerLogic P7

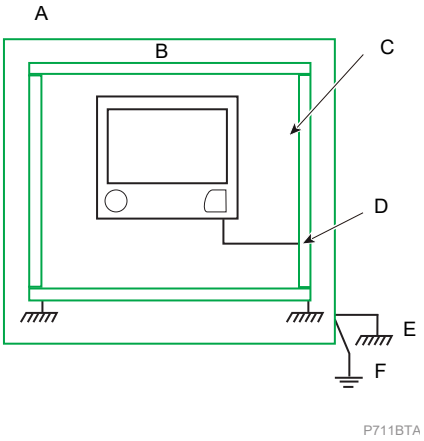


P711BSA

①	M4 hexagon nut	④	Grounding cable
②	Spring washer	⑤	Ground stud on the device
③	Plate washer		

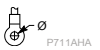
Every PowerLogic P7 device must be connected to the local ground bar using one M4 ground stud on the device case to prevent dangerous voltages being present in case of a wiring fault or damage to the product. Also, it ensures that the PowerLogic P7 meets EMC claims.

Figure 38 - Compartment grounding terminal



A	Metal upright of the LV compartment	D	Ground connection made to a surface with no paint, varnish or any insulating material. Spring washers must be used.
B	LV compartment	E	Local ground
C	The PowerLogic P7 is installed in the LV compartment near the grounding terminal, or else near one of the metal uprights	F	Electrical protection

The minimum recommended wire size is 2.5 mm² (AWG 12) and should have a ring terminal at the device end. Due to the limitations of the ring terminal, the maximum wire size that can be used is 6.0 mm² (AWG 10) per wire.

Termi-nal type	Applicable cable end	Wire gauge	Max. wire length	Tightening torque	Tool
Ground stud	 Ø = 4 mm (*0.16 in.*)	2.5 mm² 2.5...6 mm² (AWG 12...10)	2 m (*6.5 ft.*)	1...1.2 N·m (*8.85...10.62 lb-in*)	7 mm spanner

NOTE: To avoid any possibility of electrolytic action between brass or copper ground conductors and the rear panel of the PowerLogic P7, precautions should be taken to isolate them from one another. It is recommended to place a nickel-plated or insulating washer between the conductor and the PowerLogic P7 case or to use tinned ring terminals.

Rear communication ports and modules at Slot A

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

- Do not connect items of equipment with different ground potentials with an RJ45 cable.
- Do not use RJ45 cable longer than 10 m (32.8 ft) between a merging unit and an IED.

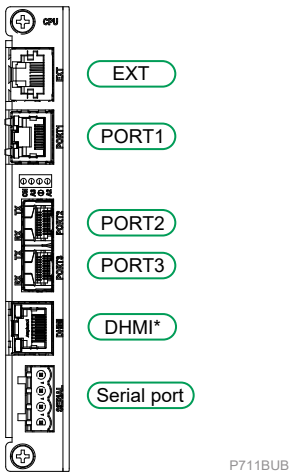
Failure to follow these instructions will result in death or serious injury.

The PowerLogic P7 includes rear communication ports and modules with RJ45 or fiber optic (optional) connections.

The ports and modules are accessible from Slot A (CPU) of the rear panel.

Layout of the communication ports

The following figure shows the layout of the communication ports on both the PowerLogic P7 and the PowerLogic P7 (no HMI option):



NOTE: The DHMI port is only available on the PowerLogic P7 (no HMI option).

Table 8 - Communication ports on the PowerLogic P7

Port	Description
EXT	CAN bus port for connection with accessories like IRIG-B module, RTD module, CLIO module
PORT1	Ethernet port for single RJ45
PORT2 PORT3	Ethernet port for optional SFP modules: • 100/1000 Mbps RJ45 • 100/1000 Mbps fiber optic multimode • 100/1000 Mbps fiber optic singlemode
DHMI (only on the no HMI option)	Ethernet port for connection with the detachable HMI or the PowerLogic Engineering Suite
Serial port	2-wire RS485 serial port

Port 1: Ethernet communication port

Port 1 is a single Ethernet communication port with fixed RJ45 connector by default, and it is located at slot A (CPU).

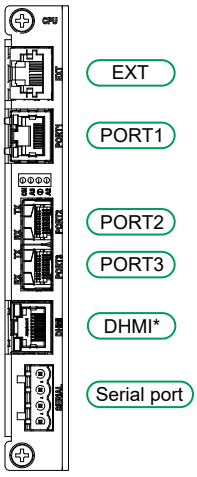
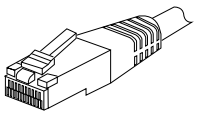


Table 9 - Characteristics of the Ethernet communication port

Characteristics	
Location	Port 1 at slot A
Connection	RJ45 connector with communication indicators  P711AIA
Ethernet connection	100 Mbps
Maximum cable length	100 m (328.08 ft)

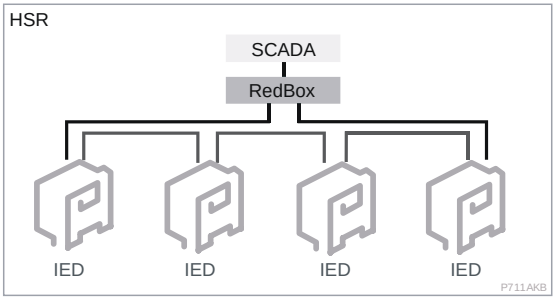
Port 2 and Port 3: Ethernet port for optional SFP modules

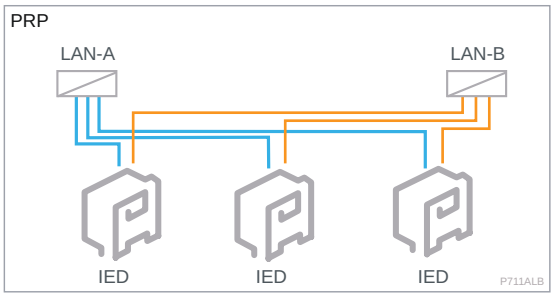
Port 2 and Port 3 are Ethernet communication ports for the optional SFP modules. The SFP modules can be selected as accessories when ordering the device or purchased later and installed on site.

The SFP modules are available for copper wire, multi-mode fiber optic or single-mode fiber optic connection.

The SFP modules with RJ45 or LC connector provide RSTP (Rapid Spanning Tree Protocol), PRP (Parallel Redundancy Protocol), HSR (High-availability Seamless Redundancy), and Failover redundancy, which are selectable by configuration. When two SFP modules are used, instantaneous reconfiguration of the communication system is allowed without communication packet loss. When only one SFP module is used, the default Failover mode should be selected which will work with the SFP installed in either port.

Figure 39 - Example of SFP module connection





Installing the optional SFP modules

The SFP modules are designed with a self-locking mechanism and are hot swappable. After sliding all the way into position along the ports, the module locks itself in final place. The bale-clasp latch at one end locks the SFP module in place. Insert the SFP modules into port 2 and port 3 on slot A.

Figure 40 - Installing the optional SFP module

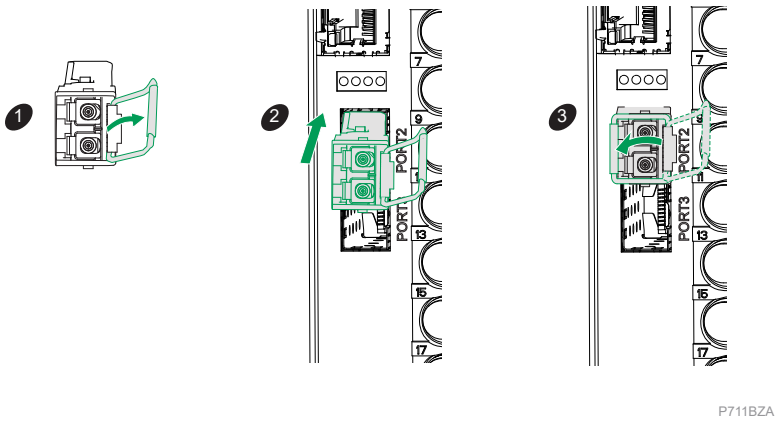
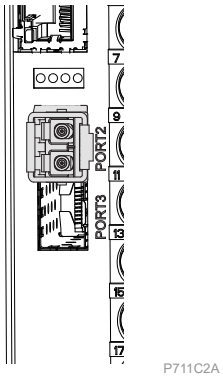


Figure 41 - Example of installed SFP module with LC connector



SFP module with RJ45 connector (reference REL70062)

Table 10 - Characteristics of the SFP module (reference REL70062)

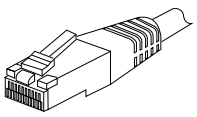
Characteristics	
Location	Port 2 or Port 3
Connector	RJ45 connector with communication indicators 
Ethernet connection	100/1000 Mbps

Table 10 - Characteristics of the SFP module (reference REL70062) (Continued)

Characteristics	
Protocol	Failover, RSTP, HSR or PRP
Maximum cable length	100 m (328.08 ft)

SFP module with fiber optic connector

⚠WARNING

EYE DAMAGE AND BLINDNESS

Never look into the end of the fiber optic.

Failure to follow these instructions can result in serious injury.

NOTICE

IMPROPER EQUIPMENT OPERATION

- Use only Schneider Electric approved optical transceiver components.
- Never replace the optical transceiver components with unauthorized manufactured parts.

Failure to follow these instructions can result in equipment damage.

Use optical power meters to determine the operation or signal level of the device.

If electrical-to-optical converters are used, they must have management of character idle state capability (when the fiber optic cable interface is "Light off").

Specific care should be taken with the bending radius of the fibers, and the use of optical shunts is not recommended as these can decrease the communication performance of the transmission path lifetime.

Table 11 - Characteristics of the SFP module, multi-mode (reference REL70063)

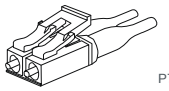
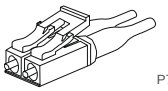
Characteristics	
Location	Port 2 or Port 3
Connector	LC connector  P711AMA
Ethernet connection	100 Mbps
Protocol	Failover, RSTP, HSR or PRP
Optical wavelength	1310 nm
Fiber type	Multi-mode glass fiber
Maximum attenuation (fiber optic + connectors)	14 dB (at fiber optic diameter: 62.5/125 µm or 50/125 µm)
Maximum range	2 km (6561.68 ft)

Table 12 - Characteristics of the SFP module, single-mode (reference REL70064)

Characteristics	
Location	Port 2 or Port 3
Connector	LC connector

Table 12 - Characteristics of the SFP module, single-mode (reference REL70064) (Continued)

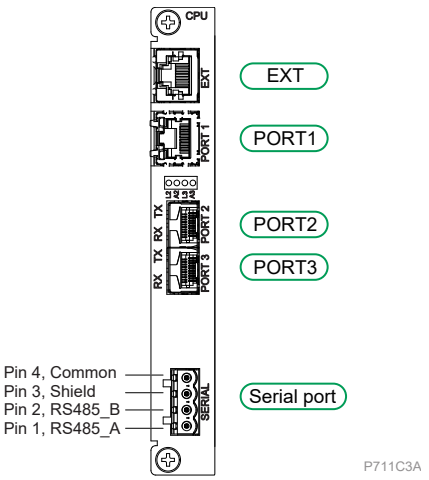
Characteristics	
	 P711AMA
Ethernet connection	100 Mbps
Protocol	Failover, RSTP, HSR or PRP
Optical wavelength	1310 nm
Fiber type	Single-mode glass fiber
Maximum attenuation (fiber optic + connectors)	14 dB (at fiber optic diameter: 9/125 µm or 10/125 µm)
Maximum range	40 km (25 mi)

Serial port: 2-wire RS485 communication port

The 2-wire RS485 communication port is located at the slot A (CPU). The RS485 connector is included in the accessory box. Install the RS485 connector on the serial port.

RS485 communication port

The PowerLogic P7 can be connected to any RS485 half duplex communication network and can exchange the data necessary for centralized management of the electrical installation by a SCADA. The serial RS485 ports are designed for wiring connections with the following characteristics for each terminal.



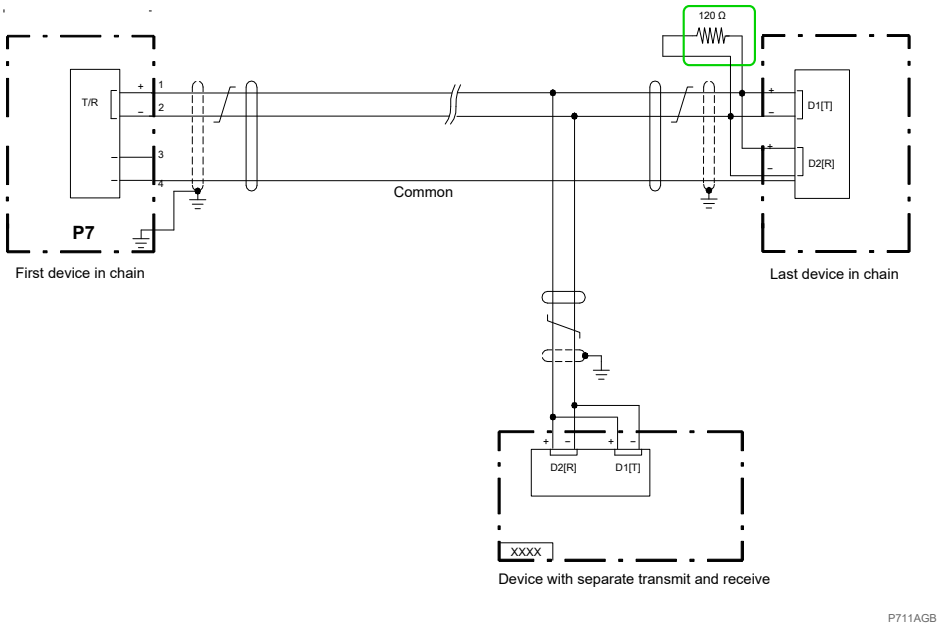
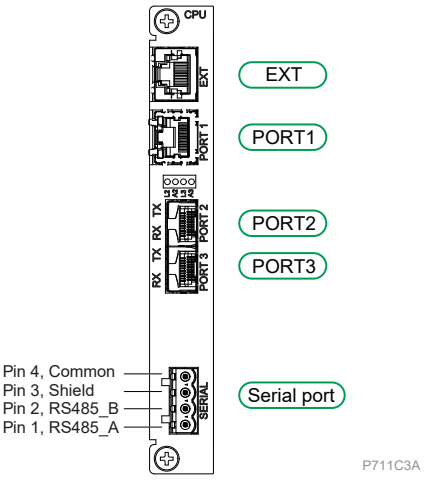


Table 13 - Characteristics of the RS485 communication port

Characteristics	
Location	Serial port in slot A
Standard	EIA 2-wires RS485 differential
Connection	Plug and socket screw connection
Communication network	Half duplex
Maximum cable length	1.2 km (4000 ft)

Extension port

The extension port is a CAN bus port located at the slot A (CPU) of the device.



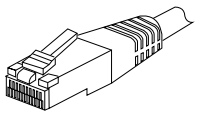
NOTICE
ETHERNET PORT DAMAGE Connect only the PowerLogic P7 accessories to the extension port. **Failure to follow these instructions can result in equipment damage.**

Connection of other equipment such as computer, switch, low power current transducer (LPCT) type sensor or other devices can result in the damage of its Ethernet port.

The extension port provides connection to the external modules. The following PowerLogic P7 accessories can be connected to the extension port:

- IRIG-B module (see IRIG-B module (reference REL51045), page 75 for more information)
- MET148-2 temperature sensor module (see MET148-2 - temperature sensor module (reference 59641) , page 73 for more information)
- CLIO module (see CLIO module (reference REL70071), page 77 for more information))

Table 14 - Characteristics of the extension port

Characteristics	
Location	Slot A
Connector	RJ45 connector 
Type of cable	The following cables (Reference numbers) can be selected for connection: • Reference 59660, length: 0.6 m (1.97 ft) • Reference 59661, length: 2 m (6.56 ft)

Accessories

MET148-2 - temperature sensor module (reference 59641)

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

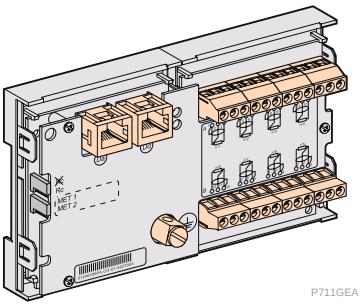
Verify that the temperature sensors are isolated from dangerous voltages.

Failure to follow these instructions will result in death or serious injury.

Description

The temperature sensor module is an external module used for temperature measurement with Resistance Temperature Detectors (RTDs). It is connected to the EXT port on the slot A (CPU). It can be selected as an accessory when ordering the device or purchased later as spare and installed on site. One temperature sensor module provides 8 RTD inputs.

Figure 42 - MET148-2 temperature sensor module



The MET148-2 module can be used to connect 8 temperature sensors (RTDs) of the same type:

- Pt100 type RTDs
- 3-wire temperature sensors
- A single module for each PowerLogic P7

Connection

Figure 43 - Connection of the MET148-2 temperature sensor module



Connectors and terminals on the module:

- A: Terminal block for RTDs 1 to 4
- B: Terminal block for RTDs 5 to 8
- Da: RJ45 connector to connect the module to the PowerLogic P7 with a 59660/59661 cord, which should not exceed 3 m (10 ft) in length.

- Dd: RJ45 connector to link up the next remote module with a 59660/59661 cord

Jumper for impedance matching with load resistor should be set to RC.

NOTE: The module is always after IRIG-B.

Jumper used to select module number, to be set to:

- MET1: 1st MET148-2 module, to measure temperatures T1 to T8 (default position)

Characteristics

Table 15 - Characteristics of the MET148-2 temperature sensor module

Characteristics	Values
Dimensions (L × W × D)	144 mm × 88 mm × 30 mm (5.67 in × 3.46 in × 1.81 in) [8]
Weight	0.2 kg (0.441 lb)
Mounting support	On symmetrical DIN rail
Operating temperature	-40°C...+70°C (-40°F...+158°F)
Temperature sensors	
Type of sensors	Pt100
Isolation from ground	None
Current to RTD	4 mA
Maximum distance between sensor and MET148-2	1 km (0.62 mi)

IRIG-B module (reference REL51045)

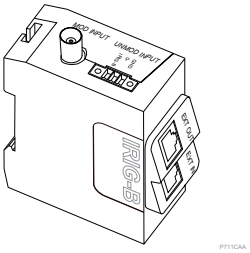
Description

The IRIG-B module is an external module used for accurate time synchronization. It is connected to the EXT port on the slot A (CPU). It can be selected as an accessory when ordering the device or purchased later as spare and installed on site.

The module provides both a modulated (MOD INPUT) and an unmodulated input (UNMOD INPUT) and can automatically detect which input type is used by the user. No configuration of input type is needed in the PowerLogic P7.

It does not require any auxiliary supply as the module gets powered over the connection interface.

Figure 44 - IRIG-B module



8. Depth is 70 mm (2.8 in) with cable connected

Connection

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

- Install the IRIG-B module between the PowerLogic P7 and any other accessories like the MET148-2 temperature module.
- Do not interface any accessories between the PowerLogic P7 and the IRIG-B module.

Failure to follow these instructions will result in death or serious injury.

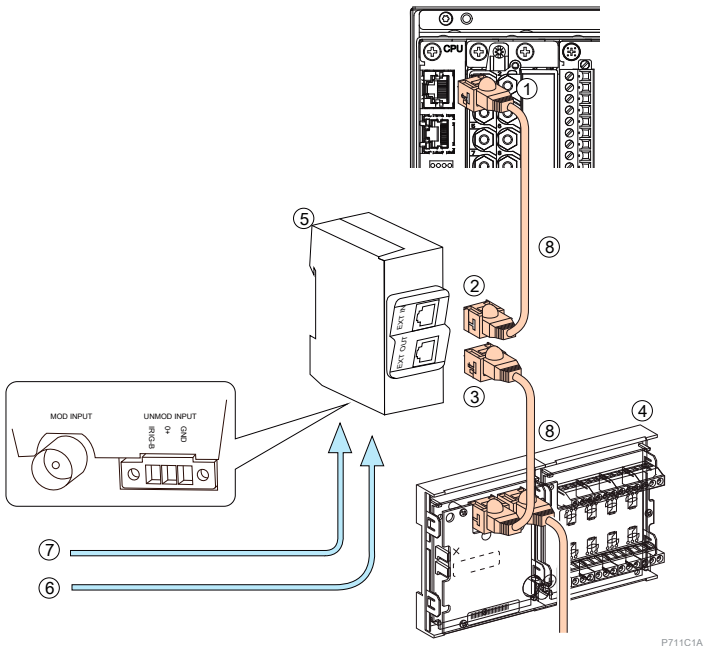
The IRIG-B module is connected to the PowerLogic P7 from its EXT IN port. The cable used for connection must be shielded and of a length not exceeding 3 m (10 ft).

The IRIG-B module provides an additional extension port (EXT OUT) for connecting other accessories such as the MET148-2 module with 59660/59661 cords.

The time source is connected to the module through the modulated input, or through the unmodulated input by connecting signal + to the IRIG-B terminal, and signal - to the 0+ terminal.

NOTE: If one source is connected on the modulated input and another one on the unmodulated input, the modulated signal has the priority.

Figure 45 - Connection of IRIG-B



① to EXT port of the PowerLogic P7

② to EXT IN port of IRIG-B

③ to EXT OUT port of IRIG-B

④ MET148-2 module

⑤ IRIG-B module

⑥ Time source to unmodulated IRIG-B input

⑦ Time source to modulated IRIG-B input

⑧ 59660/59661 cord

Characteristics

Table 16 - Characteristics of the IRIG-B module

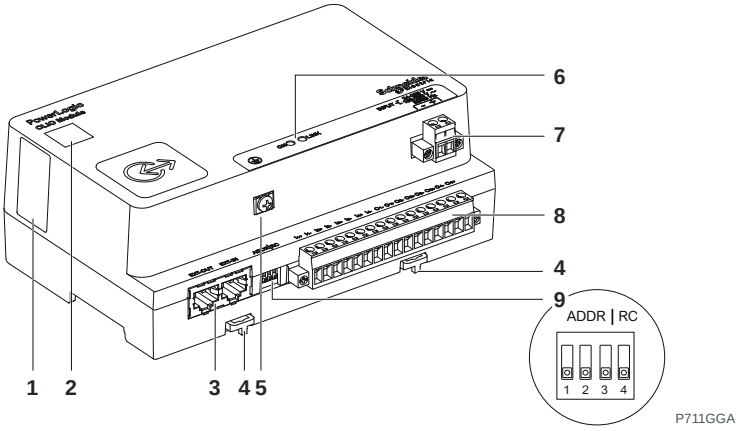
Characteristics	Values
Standard	
Standard	IRIG 200-04
Form factor	
Height	95 mm (3.7 in)
Width	36 mm (1.4 in)
Depth	87 mm (3.4 in)
Weight	100 g (0.22 lb)
Mounting support	Symmetrical DIN rail
Modulated IRIG-B input	
Connection	BNC socket
Type of cable	50 Ohm coaxial
Length of cable	< 150 m (500 ft)
Time code format	B124, B125
Input signal level	200 mV...10 V
Unmodulated IRIG-B input	
Connection	Screw-type terminals
Type of cable	Twisted pair
Length of cable	< 50 m (165 ft)
Time code format	B004, B005
Input impedance	10 kΩ
Input signal level	2...6 V peak

CLIO module (reference REL70071)

Description

The Current Loop Input/Output (CLIO) module is an external module that provides analog input and output capability for the PowerLogic P7. It can be selected as an accessory when ordering the PowerLogic P7 or purchased later as a spare and installed on site.

Figure 46 - Interface overview



1	Product label	**6**	Power LED (green) LINK LED (yellow)
2	QR code	**7**	Power supply
3	Communication port	**8**	Analog inputs/outputs
4	DIN mounting clips	**9**	DIP switches
5	Functional ground		

LED indicators

LED	Status	Description
ON	Off	Power is off.
	On	Power is on.
LINK	Off	No data received from the IED.
	On	Handshaking with the IED.
	Flashing (every 5 seconds)	Successfully handshaked with the IED.

DIP switches

The module uses the ADDR switches for configuring the address. Toggle the switches as follows to set the module address.

NOTE: If multiple CLIO modules are used on the PowerLogic P7, the address of each CLIO module must be unique.

ADDR switches positions								
Module address	000	001	010	011	100	101	110	111

The module uses the RC switch for configuring the termination of the network. Toggle the switch up if the module is the last CAN device in the loop.

RC switch position		
Termination of network	Yes	No

Connection

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

- NEVER work alone.
- Turn off all power supplying this equipment before working on or inside it.
- Verify that all power is off using a properly rated voltage sensing device.
- Connect the module to the ground with a ring terminal attached to the ground screw.
- Check the equipotential grounding network and test the grounding during installation.

Failure to follow these instructions will result in death or serious injury.

⚠DANGER

FIRE HAZARD

- Apply proper tightening torque to all wire connections.
- Never touch electronic parts.

Failure to follow these instructions will result in death or serious injury.

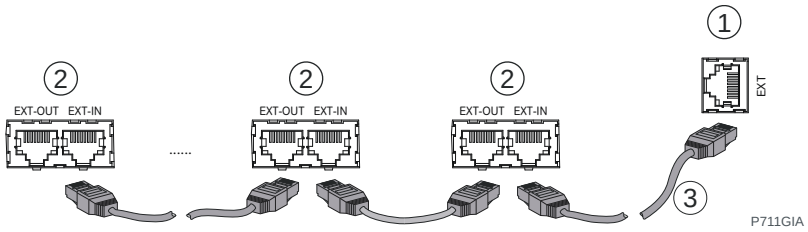
Connecting to the PowerLogic P7

Connect the CLIO module to the PowerLogic P7 from its EXT-IN communication port. The cable must be shielded twisted pair and of a length no more than 3 m (10 ft).

Recommended connection cord:

- 59660: CCA770 remote module connection cord, L = 0.6 m (2 ft)
- 59661: CCA772 remote module connection cord, L = 2 m (6.6 ft)

Figure 47 - Connection example of the CLIO module



① PowerLogic P7

② CLIO module

③ Connection cord

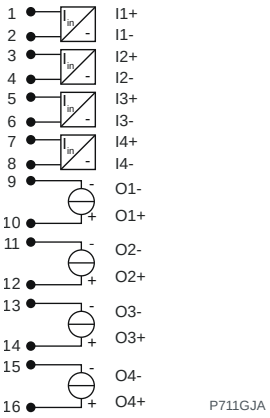
NOTE:

1. For the last CLIO module in the loop, toggle the RC switch down to set the module as termination of network.
2. When the MET148-2 module and the CLIO module are connected to the PowerLogic P7 by daisy chaining, a maximum of one MET148-2 module and one CLIO module can be connected. The address for the MET148-2 module is *MET1* and the address for the CLIO module is *000*. If the last module in the loop is disconnected from the PowerLogic P7, the communication does not rebuild automatically when the physical connection is returned. To rebuild the communication, unplug and plug the CAN cable on the EXT port of the PowerLogic P7.

Connecting the analog inputs and outputs

Each CLIO module provides four current loop input channels and four current loop output channels.

Figure 48 - Terminal diagram



Refer to Wiring specification, page 64 for detailed information on wiring the screw-type terminals.

Connecting to the power supply

Connect the module to an external power supply (24...250 V DC, 100...250 V AC).

Refer to Wiring specification, page 64 for detailed information on wiring the screw-type terminals.

Connecting the functional ground

Connect the module to the ground with a ring lug terminal attached to the ground screw. Use cable with cross-section of 2.5...6 mm² (*AWG 12...10*) and fitted with a 4 mm *(0.16 in)* ring lug at the cable end. The maximum cable length is 2 m (*6.5 ft.*). Tighten the ground screw with tightening torque of 1...1.2 N·m (*8.85...10.62 lb-in*).

Characteristics

Table 17 - Characteristics of the CLIO module

Characteristics	Values
Dimensions (L × W × H)	172 × 108 × 63 mm (6.8 × 4.3 × 2.5 in)
Mounting support	Symmetrical DIN rail
Operating temperature	-40...+70 °C (-40...+158 °F)
Power supply	24...250 V DC, 100...250 V AC 50 Hz or 60 Hz

Commissioning

Principles

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

- NEVER work alone.
- Only qualified personnel can commission this equipment. Such work must be performed only after reading this entire set of instructions.
- Obey all existing safety instructions when commissioning and maintaining high-voltage equipment.
- Apply appropriate personal protective equipment (PPE) and follow safe electrical work practices.
- Do not choose lower PPE while working on energized equipment.
- Beware of potential hazardous voltages from open circuited current transformers, any voltage transformers and any capacitors.
- Before energizing verify that the protection device and other devices are connected to a protective ground in accordance with the instructions provided.

Failure to follow these instructions will result in death or serious injury.

NOTE: See NFPA 70E, CSA Z462 or national equivalent.

⚠DANGER

FIRE HAZARD

Apply proper tightening torque to all wire connections.

Failure to follow these instructions will result in death or serious injury.

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

- Never open the secondary circuit of a live CT.
- The secondary of the line CT must be shorted before opening any connections to it.

Failure to follow these instructions will result in death or serious injury.

⚠WARNING

UNINTENDED EQUIPMENT OPERATION

Do not energize the primary circuit before the protection device is properly configured.

Failure to follow these instructions can result in death, serious injury, or equipment damage.

PowerLogic P7 devices are tested prior to commissioning, with the aim of maximizing availability and minimizing the risk of malfunctioning of the device and all connected accessories.

PowerLogic P7 devices are fully numerical in their design and implementation of the protection functions and non-protection functions in the firmware. The devices use a high degree of self-checking and give an alarm. Therefore, the

commissioning tests do not need to be as extensive as with non-numeric electronic or electro-mechanical relays.

To commission PowerLogic P7 devices, it is necessary to verify that the hardware is functioning correctly and the application function settings have been applied as expected. To confirm that the device is operating correctly once the settings have been applied, it is necessary to perform basic functional tests on each active protection element one by one.

The main tasks for the commissioning test are as follows:

- Device check
- Secondary injection test
- Primary injection test (Optional)
- Final check

Testing tools and equipment

The following tools and equipment are needed for the commissioning:

- AC current and voltage injection sources
  - For secondary injection test, on conventional CTs and VTs, to check the device functions, the injection source should be at such a rating that the current is adjustable up to at least 5 Inom (Inom = 1 A or 5 A) and the voltage is adjustable up to at least 110 V.
  - If the primary injection test is necessary to check the CT and VT primary connection and polarity, the injection source should be at such a rating that the minimum current at the CT secondary is larger than 20 mA (2% of the nominal current) and the minimum voltage at the secondary is larger than 750 mV (1% of the nominal voltage).
- DC voltage source

  Adjustable from 24 to 250 V DC, for adaptation to the voltage level of the logic input being used and tested.
- Multimeters
  - With suitable AC current range, and AC/DC voltage ranges
  - Phase angle meter
- A portable PC with the PowerLogic Engineering Suite installed
- USB cable with mini-USB type B interface or RJ45 Ethernet cable
- For CT/VT, test block and test plug for secondary injection testing
  - Plug with cord to match the current test block installed
  - Plug with cord to match the voltage test block installed

Device check

Checking with the device de-energized

The following group of tests should be carried out without the auxiliary power supply applied to the PowerLogic P7 and with the trip circuit isolated. The current and voltage transformer connections must be isolated from the device for these checks. It is suggested to apply the test block to isolate the primary system, as shown in Typical test block connection diagram , page 83.

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

- Never open-circuit the secondary circuit of a current transformer.
- Before the test plug is inserted into the test block, make sure the sockets in the test plug which correspond to the current transformer secondary windings are linked.

Failure to follow these instructions will result in death or serious injury.

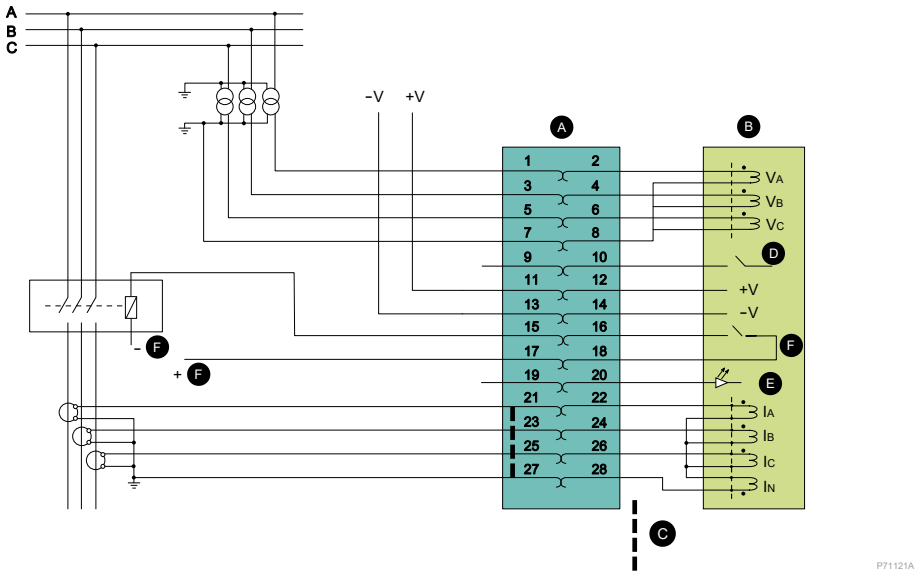
⚠⚠WARNING

HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

- Do not remove the CT/VT IP20 transparent cover during testing.
- After commissioning, verify that the CT/VT IP20 transparent cover is properly fitted and secured with the screw.

Failure to follow these instructions can result in death, serious injury, or equipment damage.

Figure 49 - Typical test block connection diagram



A	Test block	B	PowerLogic P7
C	Shorting bar	D	Output
E	Input	F	Trip

Before inserting the test plug, refer to the scheme diagram. For example, the test block may be associated with protection current transformer circuits. If the PowerLogic P7 is installed in the switchgear, the test block is not always provided. In the application case without a test block, it is mandatory to isolate the voltage transformer supply to the PowerLogic P7 using the panel links or connecting blocks, and to short-circuit them on substation side and disconnect the line current transformers from the device terminals. Where means of isolating the auxiliary power supply and trip circuit (such as isolation links, fuses and MCB) are provided, these should be used. If this is impossible, the wiring to these circuits must be disconnected and the exposed ends suitably terminated.

Visual inspection

The visual inspection should include the following aspects:

- Check the rating information on the PowerLogic P7.
- Check that the PowerLogic P7 being tested is correct for the protected objective.
- Check that the circuit reference and system details are entered onto the setting record sheet.
- Carefully examine the PowerLogic P7 to see that no physical damage has occurred since installation.
- Check that the case grounding connections, at the rear of the protection and control device case, are used to connect the protection and control device to a local ground bar using an adequate conductor (see Connecting ground, page 65).

External wiring

- Check that the external wiring is correct to the relevant device diagram and wiring scheme. Check that the phase rotation appears as expected.
- Check the connections against the wiring diagram if a test block is provided.

Auxiliary power supply

The PowerLogic P7 can be operated from either a DC or AC auxiliary power supply. Without energizing the device, measure the auxiliary power supply to help ensure it is within the operating range.

The rated voltage is:

- 24...34 V DC
- 48...125 V DC
- 110...250 V DC/AC

The incoming voltage must be within the operating range specified as:

- 19.2...41 V DC
- 38.4...150 V DC
- 88...300 V DC/ 80.3...288 V AC

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION, OR ARC FLASH

The power supply must be turned off for at least 5 seconds before power supply module is removed.

Failure to follow these instructions will result in death or serious injury.

NOTICE

POWER SUPPLY DAMAGE

Make sure that the nominal value of the auxiliary device voltage corresponds with the nominal value of the auxiliary system voltage before connecting the auxiliary voltage to the PowerLogic P7.

Failure to follow these instructions can result in equipment damage.

Watchdog

Using a continuity tester, check that the watchdog contacts (WD of slot Z) are in the states shown in the connection diagram for a de-energized device.

Testing with the device energized

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

Before performing hardware and software tests:

- Isolate the current and voltage transformer connections from the protection device.
- Isolate the trip circuit.

Failure to follow these instructions will result in death or serious injury.

The following group of tests verify that the PowerLogic P7 hardware and software is functioning correctly and should be carried out with the auxiliary power supply applied to the device.

Table 18 - Checklist of hardware and software

Hardware checklist	Software checklist
1. Energizing the device, page 85 2. Watchdog, page 85 3. Binary inputs, page 85 4. Binary outputs , page 86 5. Communication ports, page 87	1. Model number and firmware version, page 86 2. Date and time, page 86 3. Slot health, page 86 4. Communication ports, page 87

NOTE: For PowerLogic P7 with no HMI, use the PowerLogic Engineering Suite to check the device status and read measurements. Refer to Using the PowerLogic Engineering Suite, page 131 for more information.

Energizing the device

- Switch on the auxiliary power supply.
- Check that the PowerLogic P7 performs the following initialization sequence:
  1. All four fixed LEDs are illuminated. The boot screen displays and the device self-test is ongoing.
  2. When the initialization of the PowerLogic P7 is complete, LED ⏻ is on. The default screen is displayed.

NOTE: Only when this operation is successfully completed will the LED turn off and the default screen (Function Key description, Single Line Diagram of one bay and Frequency bar) is displayed.

Watchdog

Use a continuity tester to verify that the Watchdog contact is linked to the successful start-up of the relay.

Binary inputs

This test verifies that all binary inputs (opto-isolated) of the PowerLogic P7 are functioning correctly. Check the terminal configuration schemes in PowerLogic P7 rear panel, page 46 for terminal numbers. Check the polarity and connect the external 24V DC/48V DC/110V DC/220V DC/220V AC supply voltage to the appropriate terminals for the input being tested, see Configuring binary inputs (LPDI), page 144 for settable voltage values. Energize the opto-isolated input one by one.

NOTE: The external power supply is used for this test, but only after confirming that it is suitably rated, with the variation less than 20%.

The status of each opto-isolated input can be viewed from the HMI under ☰ > **General > Device config > Slot # > BI status**. # refers to the code of the slot (for example, slot G). The status of each BI should be true.

Binary outputs

This test checks that all the output contact relays are functioning correctly using the Test mode.

Connect a continuity tester across the terminals corresponding to output relay as shown in the relevant terminal configuration schemes in PowerLogic P7 rear panel, page 46.

To operate the output relay BO1 in Slot Y:

1. From the HMI, expand ☰ > **Control > Device mode** and select **Test** from the **Device mode** drop-down to set the physical device (LD0) to *Test* mode
2. Expand ☰ > **General > Device config > Slot Y+Z** and select the **BO status** tab to force the individual relays.

Repeat the test for the rest of the output relays, and then return the PowerLogic P7 to service by setting the IED mode back to *Normal*.

NOTE:

- Ensure that the thermal ratings of anything connected to the output relays during the contact test procedure are not exceeded by the over-operated output contact relays. Keep the time between application and removal of contact test to a minimum.
- Slot Z contacts DO7 and DO8 are controlled by the TIO module in slot Y.

Model number and firmware version

To view the model number and the firmware version:

1. From the HMI, expand ☰ > **General > System info > Device info**.
2. Check the **Product code** and **Firmware version** information displayed.

Slot health

If the 🔧 LED is on, it indicates a problem with the device firmware or hardware. The hardware health can be checked from the HMI under ☰ > **General > Device config > Slot # > Slot info**.

Six health statuses are defined for each slot as follows. Ensure that the health status shows OK; otherwise, perform troubleshooting until the health status is OK.

- Not fitted
- Mismatch
- Absent
- OK
- Warning
- Alarm

NOTE: If all board health statuses are *OK* or *Not fitted*, and the 🔧 LED is on, check the device firmware under ☰ > **General > Device config > Slot A > Version info > Firmware info**.

Date and time

The date and time can be synchronized with three different external clock sources, PTP (IEEE 1588), IRIG-B or SNTP. The clock can also be set from the HMI under

> General > System clock > Date and time if not synchronized to an external time source. See Configuring time synchronization, page 139.

Communication ports

The PowerLogic P7 supports both serial and Ethernet communication simultaneously.

One of the two protocols can be selected and used to communicate through the serial port.

- DNP3
- Modbus server

If one of these protocols is configured, the PowerLogic P7 can exchange data with protocol client (master). If serial communications is enabled in both protocols, only Modbus server will be active and DNP3 serial communications will be disabled. The serial port parameters, for example, **baud rate**, **parity** can be selected.

There are three protocols that can be selected and used to communicate through the Ethernet ports.

- IEC 61850
- DNP3
- Modbus server

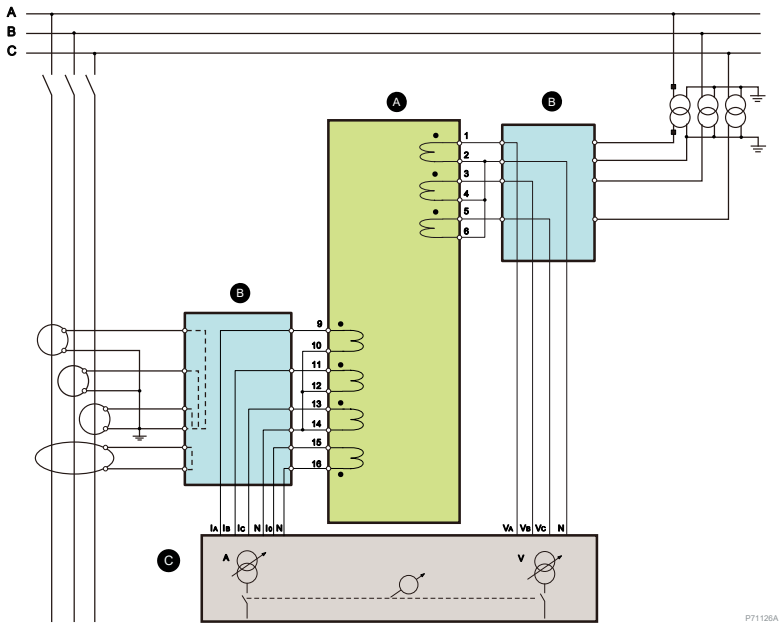
All can be selected at the same time, and for each protocol IP address needs to be selected to communicate with clients.

Secondary injection test

The secondary injection test is to check the device analog input signal processing and basic protection functions is working with the application-specific settings.

In the application case with test block, the connection diagram and the test plug mounted is illustrated in the Typical secondary injection test connection diagram with test block, page 87.

Figure 50 - Typical secondary injection test connection diagram with test block



A	PowerLogic P7 analog module	B	Test block + Test plug
C	Three phase relay test set		

In the application case without test block, it is mandatory to isolate the CT and VT supplies. The CT must be shorted before isolating normally with test links. The VT fuses are removed or the MCB opened. The relay side connection should be tested to ensure it is dead before proceeding. The trip circuit and intertrips (e.g. CBF) are isolated to avoid an unintentional circuit breaker trip during the secondary injection test. The secondary injection test can be performed by injecting the current and voltage into the related analog connection terminals.

Applying application-specific settings

There are different methods of applying the settings:

- PowerLogic Engineering Suite

  Use the PowerLogic Engineering Suite when setting the relay for the first time. It is preferred to use the Engineering Suite for configuring the settings, especially when specific logic (not the default logic) or many specific settings are to be applied, as it is much faster and allows less margin for error.

- Front panel

  The front panel of the PowerLogic P7 can also be used to configure the settings, when limited specific settings are to be applied.

  NOTE: If the application-specific settings are not available, the secondary injection test can be performed based on the default settings.

During testing it may be necessary to disable some protection functions. After the completion of the injection tests, all the protection functions applied must be enabled during the final check stage.

Current inputs

This test verifies that the accuracy of current measurement is within acceptable tolerances.

The PowerLogic P7 has three phase current inputs and single phase current inputs. Multiple instances of each type can be added to bays. The source for each input and type can be configured within the CT setup.

- Double check the connection and then start the injection test.
- Apply current equal to the related CT secondary rated current.
- Check its magnitude using a multimeter or reading from the test equipment.
- Check the current magnitude displayed on the front panel of the PowerLogic P7.
- Calculate the current measurement accuracy, it shall be within ±1% at rated current.

Voltage inputs

This test verifies that the accuracy of voltage measurement is within the acceptable tolerances.

The PowerLogic P7 has three-phase voltage inputs and single phase voltage inputs. Multiple instances of each type can be added to bays. The source for each input and type can be configured within the VT setup.

The following tests will be realized with the VT Connecting Mode set to *3ph* which is the most used configuration. Refer to Connection type, page 342 for more details.

- Double check the connection and then start the injection test.
- Apply voltage equal to the related VT secondary rated voltage.
- Check its magnitude using a multimeter or reading from the test equipment.
- Check the voltage magnitude on the front panel of the PowerLogic P7.
- Calculate the voltage measurement accuracy, it is within ±1% at rated voltage.

Binary input and binary output wiring and operation check

For binary input wiring and check, see Binary input wiring and operation check.

For binary output wiring and check, see Binary output wiring and operation check.

Checking the protection functions

The tests described in Device check, page 82, Current inputs, page 88, and Voltage inputs, page 88 have already demonstrated that the device inputs and outputs work correctly and the analog inputs are within calibration, thus the purpose of the tests for protection functions is as follows:

- To determine that each active protection function of the device can trip according to the correct application settings.
- To verify correct assignment of the trip and alarm contacts by monitoring the response to the related fault injection.

The following sections only present the test procedures for current protection and voltage protection. The basic test procedures are similar to the other protection functions. For the list of settings which are used for various current and voltage protection including the default values, see Protection functions, page 156.

Current protection

This test, performed on stage 1 of the overcurrent protection function in setting group 1, is to check that the protection and control device is operating correctly at the application-specific settings.

1. Determine which output relay has been selected to operate when an overcurrent protection trip occurs.
2. Connect the output relay so that its operation will trip the test set and stop the timer of relay test set.
3. Connect the current outputs of the test set to the protection and control device current input terminals.
4. Apply a current of 120% of the current setting to the protection and control device and it will trip according to the operation time setting.
5. Check the tripping time from the test set and compare with the operation time setting.
6. Check the related fault recorder, events, and the related LEDs for trip indications.

A similar test procedure can be applied for the secondary injection test to check the other protection functions with the application-specific settings.

Voltage protection

This test, performed on stage 1 of the under-voltage protection function in setting group 1, is to check that the protection and control device is operating correctly at the application-specific settings.

1. Determine which output relay has been selected to operate when an under-voltage protection trip occurs.
2. Connect the output relay so that its operation will trip the test set and stop the timer.
3. Connect the voltage outputs of the test set to the protection and control device voltage input terminals.
4. Apply nominal voltage first and then a voltage of 80% of the voltage setting to the protection and control device. It will trip according to the operation time setting.
5. Check the tripping time from the test set and compare with the operation time setting.
6. Check the related fault recorder, events, and the related LEDs for trip indications.

A similar test procedure can be applied for the secondary injection test to check the other protection functions with the application-specific settings.

Bay dead check

This test is to check if the bay dead function is operating correctly with the configured matrix. The bay dead function is applied to give an indication if all phases of the line are dead. Its condition is determined by monitoring the status of the BayLive input and by measuring the phase currents and voltages.

More information about bay dead, refer to Description, page 445 and Block diagram, page 446 section of bay dead function.

1. In PowerLogic Engineering Suite, check the CB status is mapped to the BayLive input via the Matrix.
2. Force the CB position to open status.
3. With zero current and nominal voltage applied, check the bay dead is true.
4. Force the CB closed status and check bay dead is false.
5. Force the CB open status and check the bay dead is true.
6. Inject nominal voltage and current and check the BayDead is false.

Primary injection test (optional)

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

- Only qualified electrical engineers can perform the primary injection test.
- Strictly follow the related primary injection testing instructions from the utility.

Failure to follow these instructions will result in death or serious injury.

Primary injection testing is recommended to:

- confirm the external wiring to the current and voltage inputs is correct,
- check the polarity of the current transformers at each end is consistent,
- check the directionality of the directional elements.

For the directional overcurrent or ground fault protection, distant protection or current differential protection applications, it is mandatory to check the correct polarity of the current transformers. If the current or voltage positive or negative sequence components are applied in the protection functions, it is mandatory to ensure the correct phase sequence of current or voltage inputs.

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

Verify that all connections are restored according to the external connection or scheme diagram after disconnecting any of the external wiring from the protection device for any tests.

Failure to follow these instructions will result in death or serious injury.

For primary injection testing on conventional CT's, it is necessary to calculate the current and voltage magnitudes to be injected in the primary side according to the actual application scenario, check that the current magnitude is more than 20 mA and the voltage magnitude is more than 100 mV on the secondary side. Normally the mains power supply in the substation or power plant can be applied for primary injection tests.

Voltage connections

NOTICE

CIRCUIT OVERLOAD

Measure the voltage transformer secondary voltages using a multimeter to ensure that they are compliant with the PowerLogic P7's input ratings.

Failure to follow these instructions can result in equipment damage.

Primary voltage injection:

- Check ratio is correctly configured.
- Check the polarity is correctly connected.
- Check that the system phase rotation is correct using a phase rotation meter.
- Inject the voltage into the voltage transformer primary connection terminals.
- Check that the voltage magnitudes and angles are displayed on the HMI of the protection and control device in primary values.
- The voltage magnitudes should be equal to the applied voltage.
- The voltage angles should be correct according to the phase sequence.

Thus, the VT ratio, polarity, phase sequence and the external wiring from the primary system to the protection and control device can be verified by the primary voltage injection.

Current connections

NOTICE

CIRCUIT OVERLOAD

Measure the current transformer secondary values for each input using a multimeter connected in series with corresponding protection device current input.

Failure to follow these instructions can result in equipment damage.

Primary current injection:

- Check ratio is correctly configured.
- Check the polarity is correctly connected.
- Inject current into the primary system through the phase under test.

- Check that the current magnitudes and angles are displayed on the HMI of the protection and control device in primary values.
- The current magnitudes should be equal to the applied current.
- The current angles should be correct according to the phase sequence.
- Check that the current transformer polarities are correct against a phase meter already installed on site and known to be correct by measuring the phase angle between the current and voltage, or by contacting the system control center for the direction of power flow.

When using a residual current transformer (core balance) or a sensitive current transformer, inject a single phase to validate the functionality.

Therefore, the CT ratio, polarity, phase sequence and the external wiring from the primary system to the protection and control device can be verified by primary current injection.

Demonstrating circuit breaker operation

The correct operation of the circuit breaker shall be verified sufficiently during the commissioning test. CB operation can be controlled by the local or remote-control commands.

CB operation test:

- Check the actual CB position, read the current value and the CB position status from the HMI of the device if the related CB position (52a, 52b) has been connected to the protection and control device opto-isolated inputs. When CB position is open (52b), there will be no current. When CB position is closed (52a), there will be current.
- Perform a local CB control command to trip and close the CB, the CB shall operate correctly per the control command. See Controlling objects, page 142 for how to control CB.
- Read the CB position status from the HMI of the protection and control device after one control command, the CB position information shall be the same as the actual CB status.

Final check

⚠CAUTION

UNINTENDED EQUIPMENT OPERATION

At the end of the commissioning, verify that no device remains in test mode.

Failure to follow these instructions can result in injury or equipment damage.

NOTICE

CIRCUIT OVERLOAD

- Remove all test or temporary shorting leads.
- Verify that all connections are restored according to the relevant external connection or scheme diagram after disconnecting any of the external wiring from the protection device for any wiring verification tests.

Failure to follow these instructions can result in equipment damage.

The commissioning is now complete, but before putting the PowerLogic P7 into normal operation, check the following items:

- Ensure that the PowerLogic P7 is restored to service.

- CB maintenance and current counters should be set as required. These counters can be reset.
- Double check the application-specific settings, to ensure that all the desired protection and control functions are enabled with the correct settings. Extract the final setting file from the PowerLogic P7.
- Check the Date and Time of the PowerLogic P7, to ensure the date and time are synchronized or set manually when no time synchronization is used.
- Clear all event records, fault records, and disturbance records. Make sure that alarms and LEDs have been reset.

The device is now ready for operation.

Cybersecurity

Cybersecurity overview

This chapter contains up-to-date information about your product's cybersecurity. Network administrators, system integrators and personnel that commission, maintain or dispose of a device should:

- Apply and maintain the device's security capabilities. See Device security capabilities, page 96 for details.
- Review assumptions about protected environments. See Protected environment assumptions, page 99 for details.
- Address potential risks and mitigation strategies. See Potential risks and compensating controls, page 99 for details.
- Follow recommendations to optimize cybersecurity.

⚠WARNING

POTENTIAL COMPROMISE OF SYSTEM AVAILABILITY, INTEGRITY, AND CONFIDENTIALITY

- Change default passwords to help prevent unauthorized access to device settings and information.
- Disable unused ports/services and default accounts, where possible, to minimize pathways for malicious attacks.
- Place networked devices behind multiple layers of cyber defenses (such as firewalls, network segmentation, and network intrusion detection and protection).
- Use cybersecurity best practices (for example: least rights, separation of duties) to help prevent unauthorized exposure, loss, modification of data and logs, interruption of services, or unintended operation.

Failure to follow these instructions can result in death, serious injury, or equipment damage.

Security policy

NOTICE

LOSS OF ACCESS

- Setup a security policy and procedure to back up the security administrator user account.
- Do not share a single user account with multiple users. Set one user account associated to roles and rights per user.
- Do not excessively decrease values of user parameters.

Failure to follow these instructions can result in loss of access to the protection device.

Cybersecurity helps provide:

- Confidentiality (to help prevent unauthorized access).
- Integrity (to help prevent unauthorized modification).
- Availability/authentication (preventing the denial of service and assuring authorized access).
- Non-repudiation (preventing the denial of an action that took place).
- Traceability/detection (logging and monitoring).

For an efficient security, the instructions and procedures should structure the roles and responsibilities in terms of security within the organization; in other words, who is authorized to perform what and when. These should be known by the users.

The anti-intrusion and anti-physical access to any sensitive installation should be set up.

All the security rules implemented in the PowerLogic P7 are in complement of the points above.

The PowerLogic P7 is delivered with auto-login via the local control panel with the default ENGINEER role. The auto-login function can be configured with the parameter **Local Default Access** using CAE.

In the PowerLogic P7, the control of accessibility to the settings, parameters, configuration and logs is done with a user authentication after **Log in**, with a name and password.

The PowerLogic P7 controls the access:

- through the front panel
- through the PowerLogic Engineering Suite (front and rear connection)

The Ethernet communication with the PowerLogic Engineering Suite is encrypted.

The access through the communication protocols is not controlled by the PowerLogic P7 but by the SCADA system. The protocols does not include any specific secured commands.

NOTICE

POTENTIAL COMPROMISE TO CYBERSECURITY

- For transmitting data over an internal network, physically or logically segment the network. Restrict the access to the internal network by using standard controls, such as firewalls, and other relevant features supported by your device, such as IP Table allowlist.
- For transmitting data over an external network, encrypt protocol transmissions over all external connections using an encrypted tunnel, TLS wrapper or a similar solution.

Failure to follow these instructions can increase the risk of unauthorized access.

The access through the binary inputs is not controlled.

Any SCADA system, and any computer using the PowerLogic Engineering Suite, CAE software and central server as well, should have an updated anti-virus, anti-malware, anti-ransomware application activated during the use. On customer side, firewalls and proxies are set up to authorize communication.

If a central server is used, a backup is recommended.

A password policy should be implemented with:

- Change of the default passwords before the PowerLogic P7 is put into operation (see Password complexity, page 121).
- Periodic change of the passwords.
- Revocation of the passwords of users who leave or do not need to use the device any more.

Product defense-in-depth

Use a layered network approach with multiple security and defense controls in your IT and control system to minimize data protection gaps, reduce single-points-of-failure and create a strong cybersecurity posture. The more layers of security in your network, the harder it is to breach defenses, take digital assets or cause

disruption. An overview of the security layers implemented by PowerLogic P7 is shown below.

ID	Layer name	Responsibilities to each layer of defense
L1	Layer 01: System hardening	Typical application usage within system context • Security zone, with a dual system implementation where essential and non-essential functions are separated and allocated different priority levels and computational resources
L2	Layer 02: Operating system hardening	OS Hardening • User account restriction • Disabling unused services (protocols, ports, …)
L3	Layer 03: Firmware integrity	Firmware package • Executable and libraries are signed using Schneider Electric trusted certificate
L4	Layer 04: Firmware Hardening	Files and folders permission • Binary application folders with limited access permission • User's data folder limiter with restricted access permission • Firmware upgrade for vulnerability fixing
L5	Layer 05: Application Hardening	Application Hardening • Client IP allowlist and firewall • RBAC management • Encryption • Network segmentation • Concurrent communication session limit

NOTE:

- Each layer provides additional defense mechanisms.
- Secure design principles are applied to each layer as each layer may be compromised.
- The objective is to reduce the attack surface of the subsequent layers.

Device security capabilities

This section describes the security capabilities available with your device.

Information confidentiality and integrity

These security capabilities help protect the confidentiality of information through secure protocols that employ cryptographic algorithms, key sizes and mechanisms used to help prevent unauthorized users from reading information in transit.

The PowerLogic P7 protects the integrity of the public key used for firmware authenticity check with One Time Password (OTP) so that it cannot be tampered with.

The PowerLogic P7 protects the confidentiality of user password and symmetric keys at rest by saving only the HASH value instead of the clear text. For the user password in transit, the PowerLogic P7 protects the confidentiality by transmitting them over HTTPs and Lightweight Directory Access Protocol (LDAP)s.

The PowerLogic P7 generates the private keys uniquely for each device to limit the scope of exploitation to that very device once compromised.

The PowerLogic P7 follows the internationally recognized recommendation for implementing cryptographic security mechanisms. In the meantime, the design teams constantly review and test the product to identify and fix any vulnerable ones.

Physical security

In order to help prevent unauthorized access, lock the USB cover on the front panel of the PowerLogic P7 with a wired lead seal. See USB ports, page 126 for details.

After flush mounting the device, the screws on the device can only be reached from the inside of the panel. See Flush mounting, page 41 for details.

The Joint Test Action Group (JTAG) debugging interfaces of CPU and Field Programmable Gate Array (FPGA) components are not soldered on manufactured devices.

Cybersecurity configuration

These security capabilities support the analysis of security events, help protect the device from unauthorized alteration and records configuration changes and user account events:

- Internal time synchronization.
- Time source integrity protection and the PowerLogic P7 configuration event logging.
- Timestamps, including date and time, match the PowerLogic P7 clock.
- Device files such as disturbance records, configuration files, log and trace files are stored in Flash Memory of the PowerLogic P7 and can be extracted over HTTPS.
- Embed user information with changes.
- Offload information to syslog or a protected storage or retention location.

User accounts and rights

These security capabilities help enforce authorizations assigned to users, segregation of duties and least rights:

- User authentication is used to identify and authenticate software processes and devices managing accounts.
- User account lockouts configurable with number of unsuccessful login attempts.
- Password strength feedback using CAE.

Port hardening

The communication ports of the PowerLogic P7 can be disabled from the PowerLogic Engineering Suite. Each logical port can be independently disabled. For more information, refer to Port hardening, page 122.

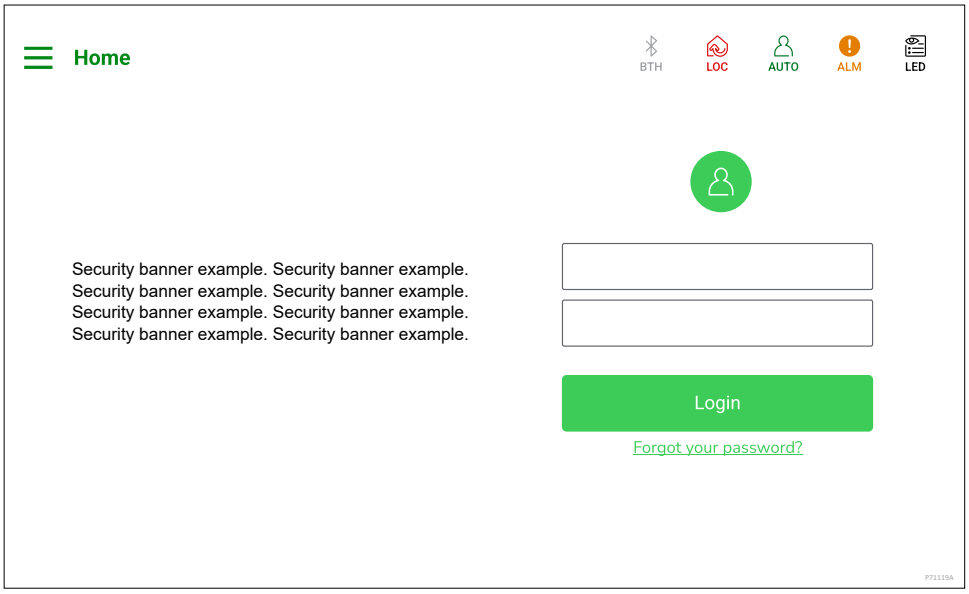
Security banner

Security banner is supported on the PowerLogic P7. For how to configure the security banner, refer to the *Security Banners* section of the CAE user manual.

> **NOTE:** Among the three configurable security banners on CAE, only *Security banner large* is supported on the PowerLogic P7.

When successfully configured, the security banner appears on the user login page of HMI like below. If left unconfigured, no security banner is displayed.

Figure 51 - Security banner on HMI



Security firmware upgrades

This security capability helps protect the authenticity of the firmware running on the PowerLogic P7 and facilitates protected file transfer: digitally signed firmware is used to help protect the authenticity of the firmware running on the device and only allows firmware generated and signed by Schneider Electric.

Device backup creation and restore

This security capability helps the PowerLogic P7 participate in system level backup operations by creating backups of the device state. In case of need, device can recover with help of the backups to a known good operational state. The protection, control and communication settings can be saved with the PowerLogic Engineering Suite; the security configuration can be saved with CAE.

For how to create such backups and to use them to restore device, refer to CAE User Manual and PowerLogic Engineering Suite User Manual.

NOTE: The created backup files must not be modified in any way. Otherwise they can't pass validity check by the PowerLogic Engineering Suite and the restoration fails.

Security event logging

These security capabilities help provide a method to generate security-related reports and manage event log storage:

- Machine and human-readable reporting options for current device security settings.
- Audit event logs to identify:
  - The PowerLogic P7 configuration changes.
  - Energy management system events.
- Audit storage capacity of 3 event files with maximum 256 KB of each file and alternate methods for log management.

Protected environment assumptions

- Cybersecurity governance – available and up-to-date guidance on governing the use of information and technology assets in your company.
- Perimeter security – installed devices, and devices that are not in service, are in an access-controlled or monitored location.
- Emergency power – the control system provides the capability to switch to and from an emergency power supply without affecting the existing security state or a documented degraded mode.
- Firmware upgrades – the PowerLogic P7 upgrades are implemented consistently to the current version of firmware.
- Controls against malware – detection, prevention and recovery controls to help protect against malware are implemented and combined with appropriate user awareness.
- Physical network segmentation – the control system provides the capability to:
  - Physically segment control system networks from non-control system networks.
  - Physically segment critical control system networks from non-critical control system networks.
- Logical isolation of critical networks – the control system provides the capability to logically and physically isolate critical control system networks from non-critical control system networks. For example, using VLANs.
- Independence from non-control system networks – the control system provides network services to control system networks, critical or non-critical, without a connection to non-control system networks.
- Encrypt protocol transmissions over all external connections using an encrypted tunnel, TLS wrapper or a similar solution.
- Zone boundary protection – the control system provides the capability to:
  - Manage connections through managed interfaces consisting of appropriate boundary protection devices, such as: proxies, gateways, routers, firewalls and encrypted tunnels.
  - Use an effective architecture, for example, firewalls protecting application gateways residing in a Demilitarized Zone.
  - Control system boundary protections at any designated alternate processing sites should provide the same levels of protection as that of the primary site, for example, data centers.
- No public internet connectivity – access from the control system to the internet is not recommended. If a remote site connection is needed, for example, encrypt protocol transmissions.
- Resource availability and redundancy – ability to break the connections between different network segments or use duplicate devices in response to an incident.
- Manage communication loads – the control system provides the capability to manage communication loads to mitigate the effects of information flooding types of DoS (Denial of Service) events.
- Control system backup – available and up-to-date backups for recovery from a control system failure.

Potential risks and compensating controls

Address potential risks using these compensating controls:

Area	Issue	Risk	Compensating controls
User accounts	Default account settings are often the source of unauthorized access by malicious users.	If you do not change the default password, unauthorized access can occur.	Change the default password for all accounts to help reduce unauthorized access. See Passwords, page 121.
Secure protocols	IEC 61850, DNP3 over Ethernet, Modbus server over Ethernet, DNP3 serial and Modbus server serial protocols are insecure. The device does not have the capability to transmit data encrypted using these protocols.	If a malicious user gained access to your network, they could intercept communications.	For transmitting data over an internal network, physically or logically segment the network. For transmitting data over an external network, encrypt protocol transmissions over all external connections using an encrypted tunnel, TLS wrapper or a similar solution. See Protected environment assumptions, page 99.

Cybersecurity configuration

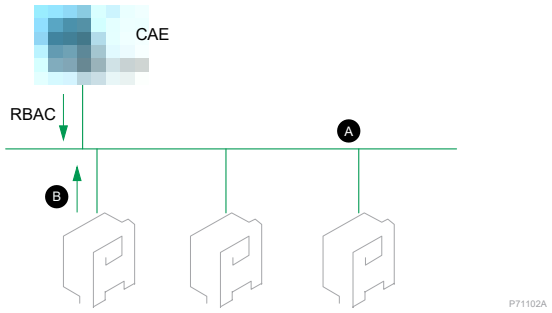
All PowerLogic P7 security rules are managed with EcoStruxure Cybersecurity Admin Expert (CAE) software.

The CAE offers an independent user manual which describes functions in a more detailed level, it can be downloaded from website of Schneider Electric.

The purpose of describing the CAE software in this manual is to help users start with the security configuration specific to the PowerLogic P7. For a thorough understanding of the CAE functions, see the CAE user manual.

Introduction of CAE software

CAE allows users to centrally update usernames and passwords for all PowerLogic P7 devices in the same local area network without having to do it bay-by-bay. It can customize the rights of user roles and user accounts. More advanced features of CAE include configuring the Syslog server, extracting locally saved security logs from devices, and centralized authentication over RADIUS/LDAP protocol with a Microsoft Active Directory or RADIUS server as the back end.



A	Ethernet	B	Security logs

Changing initial password

When launching CAE for the first time it will prompt for username and password. The default username is *SecurityAdmin* and the default password is AAAAAAAA. Both are case sensitive.



After correctly entering the default username and password, CAE will ask for the default password of the SecurityAdmin account to be changed.

Account will be locked if password is entered incorrectly up to 5 times. If this is the only SECADM account of a project, waiting for a few minutes is obliged before any further attempts with the same account. Alternatively, the blocked account can be unblocked with another SECADM account immediately by using it to open the project. Once the project is opened, all blocks of SECADM accounts will be cancelled immediately.

After correctly enter the default username and the initial password, CAE will force to change the initial password of the SecurityAdmin account



There is no password complexity requirement for a new project. When entering password input, click and hold the icon of eye to verify input.

NOTE: It is strongly recommended to add a backup SecurityAdmin account so that it can be used to unlock the CAE projects and reset the device passwords when the main SecurityAdmin account password is lost.

CAE user interface overview

EcoStruxure Cybersecurity Admin Expert (CAE) user interface window is composed of three main work areas:

1. Project Manager pane
2. Selection pane
3. Settings pane



- **Menu bar**: Provide functions to manage user accounts, manage roles and permissions, manage policies and settings, manage known devices, discover devices and update device security. The organization of functions follows a typical configuration workflow and user can jump from one to another.
- **Preferences**: Provide the function to edit application preferences such as settings for general information, security and dialog box.
- **Username**: Provide the function to display the logged in username.
- **Log out**: Provide log out function from the application.
- **?**: Provide help function to show the application logs and application information.
- **Create/Export/Import project**: Provide the function to create, export or import CAE security configuration project database.

Most CAE functions can be used without connection to PowerLogic P7 devices. Connection with devices in the same local area network (LAN) is only required when using function of **MANAGEMENT OF SYSTEM** for pushing new settings to devices.

The CAE functions on menu bar are listed as follows:

- **USER ACCOUNTS**: Provide the functions to create, rename, remove an account, change the password of an account and assign accounts to roles.
- **ROLES**: Provide the functions to create, remove roles and modify the privilege.
- **SECURITY SETTINGS**: Provide the functions to set security-related features, such as session time out duration, password complexity requirement, Syslog server and account locking.
- **SYSTEM EDITOR**: Provide the functions to import, export, add devices in the network.
- **MANAGEMENT OF SYSTEM**: Provide the functions to discover devices in the network and push the security settings to devices.

CAE recommended workflow

The security settings of devices are managed with the CAE by projects. Each project contains a set of roles and user accounts, with various security-related settings. The project can work offline. There is no need of connection to PowerLogic P7 devices when changing the settings. When offline work is done, the CAE must connect with devices and send the settings to them.

NOTE: Changing device security settings with the CAE is a one-direction process. The new settings can be pushed from the CAE project to the PowerLogic P7. The existing security settings cannot be extracted from the PowerLogic P7.

1. To manage the project, from the **Project manager** pane, open an existing CAE project or create a new project.

   Refer to Projects, page 104.

2. To manage the roles, from the **ROLES** menu, check whether the default rights of roles are in line with your organization cybersecurity policy.
   - Privileges can be changed for existing roles.
   - New roles can be created.
   - Existing roles can be removed.

   Refer to Roles, page 104.

3. To manage the user accounts, from the **USER ACCOUNTS** menu, create, remove or modify user accounts, assign roles and set password for accounts.

   Refer to User accounts, page 105.

4. To manage other security settings, from the **SECURITY SETTINGS** menu, set options including timeout, user account locking, password complexity, Syslog server, Security banners and centralized authentication methods.

   Refer to Security settings, page 107.

5. Optionally, to declare the devices, from the **SYSTEM EDITOR** menu, provide IP addresses of devices to the CAE for connection. The CAE can discover PowerLogic P7 devices automatically via Device Profile for Web Services (DPWS) and User Datagram Protocol (UDP).

   Refer to System editor, page 109.

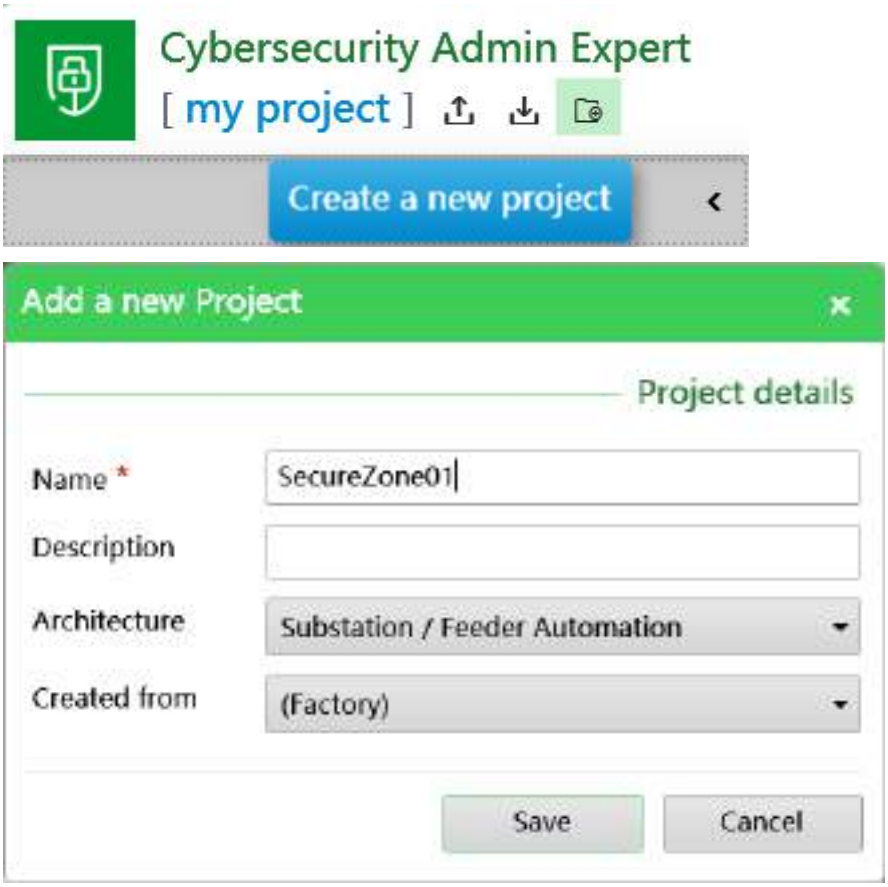
6. To prepare the connections between computers with the CAE and the PowerLogic P7, connect them via Ethernet and the front USB port. Use only one type of connection at a time for a same device.
   - To connect via Ethernet connection, confirm the CAE computer is in the same local area network (LAN) with devices to be managed.
   - To connect with front USB port, confirm only one device is to be connected.

7. To push new security settings to the PowerLogic P7, from **MANAGEMENT OF SYSTEM** menu, enable discover function to find all devices, and push new security settings to them.

   Refer to Management of system, page 110.

Projects

1. Click **Create a new project** to create a new project.



2. Select an option in **Architecture** field to set the **Security Setting** menu.
3. Select *Factory* in **Created from** to use CAE default template. Optionally, the template can also be created from one of the existing projects.
4. Click **Save** to save the project.
5. Double click the new project in the **Project manager** pane to switch to the project.

   Authentication request is pop-up.
6. Type the account *SecurityAdmin* and default password *AAAAAAAA* to login.

   No password complexity is required for a new project. CAE projects can only be opened by **SECADM** (Security Administrator) role.

   Force changing initial password window is displayed.
7. Type the customized password for the account *SecurityAdmin*.

   The project will be loaded with CAE default template settings if *Factory* is selected to create the project from.

Roles

The default roles for CAE projects are as follows:



NOTE:

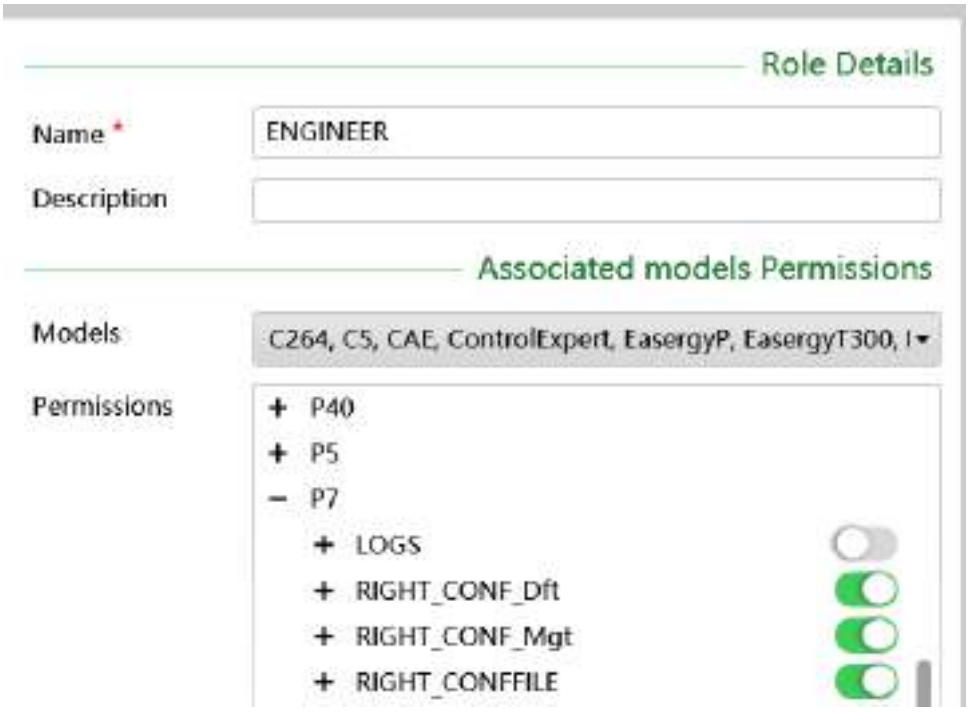
- Only SecurityAdmin account (with *SECADM* role) is allowed to modify CAE projects and push security settings to devices.

It is recommended to remove the role *RBACMNT* unless it is absolutely needed.

The privileges of existing roles can be modified in the **Role Details** fields. CAE is designed to manage security settings for multiple Schneider Electric products.

To modify privileges of the PowerLogic P7, click **+** sign at the left of **P7** and leave the other products.

NOTE: The setting **EasergyP** is not for the PowerLogic P7.

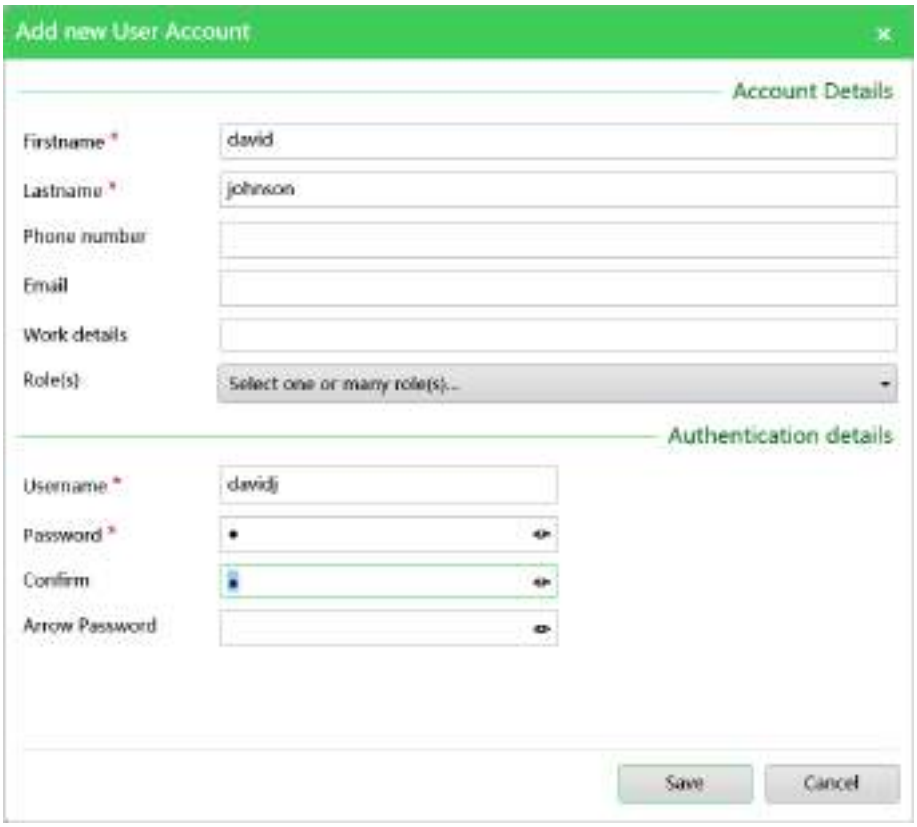


User accounts

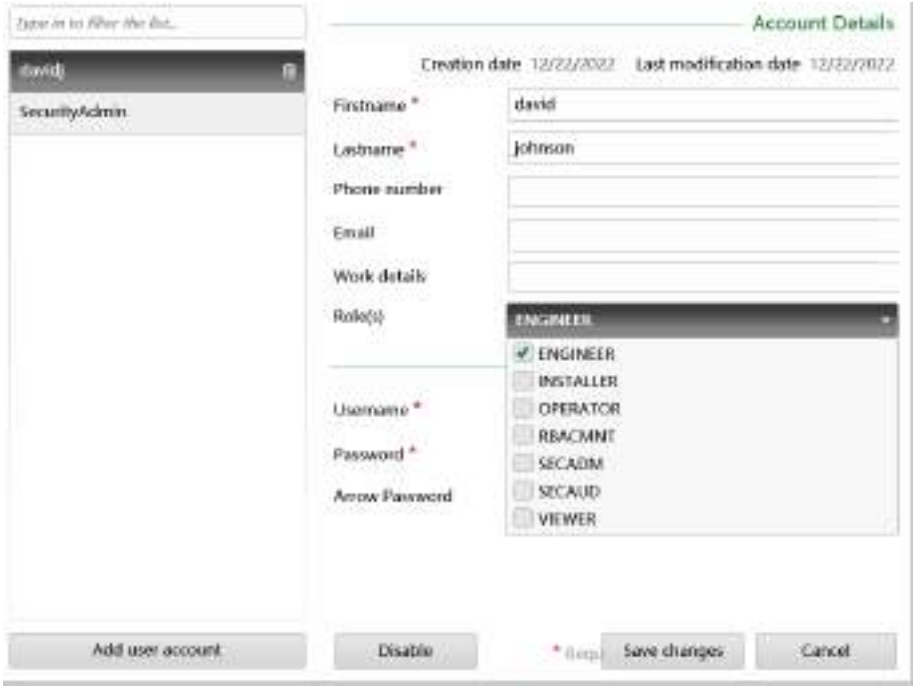
The only existing user account of any new projects which are created from *Factory* template is SecurityAdmin.

1. Click the **Add user account**.

2. Type the text in the mandatory fields of **Firstname**, **Lastname**, **Username** and **Password**.
   - The username and password are both case sensitive for the authentication.
   - The username is the name which must be given for login to the PowerLogic P7. The first name and last name will NOT be asked by the device for login.
3. Click **Save**.



4. In the **Account Details** panel, select the role(s) for the new account.
   - One account can be assigned with multiple roles. It will get the privileges of all the assigned roles combined.
   - The arrow password which facilitates operation of password input on device HMI with arrow buttons. This feature is only useful for devices without alphanumeric keypad in device HMI.



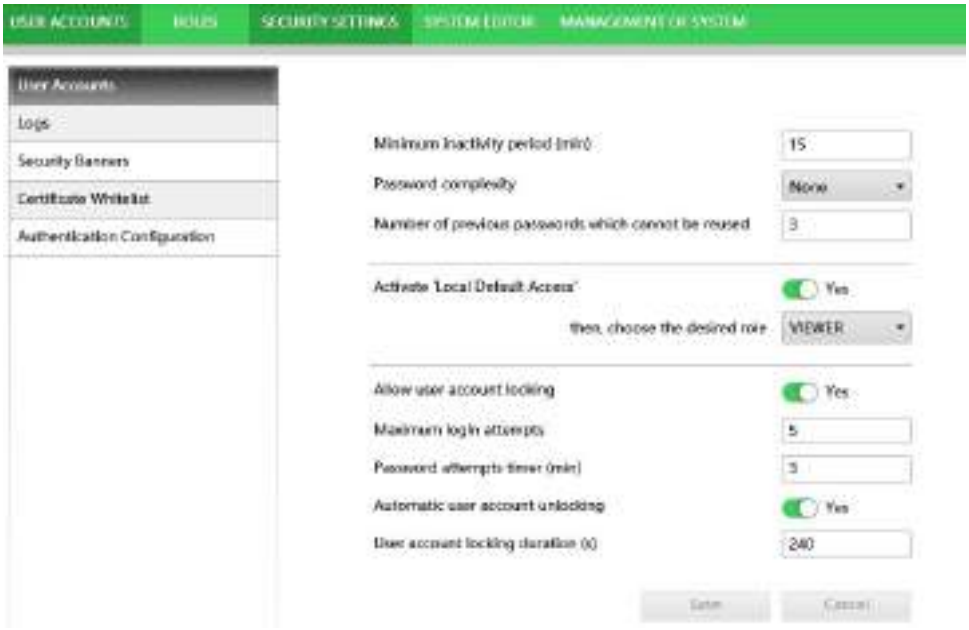
- It is strongly recommended to create a 2nd user account assigned with *SECADM* role, so that if the 1st *SecurityAdmin* password lost, the 2nd *SECADM* account can be used to open the CAE project and recover passwords.
- In case of managing multiple CAE projects in parallel, keep at least one *SECADM* account with same password across the projects.
- *SecurityAdmin* is the account with hardcoded username for all CAE projects as well as for the devices. It cannot be deleted. The username cannot be changed. It can only have *SECADM* role.
- Make sure to save changes for each account before moving to another account or another menu.

Security settings

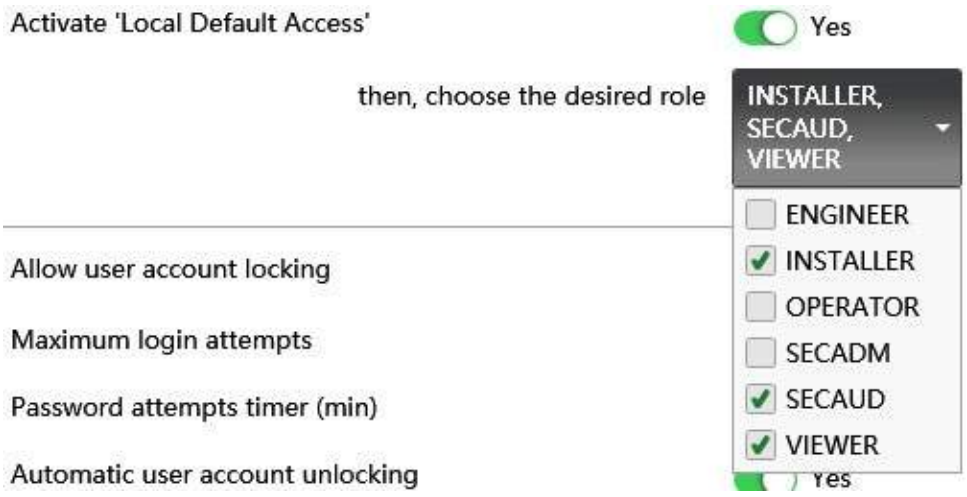
The **Security settings** menu allows configuration of security parameters and consists of the following menu items.

User accounts

The CAE is delivered with default security parameters as follows:



To facilitate operation and setting via local HMI, **Activate 'Local Default Access'** can be set to *Yes* to grant automatically selected privileges of the role. Anyone who can access to local HMI will have the privileges of the roles assigned with *'Local Default Access'*. The default setting is *VIEWER*. But it can be extended to multiple ROLES if needed as follows:



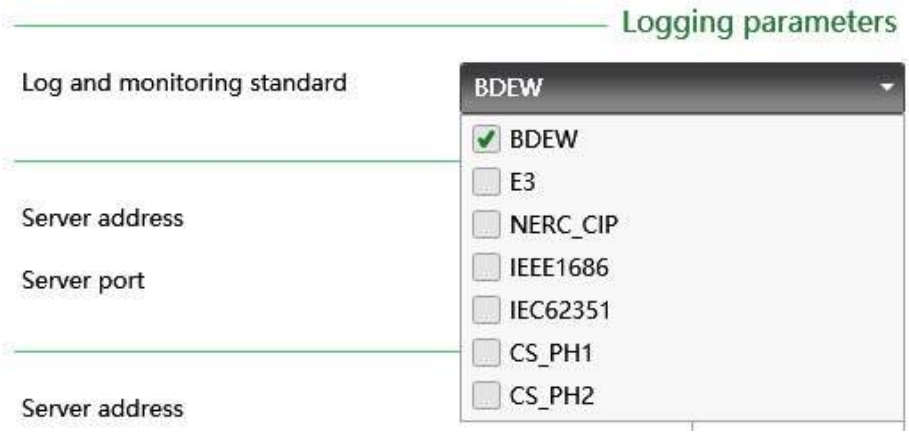
The *'Local Default Access'* option is only available for Substation / Feeder Automation architecture.

NOTE: The setting of project architecture will also impact the following options.

- **Allow user account locking**: can only be *YES* for Critical Power and Plant Automation.
- **Automatic user account unlocking**: can be only *YES* for Critical Power and Plant Automation.

Logs

- **Logging parameters**: No standard was enabled when the PowerLogic P7 was released from the factory. It will not generate any security log before been managed with the CAE. During creation of a new CAE project the default standard enabled by the CAE is *BDEW*. The device also supports security logs according to IEEE 1686 standards. For type of logs and which will be generated for both standards, see Security event logging, page 98.



- **Syslog parameters**: Input remote Syslog server address and port in this section. The device will send all the internally generated security logs to server for backup after address and port defined.
- **SNMP parameters**: The options shall not be used since the device does not support SNMP.

Certificate allowlist

The security banners are warning messages displayed on device HMI login interface for system use notification.

The PowerLogic P7 connects with the CAE via HTTPs. The device works as a server with device self-signed HTTPs certificate to help ensure the credentials and contents will not be transmitted in clear text.

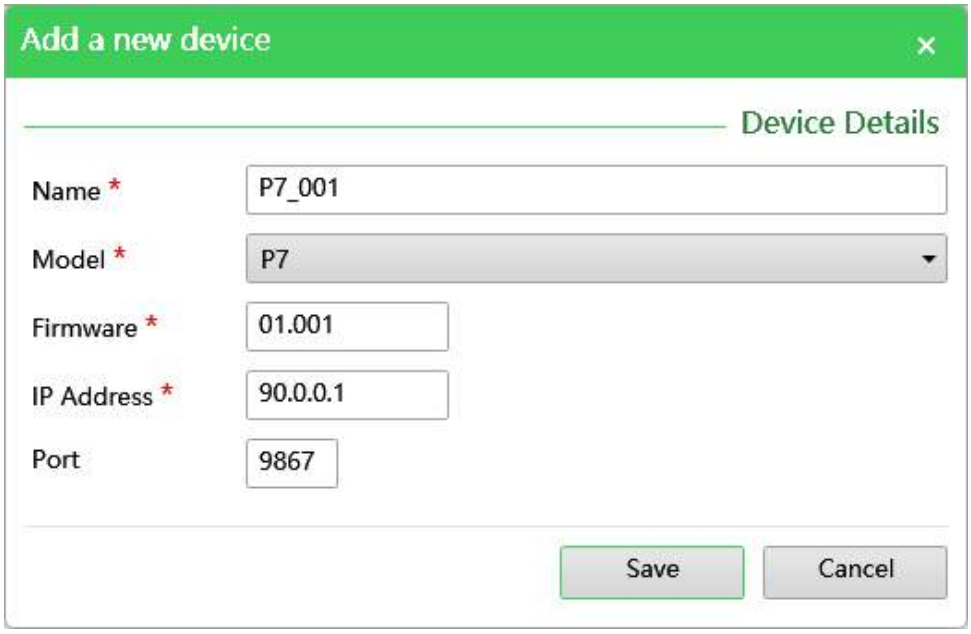


At network discovery, the CAE searches for the certificates of the devices connected to the system network, then the Security Administrator can decide whether to trust or not the detected certificates. When the Security Administrator trusts a device certificate, this certificate is stored by the CAE, so that at next discovery, the CAE will be able to identify the certificate.

System editor

The **System editor** menu is optional for the PowerLogic P7, because the CAE can discover PowerLogic P7 devices in the same local area network automatically with DPWS and UDP.

NOTE: In rare occasions the CAE may not discover all PowerLogic P7 devices in the same network. In this case, declaring them will help the CAE find them.



Management of system

When all security settings are done, they can be pushed to PowerLogic P7 devices.

Connecting to the PowerLogic P7 with the CAE

The CAE can connect with the PowerLogic P7 via Ethernet or front USB port.

- To use the Ethernet connection, please ensure that the CAE computer is in the same local area network with PowerLogic P7 devices to be managed.
- To use the front USB port, please ensure the good connection by USB cable between the CAE computer and the PowerLogic P7. Make sure that the device USB cable driver is installed. The device IP address for the front USB port is always 90.0.0.1.

It is recommended to use PING command to verify the connection between the PowerLogic P7 and the CAE computer beforehand.

Push the new security settings to the PowerLogic P7

To find all PowerLogic P7 devices automatically in the same LAN,

1. Click **Discover**.



   If the devices cannot be found, re-try after disabling the firewall in the CAE computer.

   For new devices which have been found the first time, it is necessary to Trust them first by adding their HTTPs certificate into the certificate allowlist of the CAE. The new PowerLogic P7 devices will ask for Security Admin password, which is **AAAA**.

2. Click **Send security configuration** to push new security settings to the devices. The Security Admin password will also be updated as they are set in the CAE project.

Retrieving the PowerLogic P7 internal security logs

- Right click on the PowerLogic P7 in the list of discovered devices to retrieve security logs from the device. This operation can take a few seconds.

The PowerLogic P7 keeps security logs with a cyclic non-volatile memory, upon reaching the limit of memory file size the earliest entries will be replaced by new ones.

Adding a device certificate issued by CA

Additional certificates issued by Certificate Authority (CA) entities can be added to the device for some connections to be securely established (with Syslog server, for example). To do this, follow the steps below:

1. Import the root certificate of the CA to the CAE.
   a. Open the CAE on a computer connected to the device, either with the front USB port or an Ethernet LAN.
   b. Under **SECURITY SETTINGS > Certificate management > Certificate store**, click **Add**.
   c. In the pop-up window, import the root certificate from a local directory.
   d. Click **Save**.
2. Add the root certificate to the device's trusted chain.
   a. Click **MANAGEMENT OF SYSTEM**.
   b. Run a synchronization.
   c. Right click the discovered device.

      NOTE: If the device has not been trusted by the CAE before, trust the device in the context menu and click **Send Signing Certificate** at the bottom right of the **MANAGEMENT OF SYSTEM** tab.
   d. Under **Certificate Management > Trusted chain**, click **Add Certificate (s)**.
   e. Select the imported root certificate and click **Update**.
   f. Click **Yes**.
   g. Click **OK**.
3. Add the CA-issued device certificate to the device.
   a. Under **Certificate Management > Internal**, click **Add PFX**.
   b. From a local directory, import the PFX file that contains the certificate.
   c. Input the password to the PFX file.
   d. Click **Import**.

      Note: If Step 3, page 111 isn't applicable, the device can be enrolled to the CA with the existing self-signed certificate. To do this, use the **Enroll PFX** option on the same page and the automatic enrollment feature in the CAE. See the Certificate Management chapter of the CAE manual for details.

User accounts and rights

Recommendations to optimize cybersecurity in a protected environment:

- Assign users only the essential rights needed to perform their role.

- Revoke user rights when no longer needed due to role change, transfer or termination. User credentials do not expire.
- Follow user account management tasks as described by your organization or contact your network administrator.

List of roles

The PowerLogic P7 menus and screens are accessible according to the RBAC to help prevent unauthorized operation. RBAC is essentially a collection of permissions. Users are assigned particular roles, and through those role assignments acquire the permissions to perform particular functions. Since users are not assigned permissions directly, but only acquire them through their role (or roles), management of individual user rights becomes a matter of simply assigning appropriate roles to the user's account; this simplifies common operations, such as adding a user, or changing user's account.

Table 19 - List of roles for cybersecurity

Role	Default user account	Description
VIEWER	ViewerLevel	Can view all information except security logs which are present within the PowerLogic P7 and read their value. A viewer cannot modify settings and files.
OPERATOR	OperatorLevel	Has the same rights as Viewer and can perform control actions and change setting.
ENGINEER	EngineerLevel	Has the same rights as Operator and can configure and set the PowerLogic P7. They can retrieve and analyze process data and records, perform control actions and change setting groups.
INSTALLER	DefaultInstaller	Has the same rights as Viewer plus the right to upgrade firmware[9]. Retrieve the PowerLogic P7 and process data during commissioning and change the configuration and / or setting groups during installation.
SECAUD	DefaultSecAud	Can read security logs. A security auditor can access user authentication logs.
SECADM	SecurityAdmin	Can change the security policy (user, roles and rights) of the PowerLogic P7.

RBAC of the PowerLogic P7 is compliant with IEC 62351 part 8 and, with CAE, can be extended further depending on the organization.

List of rights

For customer use, PowerLogic P7 devices have been designed in order to allow and control the following usages:

- Read the information provided by the PowerLogic P7: measurements, status of the controlled and monitored switchgears, settings, alarms, tripping context.
- Open and close the switchgears.
- Upload the log files and disturbance record files.
- Configure the PowerLogic P7 for integration into the cubicle, protection and control.
- Configure the PowerLogic P7 for integration into a SCADA system.

These usages are realized by assigning specific right(s) to the users of the PowerLogic P7 based on their role in the RBAC.

9. For this feature, please contact Schneider Electric for more information.

The followed table shows roles and their rights granted by default for the PowerLogic P7.

Table 20 - Roles and their access rights

Rights/Roles	VIEWER	OPERATOR	ENGINEER	INSTALLER	SECADM	SECAUD
Certificate Management					■	
Logs					■	■
Security					■	
Configuration read	■	■	■	■		
Configuration change		■	■			
Setting read	■	■	■	■		
Setting change		■	■			
Protection group setting read	■	■	■	■		
Protection group setting change			■			
Control status read	■	■	■	■		
Control operation		■	■			
Data read	■	■	■	■		
Data object list	■	■	■	■		
Configuration file upload			■	■		
Firmware upload			■	■		

NOTE: The role-to-right assignment can be modified using CAE.

Table 21 - List of rights

Rights	Short description	FC	Description
RIGHT_CONF_Dft	Configuration read	CF	Permission to read the configuration, for example, the operation time-out for a control object.
RIGHT_CONF_Mgt	Configuration change		Permission to modify the configuration, it means we can change any settings which need a reboot of the device, for example, the operation time-out for a control object.
RIGHT_SETTING_Dft	Setting read	SP	Permission to read any settings which do not need a reboot of the device, for example, LCD time-out, LCD dark mode and so on.
RIGHT_SETTING_Mgt	Setting change		Permission to modify any settings which do not need a reboot of the device, for example, protection or communication settings, switching device mode (mode on, mode test/blocked, mode off).
RIGHT_PROT_ SETTING_Dft	Protection group setting read	SE/SG	Permission to read any protection group settings which do not need a reboot of the device, for example, protection threshold or operation time.
RIGHT_PROT_ SETTING_Mgt	Protection group setting change		Permission to modify any protection group settings which do not need a reboot of the device.
RIGHT_CONTROL_Dft	Control status read	CO	Permission to read control data object.
RIGHT_CONTROL_ Mgt	Control operation		Permission to perform all kind of operations (select, open or close all switches, reset indications).
RIGHT_DATA_Dft	Data read	ST/MX	Permission to read all the data (i.e., measurements, status, model number and other fixed device information, ….), logs, …
RIGHT_DATA_ListObj	Data object list		Permission to list the data model directory.
RIGHT_CONFFILE	Configuration file upload	—	Permission to deploy configuration files to device.
RIGHT_FIRMWARE	Firmware upload	—	Permission to upgrade firmware of the device.

HMI Auto-login

To facilitate the commissioning work by panel builder and system integrator, the PowerLogic P7 provides an Auto-login feature when manufactured. This feature grants privilege of the role of ENGINEER for HMI access, without request of password. All roles and rights are described in List of rights, page 112 and List of roles, page 112.

Login

If the front panel auto-login has been changed from ENGINEER, it is necessary to login in to perform control actions or setting changes. If this is required, touch the icon to locate to the User Login screen, enter the name or role and the password. Refer to Login, page 128 for more information.

For login by the PowerLogic Engineering Suite, refer to Connecting to the device using the mini-USB cable, page 133 or Connecting to the device via Ethernet, page 133 for more information.

Only a Security Admin role (SECADM) can login to a CAE project by CAE tool.

Access lockout

The first invalid password entry sets the counter of failed authorization and initiates an attempt timer.

If the user reaches the maximum number of retries, a message is displayed and the user is blocked. In this case, only the VIEWER access rights are granted and any other access is blocked.

The maximum number of failed authentications is set by CAE. The default is defined at 5 and can be set up to 99.

When the maximum number of failed authentications is reached, a lockout period is activated. This lockout period is by default 3 minutes with a maximum of 30 minutes. It can be set by CAE.

If the attempt timer expires, or the correct password is entered before the attempts counter reaches the maximum number, then the attempts counter is reset to zero.

If a user is locked out, the block is applied to that user for all the PowerLogic P7 interfaces. The blocking of one user does not result in blocks to the others.

If the user entry is blocked, recovering the RBAC or pushing a new RBAC will not reset the blocked user entry, but a PowerLogic P7 reboot will reset the blocking time and attempts counter, so the user entry will be unblocked.

NOTE: Set sufficient **Maximum login attempts** and **Password attempts timer** to allow user connection after errors.

Logout

If the user logins manually via front panel and there is no operation within the **Minimum inactivity period**[10], the user will be logged out. After logout, if **Active 'Local Default Access'** field is selected in *Yes*[10], the default ENGINEER role will automatically login via front panel, otherwise, the front panel will remain logout.

A user icon in the top right corner of the title bar indicates the login status of the PowerLogic P7. The user icon changes from grey to green color when any user logs in.

10. The parameter is configured in CAE.

NOTE: It is recommended to set **Minimum inactivity period** to 15 minutes in order to download or upload files during installation, operation and maintenance.

Number of accounts

The maximum number of user accounts which can be memorized in the PowerLogic P7 is 255.

Session management

The maximum connection per role is one when login as Operator or Engineer, except the auto-login connection from the local control panel.

Centralized authentication

Centralized authentication enables the user account and privilege management of the PowerLogic P7 to be merged into an existing authentication infrastructure in the customer network. The PowerLogic P7 supports centralized authentication via RADIUS protocol or LDAP protocol, which are used to communicate with a RADIUS server or a Microsoft Active Directory server (AD server), respectively.

With centralized authentication configured, users can keep using their existing username for other devices such as other protection relays, network switches, workstations on the PowerLogic P7. The existing RADIUS server or AD server in the customer network can also be used to manage the user account and privilege for the PowerLogic P7. Once the account settings are changed at the RADIUS or AD server, the PowerLogic P7 will take account of those changes for user authentication and authorization.

Solution overview

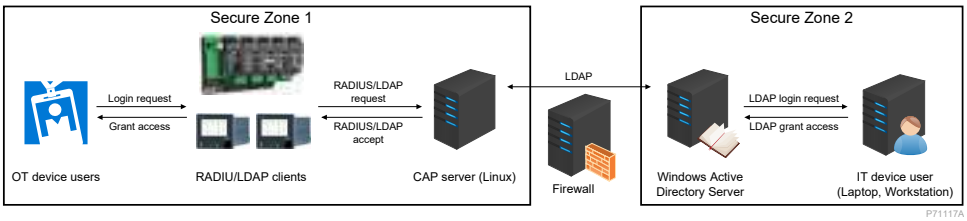
Depending on the existing authentication server used in the customer network, different solutions are available:

- If the existing authentication server is an AD server, the PowerLogic P7 can be directly connected to the AD server or connected to the AD server with the Cybersecurity Application Platform (CAP) as a proxy. To simplify the firewall setup, connecting to the AD server with the CAP is recommended.
- If the existing authentication server is a RADIUS server, the PowerLogic P7 can be directly connected to the server.

AD Server as the existing authentication server

When the existing authentication server is an AD server, connecting PowerLogic P7 devices to the AD server with the CAP as a proxy is recommended because this method simplifies the firewall setup.

Figure 52 - Connecting PowerLogic P7 devices to the AD server with the CAP as a proxy

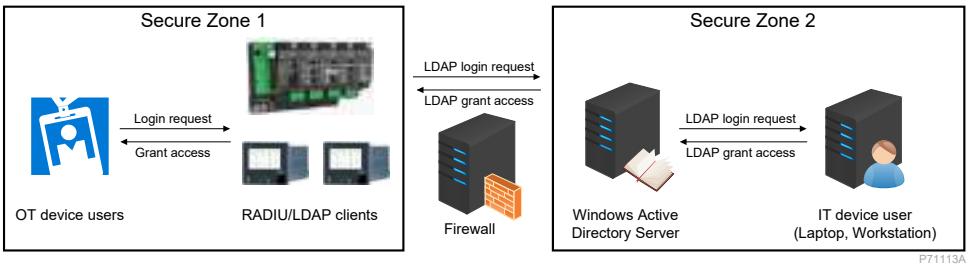


In Connecting PowerLogic P7 devices to the AD server with the CAP as a proxy, page 116, the CAP server is placed in Secure Zone 1, where PowerLogic P7 devices and other devices such as RTUs, switches are also located. The firewall only needs to allow the connection between the CAP server and the AD server, which makes the setup easier and more scalable.

NOTE: Secure Zone 1 is considered to be the most isolated and secure segment, because it has OT devices that control the critical infrastructure devices such as circuit breakers and switches. Secure Zone 2 is the network segment used for information management services such as e-mail, file servers and the Internet. To ensure the security of Secure Zone 1, firewalls and/or network diodes are used to isolate Security Zone 1 from Security Zone 2.

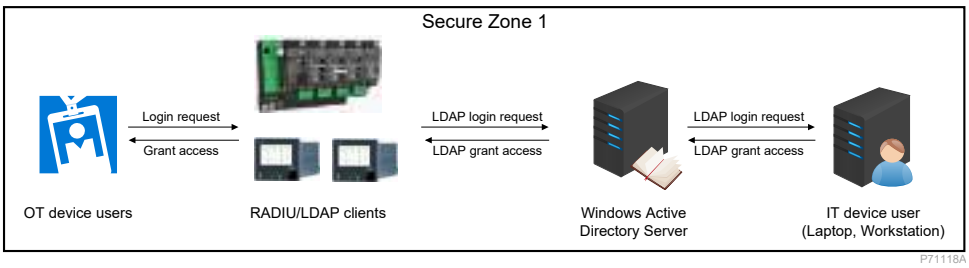
However, if using CAP is not ideal or possible, PowerLogic P7 devices can be directly connected to the AD server over the LDAP protocol.

Figure 53 - Directly Connecting PowerLogic P7 devices to the AD server



In Directly Connecting PowerLogic P7 devices to the AD server, page 116, the PowerLogic P7 devices and the AD server are directly connected and are located in different Secure Zones. As a result, the firewall needs to allow all connections between the PowerLogic P7 devices and the AD server.

Figure 54 - Directly Connecting PowerLogic P7 devices to the AD server without the firewall



In Directly Connecting PowerLogic P7 devices to the AD server without the firewall, page 116, the PowerLogic P7 devices and the AD server are directly connected and are located in the same secure zone, so there is no need to install a firewall.

RADIUS server as the existing authentication server

When the existing authentication server is a RADIUS server, PowerLogic P7 devices can be directly connected with the authentication server.

The RADIUS authentication server can be placed in the same secure zone with PowerLogic P7 devices as shown in Directly connecting PowerLogic P7 devices to the RADIUS server without the firewall, page 117, or placed in a different secure zone as shown in Directly connecting PowerLogic P7 devices to the RADIUS server with the firewall, page 117. In the latter approach, the firewall must be set to allow connections between PowerLogic P7 devices and the RADIUS server.

Figure 55 - Directly connecting PowerLogic P7 devices to the RADIUS server without the firewall

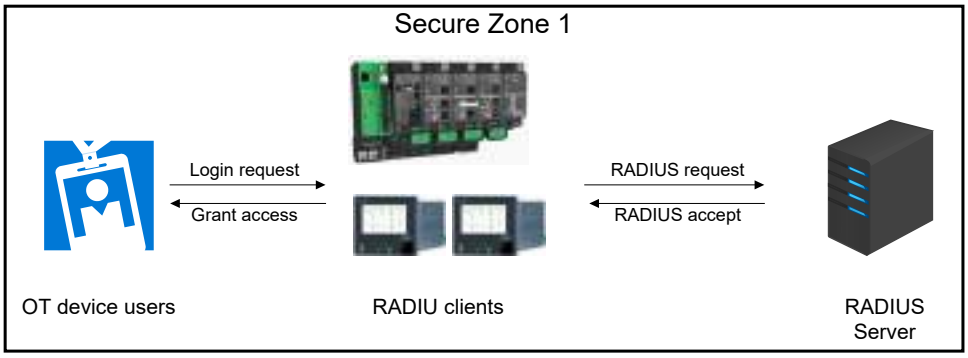
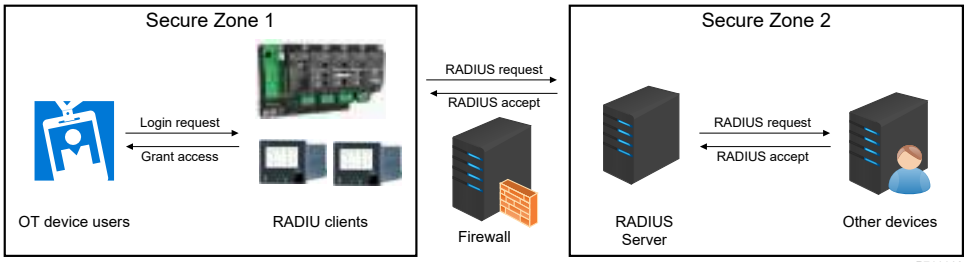


Figure 56 - Directly connecting PowerLogic P7 devices to the RADIUS server with the firewall



Configuration of centralized authentication

Depending on the existing authentication server used in the customer network, different configuration procedure is needed.

Configuring centralized authentication between the device and the AD server

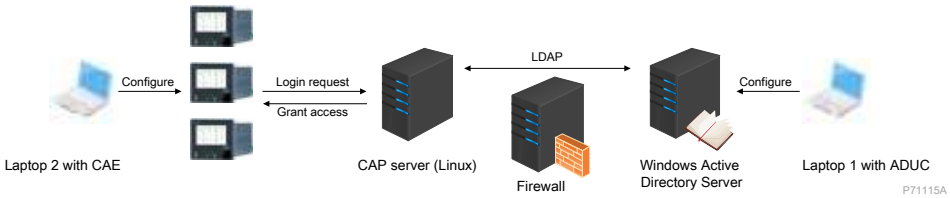
The following items are required to carry out the configuration:

- An AD server.
- A laptop with Active Directory Users and Computers (ADUC) installed. This is *Laptop 1*.

  NOTE: *Laptop 1* must be able to join the domain controlled by the AD server above. You need the domain administrator privilege on the AD server to achieve this.
- A laptop with CAE installed and the Security Admin privileges to both CAE and the PowerLogic P7. This is *Laptop 2*.

  NOTE: You can also install CAE on *Laptop 1* and only use one laptop as a result. The same Security Admin privileges are still required in such a case.
- A configured CAP server if you choose to connect via the CAP proxy.

Figure 57 - Connecting PowerLogic P7 devices to the AD server with the CAP as a proxy



The PowerLogic P7 can connect with the AD server either directly or connect with the CAP as a proxy as shown in Connecting PowerLogic P7 devices to the AD server with the CAP as a proxy, page 118. In both cases, the PowerLogic P7 and the AD server must be configured accordingly to ensure successful connection. The following guide will walk you through the full process.

Configuring the AD server for centralized authentication

In this procedure, a new user and a new group are created in the AD server. Then the new user is assigned to the new group. The *VALIDATION* Organizational Unit (OU) is used as an example of designated OU during the user creation steps.

1. On *Laptop 1*, open AUDC.
2. Expand the **val.ctc.se.com** domain.
3. Right click **OU VALIDATION**.
4. Click **New > User** on the pop-up menu.
5. Create the new user.

   As an example, below is the necessary information when creating a new user named *Alice Wang*:

   - First name: Alice
   - Last name: Wang
   - Full name: AWang
   - User logon name: Alice Wang
   - User logon name (pre-Windows 2000): Alice Wang

   NOTE: The full name **AWang** is the username used for authentication at the PowerLogic P7 device.
6. Back in AUDC of *Laptop 1*, expand the **val.ctc.se.com** domain.
7. Right click **Common Name (CN) Users**.
8. Click **New > Group** on the pop-up menu.
9. Create the new group.

   As an example, below is the necessary information when creating a new group named *Relay Engineer*:

   - Group name: Relay Engineer
   - Group name (pre-Windows 2000): Relay Engineer
   - Group scope: Global
   - Group type: Security
10. Click **OK**.
11. Add the created user *AWang* to the created group *Relay Engineer* with the following information:

    - **Select this object type**: Groups or Build-in security principals
    - **From this location**: val.ctc.se.com
    - **Enter the object names to select (examples)**: Relay Engineer

12. Click **OK**.

Configuring the device for centralized authentication

1. On *Laptop 2*, open CAE.
2. Click **SECURITY SETTINGS**.
3. Click **Authentication Configuration**.
4. Fill in the text boxes under **LDAP Protocol Details**.

   As an example, below is the necessary information when filling in the text boxes for the **VALIDATION** OU and the **val.ctc.se.com** domain:

   - Base DN: ou=VALIDATION, dc=val,dc=ctc,dc=se,dc=com
   - Server IP Address: The IP address of the CAP or the IP address of the AD server, depending on the connection method you are using.
   - Server Port: The corresponding port number at the AD server.
5. Click **Add a new group**, a text box appears.
6. Fill in the text box with *Relay Engineer*.
7. In the Roles list, check **ENGINEER** as shown in Map one role to one group, page 119.

Figure 58 - Map one role to one group



8. Click **Add a new group** again.
9. If you need to assign multiple roles to a group, fill in the text box with *Relay Power User*.
10. In the Roles list, check the roles you want to assign as shown in the example of Map multiple roles to one group, page 119.

Figure 59 - Map multiple roles to one group



11. Click **Add a new group** again.

Configuring centralized authentication between the device and the RADIUS server

The following items are required to carry out the configuration:

- A RADIUS server.
- A laptop with CAE installed.

Configuring the RADIUS server for centralized authentication

This procedure uses TekRADIUS as an example.

1. On the RADIUS server, open TekRADIUS Manager.
2. Click the **USERS** tab.

   Two panels are under the **USERS** tab. In the left **Browse Users** panel, you can find all created usernames and the groups they belong to. When you click a specific username, its attributes appear in the right panel, as shown in Map one role to one user, page 120.

   Figure 60 - Map one role to one user



3. In the **Browse Users** panel, click a username.
4. In the right panel, check the *Type* field of the second attribute is *Success-Reply* or not. If not, change it to *Success-Reply*.

   To the left of the *Type* field is the *Attribute* field for which you can choose any value available. The chosen value will be reused when configuring the device later.

5. Change the *Value* field of the second attribute to a specific role, such as *INSTALLER*.

   If multiple roles need to be assigned to one user, a semicolon is required to split the different roles. To assign the installer and engineer roles to a user, for example, you can change the *Value* of the second attribute to *INSTALLER; ENGINEER* as shown in Map multiple roles to one user, page 120.

   Figure 61 - Map multiple roles to one user



Configuring the device for centralized authentication

1. On the laptop, open the CAE software.
2. Click **SECURITY SETTINGS**.
3. Click **Authentication Configuration**.
4. Under the drop-down menu of **Centralized authentication protocol**, choose Radius.
5. Under the drop-down menu of **Mode**, choose *RADIUS_CLEAN* or *EAP_TTLS*.
6. Fill in the **IP address**, **Port** and **Shared secret** of the RADIUS server, and the role *Attribute* that you have chosen when configuring the RADIUS server.

Passwords

Changing password

The password change is done exclusively through the CAE tool by a SECADM user.

Password complexity

The PowerLogic P7 accepts the default username **EngineerLevel** and the default password **AAAA**.

The PowerLogic P7 password complexity can be configured by CAE and there is no restrictions by default in the device.

With CAE it is possible to configure the password according to NERC and IEEE 1686 standard recommendations.

Standard	Configuration
NERC	8 characters minimum with ASCII [33 to 122] characters. The lesser of three or more different types of characters (e.g. uppercase alphabetic, lowercase alphabetic, numeric from 0 to 9, non-alphabetic characters)
IEEE std1686	8 characters minimum with ASCII [33 to 122] characters 1 lowercase letter, 1 uppercase letter, 1 digit from 0 to 9 and 1 non-alphabetic character

Password reset

When a password is lost, following options are available to reset the password to default:

- by the security administrator

  The security administrator can reset the passwords for the other users with the CAE tool.

- through device factory reset

  The passwords can be reset after the factory reset of the device. Please refer to Performing factory reset, page 461.

  NOTE: A factory reset will result in loss of all device configuration and stored data, the device will reboot and operate the watchdog contact. Reserve the security log is optional during the factory reset operation.

Default password setting

NOTICE

UNAUTHORIZED EQUIPMENT TAMPERING

At the first use of the PowerLogic P7, change the default passwords.

Failure to follow these instructions can result in unauthorized product use and setting changes, and compromised security of the information contained in the product.

When delivered from factory, the RBAC configuration of the PowerLogic P7 is as follows:

Table 22 - Default password settings

Role	User account	Password	Min inactivity period	Number of previous pass-words[11]	Max login attempts	Password attempts timer	User account locking duration
VIEWER	ViewerLevel	AAAA	1 min	3	5 times	3 min	240 sec
OPERATOR	OperatorLevel	AAAA					
ENGINEER	EngineerLevel	AAAA					
INSTALLER	DefaultInstaller	AAAA					
SECADM	SecurityAdmin	AAAA					
SECAUD	DefaultSecAud	AAAA					

The PowerLogic P7 does not have any backdoors such as super password as authentication-bypass mechanism.

Port hardening

It is possible to disable communication ports from the **Device configuration > Slot A** tab of PowerLogic Engineering Suite.

The rear Ethernet ports and the logical ports on each rear Ethernet port can be independently disabled.

These logical ports are listed below with Ethernet port number in brackets:

- PowerLogic Engineering Suite Web Server (port 8080/8443/9867)
- IEC 61850 (port 102)
- DNP3 over Ethernet (default on port 20000, configurable)
- Modbus TCP/IP (default on port 502, configurable)

NOTE: By default, all logical ports listed above are disabled except the Web Server port on P7 PORT1. It is strongly recommended to keep unused ports disabled to reduce the risk of attack to the PowerLogic P7.

Security event logging

The following types of time-stamped events are logged in a dedicated security log file:

NOTE: For a detailed list of all the events logged, see List of security event logs, page 123

- Security parameter changes (such as user creation, password change)
- User authentications, attempt to authentication and logout
- Certificate updates
- Access to the security events
- Device reboots
- Device software updates
- Protection parameter changes

  Only the occurrence of the first change in each session is logged.
- Setting-group change, with the mention of the active setting group
- Control, configuration uploading, firmware uploading
- File downloading

11. The previous passwords cannot be reused.

The PowerLogic P7 can store up to 3 event files with maximum 256 KB of each file. When the maximum capacity is reached, the oldest events are erased.

NOTE: The existing security event log files are backed up to the **csbak** directory during firmware update.

The audit event logs are read-only and cannot be erased by any users. During the factory reset, however, if authorized by a user with firmware upload privilege (ENGINEER or INSTALLER role by default), they can be erased.

The security events can be read from the PowerLogic P7:

- By central server tool or any security server automatically
- By CAE with the security administrator access rights

Security logs depend on the security standards that are configurable by the CAE.

The security logs are pushed to a Syslog server over TLS-encrypted connection, if the Syslog server IP address and IP port are configured and connected. To establish the connection, the following requirements must be met:

- The device trusts the Syslog server by having any of the following certificates in the device's trusted chain:
  - The Syslog server certificate
  - The root certificate of the CA that issued the Syslog certificate
- The Syslog server trusts the device by having any of the following certificates in the Syslog server's trusted chain
  - The device certificate
  - The root certificate of the CA that issued the device certificate

Use the CAE to add certificates to the device's trusted chain, the detailed instructions for which can be found in Adding a device certificate issued by CA, page 111. Actions on the Syslog server side are done outside the CAE.

The generalized security logs include the information according to events definition in IEEE 1686 and IEC 62351 Part 7.

Table 23 - List of security event logs

Event	BDEW	E3	NERC CIP	IEEE 1686	IEC 62351	CS Phase I	CS Phase II	severity
Successful connection	■	■	■	■		■		INFO
Failed connection (wrong credentials)	■	■	■	■		■		WARNING
Failed connection (wrong credentials) triggering the blocking of the account on the IED	■	■	■	■		■		EMERGENCY
Failed connection because of a blocked user ID on this IED	■	■	■	■		■		EMERGENCY
Disconnection triggered by the peer/user	■	■	■	■		■		INFO
Disconnection triggered by a timeout	■	■	■	■		■		INFO
Update of the RBAC cache in the IED				■		■		INFO
Update of the security policy database				■			■	INFO
Retrieval of the security logs of the IED				■				INFO
Any authorization request sent to the CS Brick			■		■	■		INFO
Device had to renew its local key and certificate							■	INFO
Certificate expired							■	INFO/WARNING

Table 23 - List of security event logs (Continued)

Event	BDEW	E3	NERC CIP	IEEE 1686	IEC 62351	CS Phase I	CS Phase II	severity
A corruption is detected in the parsing of the file storage module							■	INFO
Domain changed							■	INFO
Radius server configuration changed							■	INFO
Radius dictionary changed							■	INFO
Internal enrolment failure							■	ERROR
Cannot install certificate into the store							■	WARNING
cert/key generation failure							■	ERROR
Trusted chain valid							■	INFO

Upgrades management

When the PowerLogic P7 firmware is changed, the security configuration will be replaced by the default configuration. It is recommended that the security configuration is reviewed after an upgrade to analyze rights for new or changed device features and revoke or apply them according to your company's policies and standards. Users can manually update the security configuration by using CAE.

The PowerLogic P7 firmware is signed by Schneider Electric global signing center. During the upgrade procedure the firmware will be checked for authenticity by decrypting the signature with the public key kept with the product read-only memory.

Schneider Electric cybersecurity support

The Schneider Electric website provides the list of known vulnerabilities and allows cybersecurity administrators to report an incident or vulnerability.

Visit Schneider Electric cybersecurity homepage at Report a cybersecurity incident | Schneider Electric Global.

Operation

The front panel, if fitted, can be used for both entering all the data required for operation of the PowerLogic P7 and accessing the data for device management.

The following tasks are available from the front panel:

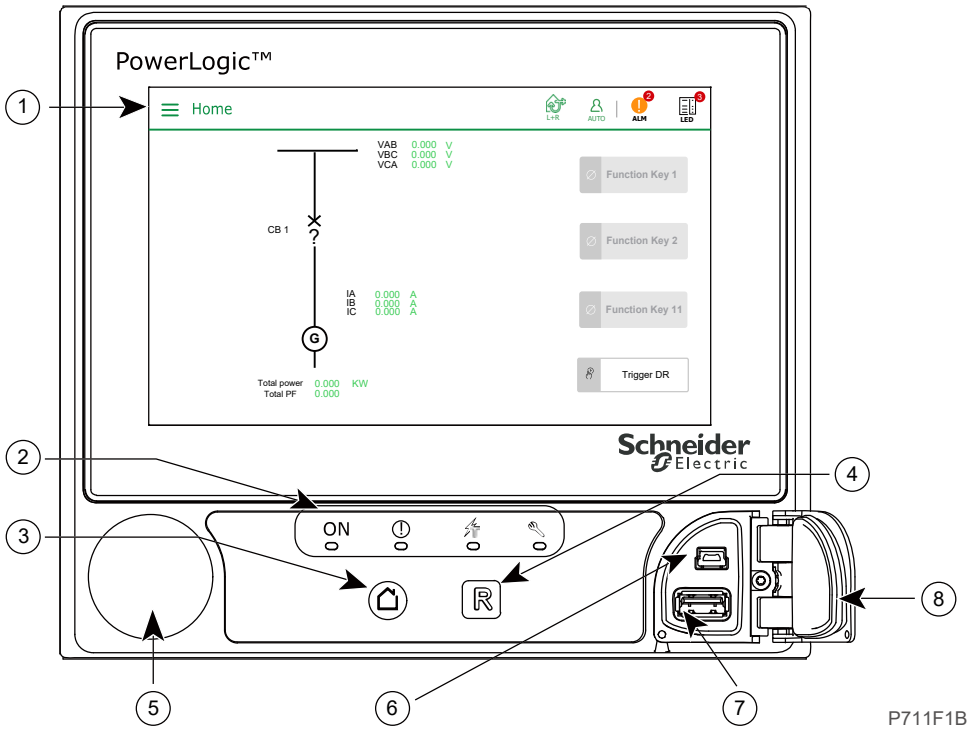
- Control switchgear units
  - View device status on an animated mimic diagram
  - Local opening and closing devices controlled by the PowerLogic P7
- Readout and modification of settings
- Readout of live operating data
- Readout of operating data logs
- Readout of event logs after overload situations, ground faults, short circuits and so on. in the power system
- Readout of hardware and firmware options from related version
- Device resetting and triggering additional control functions used in testing and commissioning
- Change device mode as required for testing and operation
- Enter a password to login according to different access rights for settings and operations

Control is also possible through the PC interface. This requires a suitable PC installed with a specific operating program called the PowerLogic Engineering Suite (see Using the PowerLogic Engineering Suite, page 131).

Using the HMI

The PowerLogic P7 can be equipped with a user-friendly front panel.

Figure 62 - Front panel of the PowerLogic P7



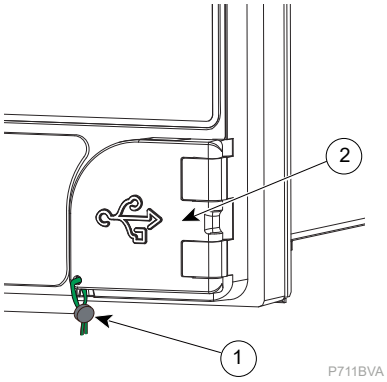
1	7” graphical color touchscreen display	5	Reference label
2	Power ON/OFF LED ON Alarm LED ① Trip LED Maintenance LED	6	Mini-USB port
3	Home button	7	USB-A port (currently unavailable)
4	Reset button	8	USB door

USB ports

USB ports	Function
Mini-USB port	For PC connection to access the PowerLogic Engineering Suite
USB-A port	For data transfer (currently unavailable)

In order to help prevent unauthorized access to the USB ports on the front panel of the PowerLogic P7, the USB cover can be locked with a wired lead seal.

Figure 63 - Lock the USB cover



① Wired lead seal

② USB cover

Push buttons

Symbol	Function
	Press **Home** button to cancel an operation or return to the home page.
	Press **Reset** button to release latched signals, outputs, alarms and LEDs.

LED indicators

Physical LEDs on the front panel

The PowerLogic P7 has four LEDs on the front panel representing the status of the PowerLogic P7 regarding power, alarm, trip, and operation mode.

Table 24 - The states of the physical LEDs on the front panel

LED	States		
	ON	OFF	Flash
ON	Safe mode Factory reset Normal operation mode Degraded operation mode Test/Test blocked mode Upgrade	-	Start-up
ⓘ	Viewed alarm	Start-up Safe mode	Unread alarm
⚡	Trip	Start-up Safe mode	-
🔧	Start-up Safe mode Degraded operation mode Upgrade	Factory reset Normal operation mode	Test/Test blocked mode

Physical LEDs on the CPU board

The PowerLogic P7 has four physical LEDs on the CPU board to indicate its current working states.

LED	States		
	OFF	ON	Flash
ON	OFF	ON	Maintenance
A3	Port 3 link down	Port 3 link up	Port 3 activity
ⓘ	No alarm	New alarm	Test mode/Test blocked
A2	Port 2 link down	Port 2 link up	Port 2 activity

Configurable virtual LEDs

Press the virtual LED icon in the upper right corner of the touchscreen display, the virtual LED list configured for the device is displayed. The icon includes an indication of the number of active virtual LEDs to remind users when an LED is **ON**.

NOTE: The LED can be colored in both the **ON** and **OFF** states. The number in the virtual LED icon indicates of number of LED with ON status.

Once any virtual LED status is changed, the LED side bar comes down from the top right side of the touchscreen display for 2 seconds. Tapping the side bar will open the virtual LED list page.

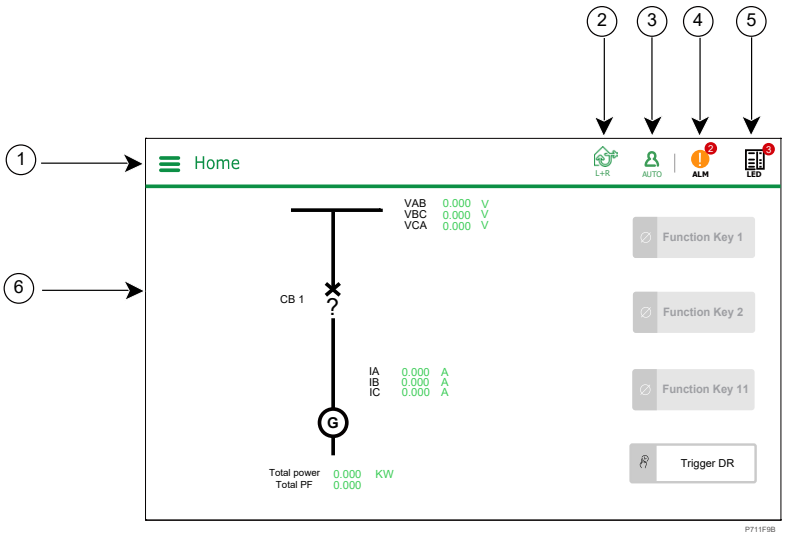
The virtual LED page will be displayed if the trip LED is **ON**. If the display has timed out (is blank), it will turn on and display the virtual LED page. If the display is active when the trip LED turns on, the display will switch to the virtual LED page after the timeout period or a maximum of 15 minutes. When the trip LED is reset, the display will time out if not being used.

To configure the virtual LEDs, see Configuring virtual LEDs (*LEDIHMI*), page 136.

Touch screen

The home page of the touch screen consists of two parts: the top bar and the Mimic view area.

Figure 64 - Home page



1	Menu icon: tap it to expand the subpage navigation list.	4	Alarm icon: tap it to check all alarm status. The bubble number on the icon indicates the number of active alarms.
2	Remote/Local/Local+Remote mode icon: indicates that the device is in Remote control mode or Local control mode, or Local and Remote control mode. This is for the control mode of switchgear.	5	Virtual LED icon: tap it to check all virtual LED status. The bubble number on the icon indicates the number of operated LEDs with colors.
3	Login/Auto login/Logout icon: indicates the login/auto login/logout status.	6	Mimic view: the mimic is user customizable. It contains a single line diagram, function keys, measurements and other elements which are configured in PowerLogic Engineering Suite.

NOTE: For the labels of LED, BI, alarm or device name displayed on HMI, the maximum length is 32 characters. If the label configured exceeds the maximum length, only the first 32 characters will be displayed on HMI.

When the device is in operation mode, press **Home** button to go to the home page. Tap the menu icon to expand the subpage navigation list to go to a specific subpage.

NOTE: To refresh the **Log** page for the updated information on this page, switch to another page and then return to **Log** page.

Login and logout

For more details about the password management and the user level, see relevant sections in Cybersecurity, page 94.

Login

Login is required before changing settings or accessing the data protected by the Role Based Access Control (RBAC) mechanism.

NOTE: In the default RBAC, the HMI is set to auto-login. This can be deactivated by CAE if required.

The login screen can be accessed by tapping the icon on the top bar of the home page. The login procedure is as follows:

1. Tap the icon to enter the User Login page.
2. Enter the username and password by the physical keyboard or the pop-up soft keypad.
3. Tap the **Login**.

   NOTE: After a correct password is entered, the icon turns to green. The view and edit capability of settings depends on the access rights of the selected user and the role managed by the RBAC.

Logout

It is possible to log out manually by pressing the green icon and then selecting **Log out** option from the drop-down menu.

Localization

Setting device language

The PowerLogic P7 supports the following device languages:

- English (Default)
- French
- Chinese
- German
- Spanish
- Polish

To set the device language:

- From the HMI menu, tap **General > System info > Settings**. From the **Device language** drop-down, select the required language and tap **Confirm**.
- From the PowerLogic Engineering Suite, click **General > System info**. From the **Device language** drop-down, select the required language and click **Confirm**.

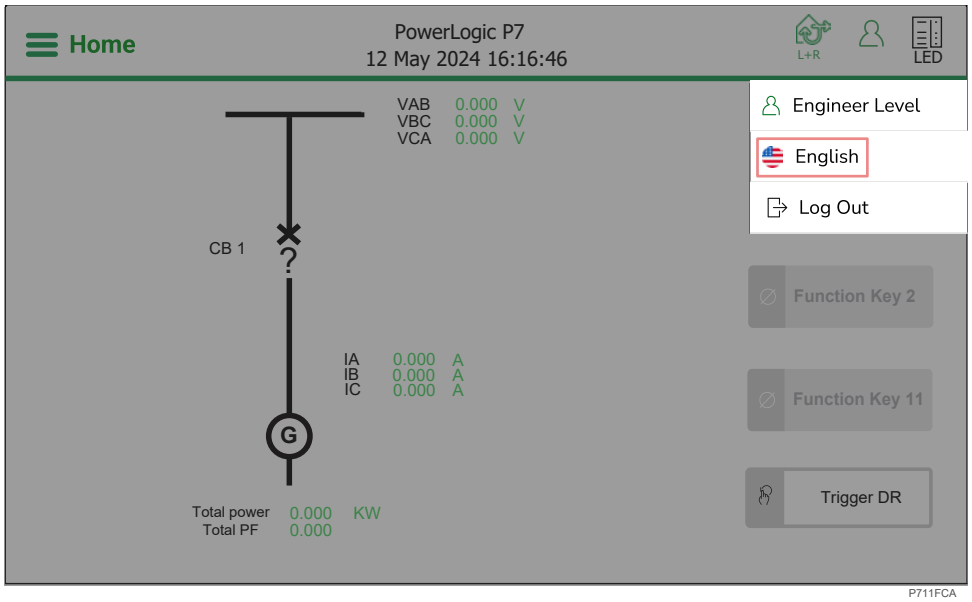
Setting session language

Within the device login page, the user can change the HMI language that only applies to the current session. Once the current session expires after inactivity or the user manually logs out, the HMI resets back to the configured language.

NOTE: The session lifetime can be changed with the **Minimum inactivity period (min)** setting in the CAE.

The session language can be changed regardless of user login status. To change the session language, tap on the HMI home page. From the language drop-down, select the required session language and tap **Confirm**.

Figure 65 - Session language selection after logging in



Changing settings

To change the data of settings with the front panel:

1. Navigate to the desired setting page from the front panel.
2. Select the parameter field you want to change.
3. Enter the value with the pop-up keypad or select the value from the drop-down menu.
4. Confirm the change operation.

   NOTE: On the right side of the pop-up keypad, the maximum, the minimum and the step values of this parameter are listed. If the entered value is beyond the range, an information box will pop up.

Adjusting screen settings

To adjust the LCD settings of the PowerLogic P7:

- From the HMI, expand ☰ **> General > Device config > HMI > Setting** and set the screen backlight or screen timeout.
- From the PowerLogic Engineering Suite, expand **Device configuration > HMI > Basic info** and set the screen backlight or screen timeout.

Managing alarms

Checking and resetting the alarm message

Check the alarm LED ⓘ status on the front panel or the alarm icon ALM 2 on the top bar of the device HMI to see if any alarm is triggered. Once an alarm occurs, the alarm LED lights up and at the same time, the alarm icon status changes. The number next to the alarm icon represents the number of alarms.

To check the alarm messages:

- Tap ALM 2 to access the **Alarm List** page to view the alarm name, occurrence time and detailed information.

To reset all alarms:

- Tap **Reset all** from the **Alarm List** page.

To reset single alarm:

- Tap **R** on the single alarm row from the **Alarm List** page.

After performing reset operation, the alarm icon will disappear and alarm LED will turn off.

Using the PowerLogic Engineering Suite

Overview

⚠WARNING

UNINTENDED EQUIPMENT OPERATION

Make sure that the modification of setting parameters with reboot of the PowerLogic P7 has no impact on people and equipment.

Failure to follow these instructions can result in death, serious injury, or equipment damage.

The PowerLogic Engineering Suite is an engineering tool for configuring the PowerLogic P7 devices, local operation and customized functions. The Engineering Suite is supplied directly through the Schneider Electric website www.se.com.

The Engineering Suite has a graphical interface where the PowerLogic P7 settings and parameters are grouped under different menu tabs. The contents of the menu tabs depend on the device type and the selected application mode. Refer to the user manual of the PowerLogic Engineering Suite for detailed information on the setting views of each menu tab.

The Engineering Suite stores the device configuration in a setting file.

When starting to work with the Engineering Suite, there are three options:

- Create a new setting file without connecting to the PowerLogic P7.
- Open an existing (previously saved) setting file without connecting to the PowerLogic P7.
- Connect to the PowerLogic P7 and read the settings from the device.

The Engineering Suite can be connected to a single device via the mini-USB port on the device front panel or to a group of devices via remote access over Ethernet connection.

Connection modes

The PowerLogic Engineering Suite software can be used in three modes:

- Offline
- Front port connection
- Network connection

Using offline PowerLogic Engineering Suite

This allows users to prepare configuration and setting parameter files for PowerLogic P7 devices prior to commissioning.

When PowerLogic Engineering Suite is offline, you can create a configuration and setting file from scratch or open a previously saved configuration or setting file as a basis for further modification for a PowerLogic P7 of the same type. Refer to PowerLogic Engineering Suite User manual for more information.

Using PowerLogic Engineering Suite with a front panel connection

The front panel connection can be used during commissioning of a PowerLogic P7:

- To upload (write), download (read), and modify device configuration and setting parameter files.

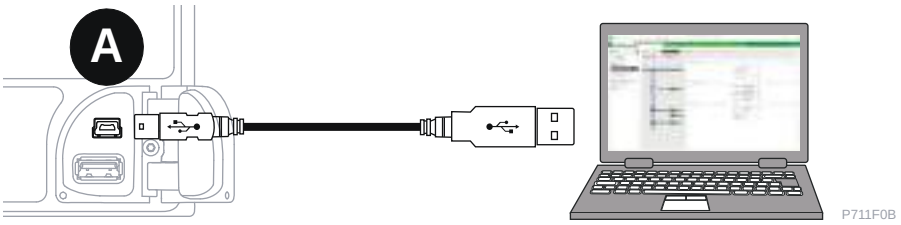
Refer to the User Manual of PowerLogic Engineering Suite for more information on uploading (writing) / downloading (reading) configuration and setting parameter files to/from the connected devices.

NOTICE
UNINTENDED EQUIPMENT OPERATION AND NUISANCE TRIPPING After writing new firmware, configurations or settings to a protection and control device, perform a test to verify that the protection and control device operates correctly with the updated parameters. **Failure to follow these instructions can result in unwanted shutdown of the electrical installation.**

The PC fitted with the PowerLogic Engineering Suite is connected to the PowerLogic P7 by using the mini-USB port on the front panel.

NOTICE
UNINTENDED EQUIPMENT OPERATION Use the mini-USB port for connecting with a PC only. Do not use the mini-USB port for other purpose. **Failure to follow these instructions can result in equipment damage.**

Figure 66 - The connection between a PowerLogic P7 and a PC



A mini-USB (PC connection)

Using PowerLogic Engineering Suite with a network connection

The network connection can be used during operation of a PowerLogic P7:

- To manage the protection system.
- To check the status of the electrical network.
- To do a network fault analysis after a protection event.

The connection window allows configuration of the PowerLogic P7 network and provides access to the configuration and setting parameters of the protection and control application of the PowerLogic P7 units on the network.

The PC fitted with the PowerLogic Engineering Suite can be connected to a group of PowerLogic P7 units via Ethernet communication network. The Ethernet port used on the PowerLogic P7 must allow access to web services. Any new configuration sent to this port must also allow web services to ensure Engineering Suite can still access the device.

Setting up the connection

Connecting to the device

Connecting to the device using the mini-USB cable

1. Plug the mini-USB cable into the front panel port.

   A box **Authentication required** pops up after the PowerLogic Engineering Suite detects the connection.
2. Enter the username and the password.
3. Click **Authenticate**.

   NOTE: If it is the first time to use the default user and password on the connected device, refer to Cybersecurity, page 94.
4. Click **Configure** to start configuring the connected device. After several minutes, a site view window with device information is displayed.

NOTE: The IP address of the mini-USB is *90.0.0.1* and this IP is fixed.

Connecting to the device via Ethernet

To connect to a device or multiple devices via Ethernet:

1. Log in the PowerLogic Engineering Suite software.
2. On the home page, click **Connect to devices**.
3. From the pop-up **Connect to devices** window, select one of the following connect types from the drop-down list.
   - Ethernet Network
   - Serial Connection
   - Modem Connection
4. Configure other options if required.
5. Select **Multiple devices**.
6. Click **Next >**.

   After several minutes, **Connection successful** is displayed for each device in the **Progress** column from **Connect to multiple device** window.
7. Click **Configure** to start configuring connected devices.

   After several minutes, a site view window is displayed to show multiple devices information.

Displaying live data from the device

To display device live data on the PowerLogic Engineering Suite:

1. Click 《 at the top right corner.
2. If the device is connected, go to Step 3, page 133.

   If the device is not connected, click **Connect to device** and finish the device connection process.
3. Click **Display live data** .

Device information

The PowerLogic Engineering Suite will provide the device information for the connected device.

NOTE: You can use this function to verify that the correct device is connected.

- **Device nameplate**

  The device information, such as device name**,** product code, serial number, can be viewed under **General > System info**.

- **HMI information**

  The HMI application version can be viewed under **Device configuration > HMI > Basic info**.

- **Board information**

  The board information, such as board type, hardware version, FPGA version, can be viewed under **Device configuration > Slot # > Basic info**.

Synchronizing parameters

Reading settings from the device to database

The device and the PowerLogic Engineering Suite must be in connected status.

1. From the PowerLogic Engineering Suite, click **Synchronize Parameters** on the main header bar.

   If a pop-up **Unsaved changes** dialog appears:

   - Click **OK** to continue.
   - Click **Cancel** to quit.

2. From the pop-up **Choose synchronization settings** dialog, select **From Device to Project Database**.

3. Select one of the available options for reading settings.

Option	Description
Full configuration	To read all settings from device to project database. **NOTE:** Your database content will be replaced.
Changes (n)	To read only detected changes from device to project database. **NOTE:** (n) represents the number of detected changes in your device.

4. Click **Start Synch** to proceed or **Cancel** to exit.

   After synchronization, one of the following three results will be available.

Option	Description
Synchronized	The synchronization for reading settings is successful.
Partially synchronized	The synchronization for reading settings is partially successful. Click **View details** for details.
Synchronization failed	The synchronization for reading settings is failed. Click **Open logs** for details.

5. Click **OK**.

Writing settings from project database to device

The device and the PowerLogic Engineering Suite must be in connected status.

1. Change the settings from the PowerLogic Engineering Suite.

   The changed setting values will be highlighted in blue.

2. Click **Save Working Copy** to save the modifications.
3. Click **Synchronize Parameters**.
4. From the pop-up **Choose synchronization settings** dialog, select **From Project Database to Device**.
5. Select one of the available options for writing settings.

Option	Description
Full configuration	To write all settings from project database to device. **NOTE:** This requires device reboot. During the reboot, the connection between the PowerLogic Engineering Suite and the device will be automatically disconnected.
Changes (n)	To write only detected changes from project database to device. **NOTE:** (n) represents the number of detected changes in your database.

6. Click **Start Synch**.

   After synchronization, one of the following three results will be available.

Option	Description
Synchronized	The synchronization for writing settings is successful. The device will reboot automatically.
Partially synchronized	The synchronization for writing settings is partially successful. Click **View details** for details.
Synchronization failed	The synchronization for writing settings is failed. Click **Open logs** for details.

7. Click **OK**.

Engineering

Configuring virtual LEDs (*LEDIHMI*)

To configure the virtual LEDs with the PowerLogic Engineering Suite:

1. Expand **Device configuration > LED > Configuration**.
2. Define respectively the label name, ON color, OFF color, and behavior of each virtual LED.

The LED behavior can be set to *Latch* or *Flashing*. If the behavior of an LED is set to *Latch*, to reset the LED status, press R button on the front panel of the device.

The 24 virtual LEDs can be configured in four different colors: red, yellow, green or gray, and can be individually latched or unlatched. The virtual LEDs are configured by default as follows:

Table 25 - LED1 to LED24 on Motor, Generator, Feeder, and Transformer applications

LEDs	Green	Red	Yellow	Latch	Flashing
LED 1		Phase A		TRUE	FALSE
LED 2		Phase B		TRUE	FALSE
LED 3		Phase C		TRUE	FALSE
LED 4		Neutral		TRUE	FALSE
LED 5		Overcurrent		TRUE	FALSE
LED 6		Voltage		TRUE	FALSE
LED 7		Frequency		TRUE	FALSE
LED 8		Power		TRUE	FALSE
LED 9		Impedance		TRUE	FALSE
LED 10		Temperature		TRUE	FALSE
LED 11		Motor/Generator/Feeder/ Transformer		TRUE	FALSE
LED 12		Coil alarm		FALSE	FALSE
LED 13				TRUE	FALSE
LED 14				TRUE	FALSE
LED 15				TRUE	FALSE
LED 16				TRUE	FALSE
LED 17				TRUE	FALSE
LED 18				TRUE	FALSE
LED 19				TRUE	FALSE
LED 20				TRUE	FALSE
LED 21				TRUE	FALSE
LED 22				TRUE	FALSE
LED 23		DR start		FALSE	FALSE
LED 24				TRUE	FALSE

LED matrix

The LED matrix defines how the virtual LEDs are linked to signals. The input of LED status is configured by the matrix. Multiple signals can be configured as one LED's input. Dedicated signals can be taken with an inverted status, multiple assigned signals are taken in OR logic, the LED shows the related logical result.

Input and output signals

Table 26 - Status of the *LEDIHMI*

Name	Short label	Infotip
LED1	LED1 status	LED1 status
.....	.....	.....
LED24	LED24 status	LED24 status

Table 27 - Control of the *LEDIHMI*

Name	Short label	Infotip
LEDAllRst	Reset all LEDs	Reset all LEDs
LEDRst	Reset	Reset LED

Configuring system time

The date and time can be configured with the HMI or with the PowerLogic Engineering Suite.

Setting local time

To configure local time:

- From the HMI, expand ☰ **> General > System clock > Date and time**, set the **Enable local time** as *True* and enter the offset value in **Time offset from UTC** field to adjust the local time based on UTC time.
- From the PowerLogic Engineering Suite, expand **General > System clock**, select **Enable local time** and enter the offset value in **Time offset from UTC** field to adjust the local time based on UTC time.

  NOTE: Time zone offset (or bias) is to adjust the protection relay's local time. The offset can be set as a Positive (+) or Negative (-) value within a range of -720 to +840 minutes with a resolution of 15 minutes.

Setting daylight saving time (DST)

The PowerLogic P7 provides automatic daylight saving time or summer time adjustments when configured. The automatic daylight time adjustments can be configured when the DST is enabled.

By default, the time on the device is UTC (24-hour clock) and DST is disabled. When the DST is enabled, the initial DST rule is as follows:

- Daylight saving time starts: 02:00 am on the last Sunday of March
- Daylight saving time ends: 03:00 am on the last Sunday of October

To configure the automatic daylight time adjustments:

- From the HMI, expand ☰ **> General > System clock > Date and time**, set the **Enable local time** and the **Enable DST** as *True*.
- From the PowerLogic Engineering Suite, expand **General > System clock**, select **Enable local time** and **Enable DST**.

  NOTE: Enable DST can adjust clocks by one hour only.

Coordinating time settings

If the time and date is not being maintained by an IRIG-B, SNTP or PTP time source, set the date and time to the correct value manually in **Date and time** page. Be aware that the unsynchronized internal clock will have a small drift against the real time, which requires to correct the internal time in a cyclic way to keep all devices of a substation on track. Some SCADA communications (e.g. Modbus or DNP3) can also synchronize the device time by regularly updating the date and time.

Parameters

Table 28 - Settings of the *LTIM*

Name	Short label	Infotip	Setting range	Step size	Default setting
TmLocTmEna	Enable local timezone	Enable local timezone	• Off • On		On
TmOfsTmm	Time offset from UTC	Time offset from UTC	-720...840 min	15 min	0 min
TmUseDT	Enable DST	Enable daylight savings time	• true • false		false
DSTBgnWk	DST begin week	DST begin week	• First • Second • Third • Fourth • Last		Last
DSTBgnMon	DST begin month	DST begin month	• January • February • March • April • May • June • July • August • September • October • November • December		March
DSTBgnDay	DST begin day	DST begin day	• Monday • Tuesday • Wednesday • Thursday • Friday • Saturday • Sunday		Sunday
DSTBgnHr	DST begin hour	DST begin hour	0...24	1	2
DSTEndWk	DST end week	DST end week	• First • Second • Third • Fourth • Last		Last
DSTEndMon	DST end month	DST end month	• January • February • March • April • May		October

Table 28 - Settings of the *LTIM* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
			• June • July • August • September • October • November • December		
DSTEndDay	DST end day	DST end day	• Monday • Tuesday • Wednesday • Thursday • Friday • Saturday • Sunday		Sunday
DSTEndHr	DST end hour	DST end hour	0...24	1	3

Configuring time synchronization

The internal clock in the PowerLogic P7 is used to time-stamp events and disturbance recordings. The system clock should be externally synchronized to get comparable event time stamps for all the protection relays in the system.

The synchronization is based on the difference of the internal time and the synchronizing message or pulse. This deviation is filtered and the internal time is gradually corrected towards a zero deviation.

Checking time synchronization status

To check the status of time synchronization:

- From the HMI, expand ☰ **> General > System clock > Time source > Status**.

Setting time source

To change the time source parameters:

- From the HMI, expand ☰ **> General > System clock > Time source > Settings**.
- From the PowerLogic Engineering Suite, expand **General > System clock**.

Figure 67 - Time source configuration on the PowerLogic Engineering Suite



NOTE: *Main time source* and *Backup time source* are read-only from the HMI and can only be modified from the PowerLogic Engineering Suite. The time source can be set as *1588*, *IRIG-B*, or a valid SNTP server IP address.

Synchronization source

The internal system time of the PowerLogic P7 can be synchronized with configured time source. The supported time sources are IRIG-B, PTP (IEEE 1588) or SNTP.

NOTE: If the device is configured to publish or subscribe to Sampled Values, only PTP or IRIG-B time sources can be used.

- **Synchronization source PTP (1588)**

  Precision Time Protocol (PTP) communication is based on the IEEE 802.3 protocol. The PTP time synchronization can be configured on either of the two Ethernet interfaces. For the PowerLogic P7, PTP can work under Failover, PRP and HSR mode, but not under RSTP mode. Additionally, the PowerLogic P7 supports Transparent Clocking (TC) in HSR mode. PTP provides higher time accuracy (1 µs).

  PTP implementation is compliant with IEC 61850-9-3 and IEEE 1588v2/IEC 61588.
  Peer-to-peer mode and Best Master Clock algorithm (BMCA) are supported.

- **Synchronization source IRIG-B**

  IRIG-B synchronization is supported by the IRIG-B module connected to the device. The supported code formats are B122, B123, B126, and B127. Note that for B123 and B127, Straight Binary Seconds (SBS) is not decoded and used by the PowerLogic P7. The IRIG-B time must be local time if local time is enabled.

- **Synchronization source SNTP**

  Simple Network Time Protocol (SNTP) is used to synchronize the clocks of computer systems over packet-switched, variable-latency data networks. A jitter buffer is used to reduce the effects of variable latency introduced by queuing in packet switched networks, helping ensure a continuous data stream over the network. The PowerLogic P7 receives the synchronization from the SNTP server by using the SNTP server IP address. The device supports the configuration of two SNTP server IP addresses.

If the *Main time source* is configured as *1588* or *IRIG-B*, and the *Backup time source* is configured as *SNTP*, the device will try to synchronize with the main time source as it is powered on. The device will try with backup time source if the signal of main time source is lost. When the backup time source is working, the device will periodically check the status of main time source and switch to the main time source once it detects a valid signal from the main time source.

If none of the time sources is configured, or none of the IRIG-B, PTP and SNTP signals is valid, the device will synchronize with communication protocols like Modbus or DNP3 with a reduced accuracy.

Table 29 - Time source accuracy

Time source	Accuracy
PTP	Class T5, 1 µs.
IRIG-B	Class T1, 5 µs.
SNTP	Class T1, 1 ms. (single hop to SNTP server)
Communication channel	Class T0, 8 ms.

Deviation

The time deviation means how much the system clock time differs from the synchronization source time. The time deviation is calculated after receiving a new synchronizing message. The filtered deviation means how much the system clock was really adjusted. Filtering takes care of small deviation in synchronizing messages.

Parameters

Table 30 - Status of the *LTMS*

Name	Short label	Infotip
TmSrc	Active time source	Active time source
TmSrcTyp	Active source type	Active source type
TmSyn	Active sync type	Active sync type
TmChSt1	Main clock status	Main clock status
TmChSt2	Backup clock status	Backup clock status
IRIGBStat	IRIG-B status	IRIG-B status
PTPStat	PTP status	PTP status
OsFromMstr	Offset from master	Offset from master
PrMnPDly	Peer mean path delay	Peer mean path delay
StpsMvd	Steps removed	Steps removed
PrntClkId	Parent clock Id	Parent clock Id
PrntClkCls	Parent clock class	Parent clock class
PrntClkAcc	Parent clock accuracy	Parent clock accuracy
PrntClkVar	Parent clock variation	Parent clock variation
PrntPri1	Parent clock priority 1	Parent clock priority 1
PrntPri2	Parent clock priority 2	Parent clock priority 2

Table 31 - Settings of the *LTMS*

Name	Short label	Infotip	Setting range	Step size	Default setting
TmSrcSet1	Main time source	Must be 1588 or IRIG-B or SNTP IP address (e.g. 192.168.0.0). Any other text will disable this source			1588
TmSrcSet2	Backup time source	Must be 1588 or IRIG-B or SNTP IP address (e.g. 192.168.0.0). Any other text will disable this source			1588 or IRIG-B or SNTP IP
DomainNum	PTP domain number	Precision time protocol (1588) domain number	0...255	1	0
IntrfNo	PTP Ethernet interface	Selects which interface is used for PTP time sync	• Redundant Ethernet		Single Ethernet

Table 31 - Settings of the *LTMS* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
			• Single Ethernet		
PTPVlanId	PTP VLAN ID	PTP VLAN ID	0...4094	1	0
PdelInterv	PTP path delay interval	Time between PTP delay request messages	0...5	1	1

Configuring alarms

To configure the alarm parameters with the PowerLogic Engineering Suite:

1. Expand **Device configuration > Alarm > Alarm configuration**.
2. Define the label name and the latch mode of individual alarms.

   NOTE: If the latched mode is enabled, the alarm must be reset manually; otherwise, the alarm will reset automatically.

Alarm matrix

Map signals to activate alarms by the alarm matrix. The PowerLogic P7 supports a maximum of 128 alarms. Signals can be filtered by standard or IEC 61850 name and signal inversion is allowed.

Controlling objects

The PowerLogic P7 has the Mimic view on the home page of the HMI. Tap the symbol of the object like circuit breakers and ground switches on the Mimic view or navigate to the **Control** menu to find the options to open or close the objects.

The PowerLogic P7 supports three control models.

- Status only
- Direct with normal security
- SBO with enhanced security

To control objects or to change the control model for objects depends on the privilege of the user logged in. The controlling features can be configured with the PowerLogic Engineering Suite. See CB and switch control (*CBCSWI*/*SWCSWI*), page 368 for the parameters of CB and switch control function.

To control objects with Select Before Operate (SBO) control or direct control on the HMI:

1. Tap the symbol of the object on the Mimic view or expand ☰ **> Control > Bay1** to locate to the object (for example, CB 1).
2. Navigate to **Control**.
3. From the **Status** tab, tap ✎ in the **Position** field.
4. Select | or ○ from the pop-up window.

   The result varies between SBO control model and direct control mode:

   - SBO control model: Tap **Confirm** or **Cancel** from the pop-up window, and the control to the object is performed or canceled.
   - Direct control model: The control to the object is performed without further confirmation.

Configuring binary outputs (LPDO)

Description

Binary outputs are available for control and signaling purposes.

The number of available outputs is six on the MIO module. The MIO module can be fitted to slot D/E/F/G. The location depends on the configuration ordered. TIO board is fixed to slot Y, it contains 8 BIs and 8 BOs, and 2 of 8 BOs are on the PSU board in slot Z.

The following binary output contact relays are used by default in slot Y, Z:

- **Slot Y**

  The binary output BO1 is used for trip and CB open.

  The binary output BO2 is used for CB close.

  The binary output BO3 is used for CBF (CB failure).

- **Slot Z**

  The binary output BO7 is used for trip and CB open.

  The binary output BO8 is used for CB close.

  The watchdog relay is used for device supervision.

The outputs on other MIO modules can be flexibly used and set for signal or control as required by default. The allocation of the contacts on the other boards is also flexible using the matrix.

To view the status of the binary outputs:

- From the HMI, expand ☰ **> General > Device Config > Slot #** and select the **BO status** tab.
- From the PowerLogic Engineering Suite, expand **Device configuration > Slot # > Binary outputs**.

The status of binary outputs can also be viewed by the SCADA system via different protocols.

Force control for BO

The force control for BO function is to test the contact of the binary output.

NOTE: This function is only available when the mode of logic device (LD0) containing the binary outputs is in *Test-blocked* mode which will disable processing of all inputs.

When switched to this mode, all the physical outputs will be open and the latch function will not work.

To enable the force control on binary outputs:

1. From the HMI, expand ☰ **> Control > Device mode**.
2. From the **Device mode** tab, tap ✎ in the **Device mode** field.
3. Select *Test-blocked* from the drop-down to set the device to *Test-blocked* mode.
4. Expand ☰ **> General > Device config > Slot #**.
5. From the **BO status** tab, tap ✎ in the **BOx** field or the **Force all BO** field
6. Select *On* to enable the force function for one or all binary outputs.

   NOTE: The BOx input will be *True* if the corresponding binary output is set to *On*.

Configuring binary outputs with the PowerLogic Engineering Suite

Any internal signal can be connected to the output relays using the output matrix in the PowerLogic Engineering Suite. An output relay can be configured as latched or non-latched with the PowerLogic Engineering Suite under **Device configuration > Slot # > Binary outputs**.

Setting parameters

Table 32 - Settings of the T1LPDO

Name	Short label	Infotip	Setting range	Step size	Default setting
LatchCh1	BO1 latch	BO1 latch	• Off • On		Off
Ind1Lab	BO1 label	BO1 label			BO1

NOTE: When the binary output is latched, the value will keep *1* or *True*. This status can only be changed by **Reset** button or a SCADA reset command.

Configuring binary inputs (LPDI)

Binary inputs are available for control purposes. For example, the binary inputs can provide the position of the circuit breaker block/enable/disable functions, trigger a programmable logic, and indicate a function or object status.

The number of available inputs depends on the number of ordered module options. There are eight available inputs on each MIO module.

The binary inputs require an external control voltage (AC or DC) and are activated after the voltage exceeds the pick-up threshold. Deactivation follows when the voltage drops below the drop-off threshold limit.

To view the status of the binary inputs:

- From the HMI, expand ☰ **> General > Device config > Slot # > BI status**.

The status of binary inputs can also be read by the SCADA system via different protocols.

Configuring binary inputs with the PowerLogic Engineering Suite

The binary inputs are set with the PowerLogic Engineering Suite under **Device configuration > Binary inputs**.

When the **BI common setting** is *ON*, the auxiliary supply range of all standard binary inputs on the module will be set as the same as BI1/BI2. Special binary inputs such as BI7/BI8 in speed mode and TCS binary inputs always have independent settings.

The settable items include:

- Auxiliary supply range (Not used/24V DC/48V DC/110V DC/220V DC/220V AC/TCS)

  NOTE: The nominal voltage pickup for TCS is 19 V with no inrush and a constant current of 1 mA.

- Pick-up ratio

  The available range is from 40% to 80% based on the input voltage.

- Drop-off ratio

  The available range is from 50% to 90% based on the pick-up voltage.
- Filter time

Applying a time over 10 ms makes the input operation immune to AC induction on long DC circuits. If a faster response is required, external burden should be added to the circuit.

Timing diagram of a binary input during pick-up, page 145 and Timing diagram of a binary input during a drop-off, page 145 below illustrate the timing diagrams of a binary input during pick-up and drop-off:

Figure 68 - Timing diagram of a binary input during pick-up

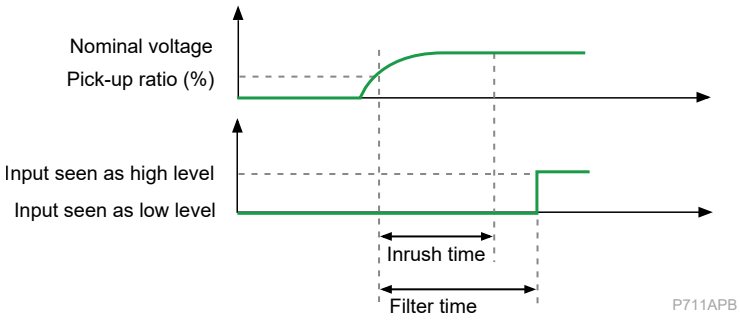
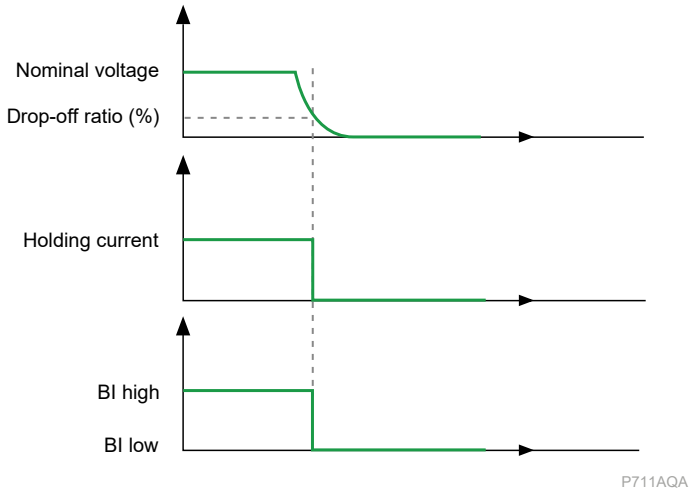


Figure 69 - Timing diagram of a binary input during a drop-off



Setting parameters

Table 33 - Settings of the T1LPDI

Name	Short label	Infotip	Setting range	Step size	Default setting
SpeedMod	Speed input	When speed is required the pulse input must be connected to the selected input (BI7 or BI8). The other input is then not used	• Off • BI7 • BI8		Off
BroadCastMod	BI common setting	Applies the same settings to all binary inputs. If speed is enabled it is excluded from common settings	• Off • On		On
Ch1Ch2VTyp	BI1/BI2 type	BI1/BI2 type	• Not used • 24V DC • 48V DC • 110V DC • 220V DC • 220V AC		24V DC

Table 33 - Settings of the T1LPDI (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
			• TCS		
Ch1Ch2PiPct	BI1/BI2 pickup ratio	BI1/BI2 pickup ratio	40...80 %	1 %	70 %
Ch1Ch2DrPct	BI1/BI2 dropoff ratio	BI1/BI2 dropoff ratio	50...90 %	1 %	90 %
Ch1Ch2Filter	BI1/BI2 filter delay	BI1/BI2 filter time delay	0.02...100 ms	0.02 ms	1 ms
Ch3Ch4VTyp	BI3/BI4 type	BI3/BI4 type	• Not used • 24V DC • 48V DC • 110V DC • 220V DC • 220V AC • TCS		24V DC
Ch3Ch4PiPct	BI3/BI4 pickup ratio	BI3/BI4 pickup ratio	40...80 %	1 %	70 %
Ch3Ch4DrPct	BI3/BI4 dropoff ratio	BI3/BI4 dropoff ratio	50...90 %	1 %	90 %
Ch3Ch4Filter	BI3/BI4 filter delay	BI3/BI4 filter time delay	0.02...100 ms	0.02 ms	1 ms
Ch5Ch6VTyp	BI5/BI6 type	BI5/BI6 type	• Not used • 24V DC • 48V DC • 110V DC • 220V DC • 220V AC • TCS		24V DC
Ch5Ch6PiPct	BI5/BI6 pickup ratio	BI5/BI6 pickup ratio	40...80 %	1 %	70 %
Ch5Ch6DrPct	BI5/BI6 dropoff ratio	BI5/BI6 dropoff ratio	50...90 %	1 %	90 %
Ch5Ch6Filter	BI5/BI6 filter delay	BI5/BI6 filter time delay	0.02...100 ms	0.02 ms	1 ms
Ch7Ch8VTyp	BI7/BI8 type	BI7/BI8 type	• Not used • 24V DC • 48V DC • 110V DC • 220V DC • 220V AC • TCS		24V DC
Ch7Ch8PiPct	BI7/BI8 pickup ratio	BI7/BI8 pickup ratio	40...80 %	1 %	70 %
Ch7Ch8DrPct	BI7/BI8 dropoff ratio	BI7/BI8 dropoff ratio	50...90 %	1 %	90 %
Ch7Ch8Filter	BI7/BI8 filter delay	BI7/BI8 filter time delay	0.02...100 ms	0.02 ms	1 ms
TcsVTyp	TCS type	Trip Circuit Supervision (TCS) input type. Normally set TCS to operate on a fixed current with 19V nominal. For non TCS application choose the nominal voltage	• Not used • 24V DC • 48V DC • 110V DC • 220V DC • 220V AC • TCS		TCS
TcsPiPct	TCS pickup ratio	TCS pickup ratio	40...80 %	1 %	70 %
TcsDrPct	TCS dropoff ratio	TCS dropoff ratio	50...90 %	1 %	90 %
TcsFilter	TCS filter delay	TCS filter time delay	0.02...100 ms	0.02 ms	1 ms

NOTE:

- *Pick-up voltage* = *pick-up ratio* x *nominal voltage*
- *Drop-off voltage* = *drop-off ratio* x *pick-up voltage*

Table 34 - Settings of the T2LPDI

Name	Short label	Infotip	Setting range	Step size	Default setting
BroadCastMod	BI common setting	Applies the same settings to all binary inputs. If speed is enabled it is excluded from common settings	• Off • On		On
Ch1Ch2VTyp	BI1/BI2 type	BI1/BI2 type	• Not used • 24V DC • 48V DC • 110V DC • 220V DC • 220V AC • TCS		24V DC
Ch1Ch2PiPct	BI1/BI2 pickup ratio	BI1/BI2 pickup ratio	40...80 %	1 %	70 %
Ch1Ch2DrPct	BI1/BI2 dropoff ratio	BI1/BI2 dropoff ratio	50...90 %	1 %	90 %
Ch1Ch2Filter	BI1/BI2 filter delay	BI1/BI2 filter time delay	0.02...100 ms	0.02 ms	1 ms
Ch3Ch4VTyp	BI3/BI4 type	BI3/BI4 type	• Not used • 24V DC • 48V DC • 110V DC • 220V DC • 220V AC • TCS		24V DC
Ch3Ch4PiPct	BI3/BI4 pickup ratio	BI3/BI4 pickup ratio	40...80 %	1 %	70 %
Ch3Ch4DrPct	BI3/BI4 dropoff ratio	BI3/BI4 dropoff ratio	50...90 %	1 %	90 %
Ch3Ch4Filter	BI3/BI4 filter delay	BI3/BI4 filter time delay	0.02...100 ms	0.02 ms	1 ms
Ch5Ch6VTyp	BI5/BI6 type	BI5/BI6 type	• Not used • 24V DC • 48V DC • 110V DC • 220V DC • 220V AC • TCS		24V DC
Ch5Ch6PiPct	BI5/BI6 pickup ratio	BI5/BI6 pickup ratio	40...80 %	1 %	70 %
Ch5Ch6DrPct	BI5/BI6 dropoff ratio	BI5/BI6 dropoff ratio	50...90 %	1 %	90 %
Ch5Ch6Filter	BI5/BI6 filter delay	BI5/BI6 filter time delay	0.02...100 ms	0.02 ms	1 ms
Ch7Ch8VTyp	BI7/BI8 type	BI7/BI8 type	• Not used • 24V DC • 48V DC • 110V DC • 220V DC • 220V AC • TCS		24V DC
Ch7Ch8PiPct	BI7/BI8 pickup ratio	BI7/BI8 pickup ratio	40...80 %	1 %	70 %
Ch7Ch8DrPct	BI7/BI8 dropoff ratio	BI7/BI8 dropoff ratio	50...90 %	1 %	90 %
Ch7Ch8Filter	BI7/BI8 filter delay	BI7/BI8 filter time delay	0.02...100 ms	0.02 ms	1 ms

Table 35 - Settings of the T3LPDI

Name	Short label	Infotip	Setting range	Step size	Default setting
BroadCastMod	BI common setting	BI common setting	• Off • On		On
Ch1Ch2VTyp	BI1/BI2 type	BI1/BI2 type	• Not used		24V DC

Table 35 - Settings of the T3LPDI (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
			• 24V DC • 48V DC • 110V DC • 220V DC • 220V AC • TCS		
Ch1Ch2PiPct	BI1/BI2 pickup ratio	BI1/BI2 pickup ratio	40...80 %	1 %	70 %
Ch1Ch2DrPct	BI1/BI2 dropoff ratio	BI1/BI2 dropoff ratio	50...90 %	1 %	90 %
Ch1Ch2Filter	BI1/BI2 filter delay	BI1/BI2 filter time delay	0.02...100 ms	0.02 ms	1 ms
Ch3Ch4VTyp	BI3/BI4 type	BI3/BI4 type	• Not used • 24V DC • 48V DC • 110V DC • 220V DC • 220V AC • TCS		24V DC
Ch3Ch4PiPct	BI3/BI4 pickup ratio	BI3/BI4 pickup ratio	40...80 %	1 %	70 %
Ch3Ch4DrPct	BI3/BI4 dropoff ratio	BI3/BI4 dropoff ratio	50...90 %	1 %	90 %
Ch3Ch4Filter	BI3/BI4 filter delay	BI3/BI4 filter time delay	0.02...100 ms	0.02 ms	1 ms
Ch5Ch6VTyp	BI5/BI6 type	BI5/BI6 type	• Not used • 24V DC • 48V DC • 110V DC • 220V DC • 220V AC • TCS		24V DC
Ch5Ch6PiPct	BI5/BI6 pickup ratio	BI5/BI6 pickup ratio	40...80 %	1 %	70 %
Ch5Ch6DrPct	BI5/BI6 dropoff ratio	BI5/BI6 dropoff ratio	50...90 %	1 %	90 %
Ch5Ch6Filter	BI5/BI6 filter delay	BI5/BI6 filter time delay	0.02...100 ms	0.02 ms	1 ms
Ch7VTyp	BI7 type	BI7 type	• Not used • 24V DC • 48V DC • 110V DC • 220V DC • 220V AC • TCS		24V DC
Ch7PiPct	BI7 pickup ratio	BI7 pickup ratio	40...80 %	1 %	70 %
Ch7DrPct	BI7 dropoff ratio	BI7 dropoff ratio	50...90 %	1 %	90 %
Ch7Filter	BI7 filter delay	BI7 filter time delay	0.02...100 ms	0.02 ms	1 ms

Configuring control inputs

The control inputs function as software switches that can be set or reset either locally or remotely. These inputs can be used to trigger any function that they are connected to via the FSL or matrix.

In the PowerLogic P7, there are 64 control inputs in total.

The mode of the control inputs can be configured with the PowerLogic Engineering Suite under **Device control > Control inputs**. The control inputs can be configured as either **Latched** or **Pulse** mode:

- A latched control input will remain in the set state until a reset command is given.
- A pulsed control input will remain energized for the configurable pulse duration after the set command is given and will then reset automatically (i.e. no reset command required).

Configuring function keys

The PowerLogic P7 provides 12 function keys for programming any operator control functionality via fast scheme logic or matrix. These function keys can be used to trigger any function that they are connected to as part of the fast scheme logic or matrix.

To select the function keys with front panel:

1. Expand ☰ **> Control > Function keys**.
2. From the **Function keys** page, select the desired **Function key**.

   NOTE: In case of two keys pressed at the same time, only one key works and the other is time out.

Two control models are available for each function key:

- Direct control model - The function key with direct control model has the direct control icon showing the finger with clock.

  NOTE: For the function key with direct control model, the key should be pressed and held on the key for at least 500 milliseconds so as to prevent the inadvertent key presses.
- SBO control model - The function key with SBO control model has the two-step icon showing the finger with touch.

The function key has three kinds of mode:

- Pulse mode - In this mode, the function key output remains *high* as long as the key is pressed, and then be reset automatically after the key press is released.

  NOTE: The pulse can be detected by the receiving application function by the pulse duration. A minimum pulse duration is **1 s**.
- Toggle mode - In this mode, a single keypress will set or latch the function key output as *high* or *low* in fast scheme logic and the signal will be mapped via the matrix on the PowerLogic P7 as well. This feature can be used to enable or disable the relay functions.
- Disable mode - In this mode, the function key is disabled.

  NOTE: Mode setting is used to allow the key to be disabled.

Matrix

Description

The PowerLogic P7 protection and control device has a flexible structure that supports a virtually infinite number of configurations. To fulfill the protection scheme’s needs, different parts of this structure can be linked (i.e. physical and network I/Os, protection functions, custom logic equations, front panel I/Os).

Each part can emit and receive signals. Those signals from one function can be mapped to another using routing matrices.

The PowerLogic P7 has several matrices that are used for linking the hardware and software elements together to create a protection chain:

- **BO matrix**

  It is used to link various signals to the contact relays. See Configuring binary outputs (LPDO), page 143.
- **LED matrix**

  It is used to control virtual LEDs. See Configuring virtual LEDs (*LEDIHMI*), page 136.
- **Alarm matrix**

  It is used to link various signals to activate alarms. See Configuring alarms, page 142.
- **CT/VT matrix**

  It is used to link hardware channels in CT/VT board with virtual channels in CT/VT group. CT/VT matrix is for current and voltage mapping. See CT/VT matrix, page 347.
- **Protection matrix**

  See Protection matrix, page 156.
- **Protection trip matrix**

  It is used to link the combination of all protection functions' start outputs and operate outputs to a general start and a general operate. See Trip conditioner matrix, page 424.
- **Bay dead matrix**

  It is used to monitor all CB positions in the bay. See Bay dead matrix, page 446.
- **Interlocking matrix**

  It is used to inhibit the CB and ground switch control. See Interlocking matrix, page 373.
- **Disturbance record matrix**

  It is used to trigger the disturbance record. See Disturbance record triggering matrix, page 413.

Matrix processing for test bit

Table 36 - Matrix process for test bit

Matrix process for test bit		Receiving function	
		ON	Test/Test- Blocked
Input	Valid, Test=1	Invalid	Valid
	Valid, Test=0	Valid	Valid
	Invalid, Test=0/1	Invalid	Invalid

NOTE: As the matrix is not within a LN or LD, the BEH should be inherited from the LN that owns the output from the matrix, If the function is *ON*, then the gate should consider the input signals with the test flag set as invalid. If the function is *Test* or *Test-blocked*, then the test bit of the input data can be ignored.

Configuring signal routing

To configure signal routing in PowerLogic Engineering Suite.

1. Expand a function and select the related mapping you want to configure within the function configuration.

   The matrix is displayed in the **Setting** view.

   NOTE: The available sources are arranged in rows and the available destinations are arranged in columns.

2. Click **IEC 61850** or **Standard** to change the mapping to **IEC 61850** view or **Standard** view.

   NOTE: The **IEC 61850** view indicates the IEC 61850 name and the data type for the sources. At the Logical Node (LN) level, data type indicates the type of LN.

3. Select the **Routed signals only** check box if you want to list the routed signals only in the mapping.
4. Select the **Expand/collapse top level** check box if you want to expand or collapse signal top level. This allows the detailed view of the data attribute mapping to be displayed for complex data objects.
5. Select a signal and click on the cell in white to link the signal to the appropriate output from the matrix. This displays a tick symbol (√) in the cell.

   NOTE: Inputs and outputs can be expanded by selecting the arrows next to the source and destination. This allows linking at the main signal (data object) or sub signal (data attribute) level or selection of specific states for enumerated values.

6. Optionally, click the cell again to deselect the signal. This removes the tick symbol.
7. Optionally, right-click the cell with the tick and select **Invert** option to invert the signal from the matrix.
8. Optionally, right-click the output destination and select **Invert** option to invert the matrix outputs which feed into function inputs. This displays a line on the top of the outputs.

Mimic

Home page editor

The HMI home page consists of the top bar and the mimic panel. The mimic panel is constructed by placing different symbols together with the PowerLogic Engineering Suite.

NOTE: Multiple mimic panels can be set up with the PowerLogic Engineering Suite. Once set up and synchronized with the device, the user can switch to a different mimic panel by horizontally scrolling the current one on the HMI home page.

Two types of symbols are available (on home page) for the mimic panel:

- **widgets**: General elements for the operator interface.
  - Control: Function key
  - Measurements: Single measurement and gauges
  - Status: Annunciator
  - Text: Static label
  - Shapes: Ellipse, rectangle and static line
- **SLD**: Elements used for SLD diagram. They are organized into libraries such as busbars, switchgear, plant and sensors. Symbols include ANSI, IEC and electrical drawing symbols.

Adding and configuring symbols

To configure the symbols with the PowerLogic Engineering Suite:

1. Navigate to **Device configuration > Mimic**.
2. From the **Mimic editor** page, click in **Mimic** tool bar or click **Edit** at the bottom of the page.
3. From the **Home page editor** page, select **SLD symbols** or **widgets** from the **Add** drop-down.
4. Drag the selected symbol to canvas sheet.

   Up to four fields are displayed in the left panel according to the symbol type.

   - General: includes **Name** and **Description** to be defined.
   - Status: provides the configuration for the signals to be mapped. It is only available for some certain symbols for data binding to implement the mapping between the symbols and signals. This allows the presentation of the information to be adapted according to the data within the device. (For example, the position of the switchgear or value of a measurement).

     NOTE: Some SLD symbols can be mapped with one or two signals, and some SLD symbols or widgets have no signals.
   - States preview: indicates the status and colors based on the values of the status signals.

     NOTE: A pop-up menu appears when clicking the SLD symbols under the **Status preview** panel. The color of SLD symbols can be customized from this menu.
   - Colors preview: This field appears only when a measurement widget is selected. Within this field, the widget color can be customized based on the range and quality of the measured signal.
5. Type text in **Name** and **Description** fields.
6. Optionally, for symbols of which status are available for data binding, click from the **Status** field.
7. Optionally, from the pop-up **Select status signals** window, click the signals from the selection table to map the selected symbol.
8. Optionally, click **Select** to complete the data binding. A path with selected signal is displayed in the **Status** field.
9. Optionally, from the **States preview** field, click the symbol in each state and select the color you want. This customizes the color of the SLD object within the different states.

Blocking remote settings

Settings on the PowerLogic P7 can be changed locally or remotely:

- Local: Settings made on the HMI, or the PowerLogic Engineering Suite connected through the mini-USB or DHMI ports. Local settings cannot be blocked.
- Remote: Settings made on the PowerLogic Engineering Suite or IEC 61850 clients connected through PORT 1-3. Remote settings can be remotely or locally blocked, but can only be unblocked locally.

To block remote settings:

- From the HMI, expand **Menu > General > System into > Settings**, and select **On** from the **PLES setting block/IEC 61850 setting block** drop-downs.
- From the PowerLogic Engineering Suite, expand **General > System info**, and select **On** from the **PLES setting block/IEC 61850 setting block** drop-downs.

- From an IEC 61850 client, change the related parameter values and write to the device.

  NOTE: To unblock remote settings, select **Off** with the same paths above on the HMI or locally connected PowerLogic Engineering Suite.

Configuring fast scheme logic

The PowerLogic P7 supports user-defined programmable logic for boolean and enumerated signals. User-defined logic can be used to create functionality that is not provided by the device as a pre-defined function.

The fast scheme logic can be viewed or modified via the PowerLogic Engineering Suite:

- Expand **Device control > Fast scheme logic**.

The following table provides the number of the available logic gates for each logic gate type in total:

Table 37 - Available logic functions

Logic gate type	Number of gates reserved
OR	1000
NOT	1000
AND	1000
XOR	1000
TIMER	256
RS	128
Fast TIMER	32

Logic timer

Logic timer provides the possibility of assigning a freely configurable time characteristic to the output signal of each Boolean equation.

Three modes of the timer are available for logic timer:

- *Pickup*
- *Dropoff*
- *Pickup + dropoff*

Two types of the timer are available for logic timer:

- *TIMER*
- *FAST TIMER*

Logic gates

Tables below show the pre-defined resulting gate logic outputs of the fast scheme logic, for example, with binary input A, input B and the quality status.

NOTE: Quality **Questionable** is treated as **Valid** regardless of its detailed quality.

Table 38 - Logic output results for gate OR

Logic equation for gate OR		Gate input A		
		True-Valid	False-Valid	False/True-Invalid
Gate input B	True-Valid	True-Valid	True-Valid	True-Valid
	False-Valid	True-Valid	False-Valid	False-Invalid
	True/False-Invalid	True-Valid	False-Invalid	False-Invalid

Table 39 - Logic output results for gate AND

Logic equation for gate AND		Gate input A		
		True-Valid	False-Valid	False/True-Invalid
Gate input B	True-Valid	True-Valid	False-Valid	False-Invalid
	False-Valid	False-Valid	False-Valid	False-Valid
	True/False-Invalid	False-Invalid	False-Valid	False-Invalid

Table 40 - Logic output results for gate XOR

Logic equation for gate XOR		Gate input A		
		True-Valid	False-Valid	False/True-Invalid
Gate input B	True-Valid	False-Valid	True-Valid	False-Invalid
	False-Valid	True-Valid	False-Valid	False-Invalid
	True/False-Invalid	False-Invalid	False-Invalid	False-Invalid

Table 41 - Logic output results for gate NOT

Gate input	Gate output
True-Valid	False-Valid
False-Valid	True-Valid
True/False-Invalid	False-Invalid

Table 42 - Logic output results for gate RS (Reset dominant mode)

Logic equation for gate RS		Gate reset		
		True-Valid	False-Valid	False/True-Invalid
Gate set	True-Valid	False-Valid	True-Valid	Output is not updated.
	False-Valid	False-Valid	Output is not updated.	Output is not updated.
	True/False-Invalid	False-Valid	Output is not updated.	Output is not updated.

Table 43 - Logic output results for gate SR(Set dominant mode)

Logic equation for gate SR		Gate reset		
		True-Valid	False-Valid	False/True-Invalid
Gate set	True-Valid	True-Valid	True-Valid	True-Valid
	False-Valid	False-Valid	Output is not updated.	Output is not updated.
	True/False-Invalid	Output is not updated.	Output is not updated.	Output is not updated.

NOTE: The inputs of the logic gates should be connected. Care must be taken when using logic outputs as logic inputs. Toggling feedback loops must be avoided. If a bay is placed into test mode without placing the device in test mode, the input will be seen as invalid which may cause the output to become invalid. If this signal is fed back, it may create a situation where the logic is permanently invalid even after disabling test mode.

FSL processing for test bit

Table 44 - Fast scheme logic process for test bit

Fast scheme logic process for test bit		Logic model mode	
		ON	Test/Test- Blocked
Input	Valid, Test=1	Invalid	Valid
	Valid, Test=0	Valid	Valid
	Invalid, Test=0/1	Invalid	Invalid

NOTE: For fast scheme logic, if LN node LMODELGAPC1's BEH is *ON*, inputs whose QUALITY.TEST is set will be treated as invalid. If LN node LMODELGAPC1's BEH is *Test/Test Blocked*, the test bit of the input data can be ignored.

Logic gate input and output inversion

The inputs and outputs of the logic gates can be inverted via the PowerLogic Engineering Suite:

1. Expand **Device control > Fast scheme logic**.
2. Click **Edit** to enter **Logic editor** page.
3. Double-click or drag the gate symbols from the logic gate drop-down list into the canvas to add them.
4. Right-click the gate on the canvas.
5. Enter the number in **Inverted inputs** to set the number of the input you want to invert.
6. Turn on **Invert output** toggle button if you want to invert the logic gate output.

   NOTE: The logic gate input and output inversion function is not applicable to **NOT** gate.

Protection functions

General features

Setting groups

Setting groups are controlled by the HMI or the communication client.

For each protection stage, eight setting groups are available. Each setting group can be used for eight various applications. Functions such as trip conditioning, breaker fail, and pole dead are constant for all applications and a single stage is provided.

Switching the setting groups

To switch the setting groups from the HMI:

1. Press **Home** button.
2. Expand ☰ **> Control > Bay 1 > Setting groups**.
3. Tap **Active group** from the **Setting groups** tab.
4. Select the desired group number from the pop-up window to activate the setting group.

Enabling the protection functions

The different protection function can be enabled or disabled individually in different setting groups.

- With the HMI
  1. Expand ☰ **> Protection > Bay 1** to locate to the desired protection function.
  2. Select the desired stage.
  3. From the **Settings** tab, tap **Group** field at the top right corner.
  4. Select the desired group from the **Group** drop-down.
  5. Select **On** from the **Function status** drop-down to enable the protection with the desired stage.
- With the PowerLogic Engineering Suite
  1. Expand **Bay 1 protection** to locate to the desired protection function.
  2. Select **On** from the **Function status** drop-down to enable the protection in the specific setting group.

Protection matrix

Functions like Selective Overcurrent Logic must interact with the protection functions to adapt the timing and threshold constraints. It must be determined which function should be linked with the dynamic input (Dyn).

Functions like Inrush Detection (ID) must interact with the protection functions to dynamically block the related protection stage(s). For example, when the inhibit signal (Inh) is linked with ID function, the protection will be blocked. From the matrix of a specific protection, link the output signal of the ID function to the inhibit signal of the protection.

The binary inputs or GOOSE signals also can be linked to the dynamic input or block signals of protection functions.

Under protection matrix, configure the input signals of Inhibit, Op block, Block and Hold for each protection respectively according to actual requirements.

Operation modes of the logical device

LD0 represents the physical PowerLogic P7 and contains the client access points.

LD0 has three modes:

- ON
- Test
- Test/Blocked

The PowerLogic P7 mode affects all the functions of the device, not only all the functions under the LD0, but also the functions under the BayLD.

Each PowerLogic P7 offers one bay, which has a separate mode under the BayLD (Logical Device of a bay). The mode of the BayLD represents the mode of the entire bay and has four options:

- ON
- Test
- Test/Blocked
- OFF

The bay mode affects all the functions under the bay. These functions are used to ensure the normal operation of this bay, i.e., the protection function and the measurement function.

Quality

The current application function considers the validity of each input signal and manages the behavior accordingly if the input is *invalid*. The behavior is to block the function or let the function operate if the signals are less critical.

NOTE: When the quality is *questionable*, the application will execute the normal logic, except for blocking the output.

It also considers the Test bit as follows:

- When the receiving application function is in **ON** state, any data received with the test bit set to *True* is treated as *invalid*.
- When the receiving application function is in **Test** state or **Test/Blocked** state, the test flag of the received data is not taken into consideration for the input validity.

  NOTE: Functions with physical outputs, for example, LPDO will block all inputs when they have **Test/Blocked** state.

When the application function is in **OFF** state, the binary output will be reset to default value, and the analog output will be reset to zero.

- Quality will be set to *invalid* for each output signal in **OFF** state.

Timer

There are up to four matrix inputs which have common behavior for all protection functions in which they are used.

- Inhibit input (**Inh**)
- Timer block input (**TmBlk**)
- Timer hold input (**TmHld**)
- Operate block input (**OpBlk**)

Inh, when asserted, will result in the protection function being held in a reset condition with internal timers and latches reset and outputs set to default values. It will also result in a block output being asserted.

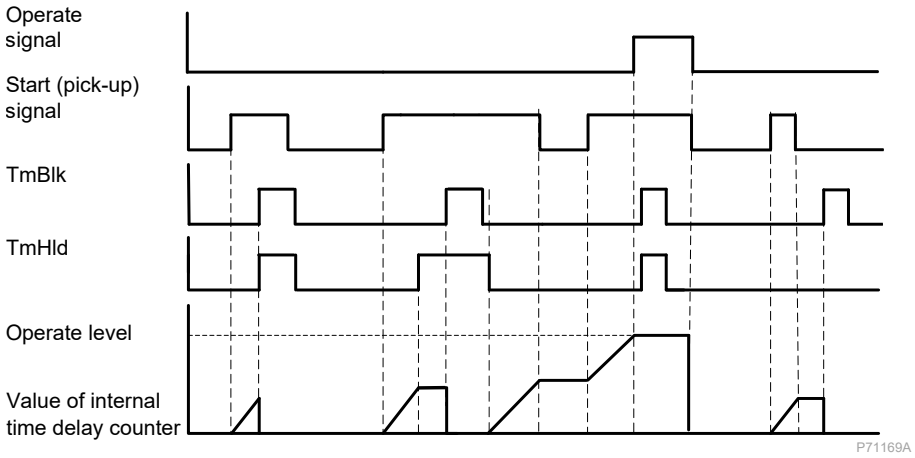
TmBlk, when asserted, will result in the timer function being reset to zero.

TmHld, when asserted, will result in the timer function being frozen at the value that it had reached at the instant that the **Hold** input became asserted.

> **NOTE: TmBlk** has priority over **TmHld**, if both these inputs are simultaneously asserted the timer function will be reset to zero, see figure below.

OpBlk, when asserted together with start output, will prevent the operate output from being asserted, no matter whether the timer has elapsed or not.

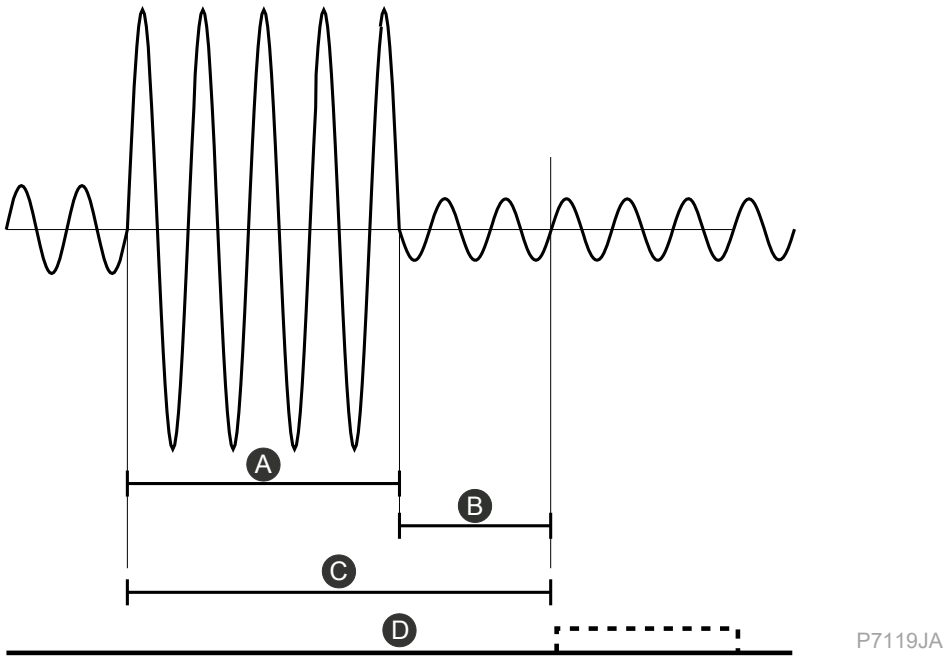
Figure 70 - Behavior of timer block and timer hold



Overshoot time

Overshoot time is the time the protection and control devices need to notice that a fault has been cleared during the operate time. This characteristic is important when grading the operate time settings between the devices.

Figure 71 - Definition for overshoot time



A	Fault time	B	Overshoot time (≤ 50 ms)
C	Operate time configuration, have to be greater than the sum of fault time and overshoot time.	D	Trip contacts

For example, when there is a heavy fault in an outgoing feeder, it will start both the incoming and outgoing feeder protection and control devices. However, the fault must be cleared by the outgoing feeder protection and control device and the incoming feeder protection and control device must not trip. Although the operating delay setting of the incoming feeder is more than that of the outgoing feeder, the incoming feeder might still trip if the operate time difference is not big enough. The difference must be more than the overshoot time of the incoming feeder protection and control device plus the operate time of the outgoing feeder circuit breaker.

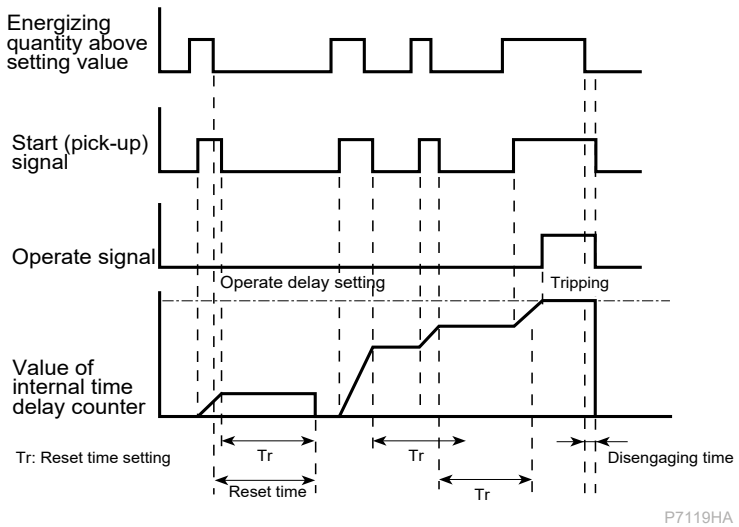
Definition for overshoot time, page 158 shows an overcurrent fault seen by the incoming feeder when the outgoing feeder clears the fault. If the operation delay setting would be slightly shorter or if the fault duration would be slightly longer than in the figure, an unselective trip might happen (the dashed 40 ms pulse in the figure). In PowerLogic P7, the overshoot time is less than 50 ms.

Disengaging time and reset time

The disengaging time is the time between the moment when the fault conditions disappear and the moment the tripping contact relay opens.

According to IEC 60255-151 standard, Disengaging time and adjustable reset time, page 159 shows an example of disengaging time, that is, release delay when the PowerLogic P7 is clearing an overcurrent fault. When the trip contacts of the PowerLogic P7 are closed, the Circuit Breaker (CB) starts to open. After the CB contacts are open, the fault current still flows through an arc between the opened contacts. The current is finally cut off when the arc extinguishes at the next zero crossing of the current. This is the start moment of the disengaging delay and the trip start contacts are opened unless dwell or latching is configured. The precise disengaging time depends on the fault size; after a significant fault, the disengaging time is longer. The disengaging time also depends on the specific protection stage. The maximum disengaging time for each stage is specified under the characteristics of every protection function.

Figure 72 - Disengaging time and adjustable reset time



The adjustable reset time is a definite or inverse time hold used mainly to detect restriking faults (DT) or allow coordination with electromechanical devices (Inverse). The adjustable reset time is inhibited if the element operates.

Physical contact operate time and reset time

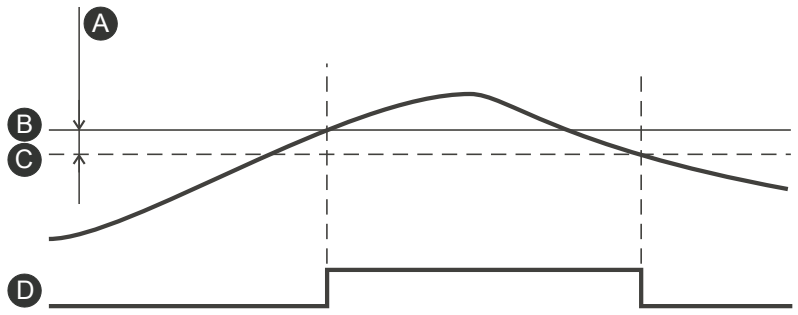
Performance from the characteristic table of each protection in this chapter is based on the function without the delay caused by the physical contact or GOOSE transmission.

From hardware aspect, the relay contact operate time is 4 ms and the reset time is 5 ms.

Hysteresis and reset ratio

When comparing a measured value against a start value, some amount of hysteresis is needed to avoid oscillation near equilibrium situation. With zero hysteresis, any noise in the measured signal or any noise in the measurement itself would cause unwanted oscillation between fault-on and fault-off situations.

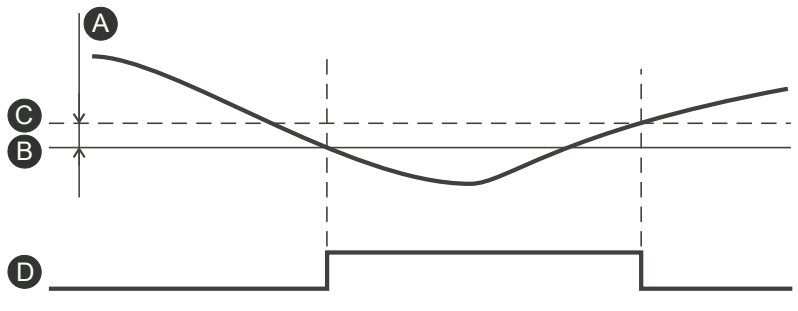
Figure 73 - Example of behavior of an over-protection with hysteresis



A	Hysteresis	B	Start level
C	Reset level	D	Start

The reset ratio is the ratio between the reset level and the start level. To avoid any chattering of the protection for low settings of thresholds, a reset ratio can be claimed with a minimum value of hysteresis. For example: < 93% with a minimum of hysteresis of 0.005 I_n.

Figure 74 - Example of behavior of an under-protection with hysteresis



A	Hysteresis	B	Start level
C	Reset level	D	Start

CT requirements

NOTICE
IMPROPER EQUIPMENT OPERATION Select the CT size according to the requirement from the electrical network. **Failure to follow these instructions can result in improper operation.**

The PowerLogic P7 standard current inputs can be connected to standard 1 A or 5 A CTs. The core balance CT can only be connected to a 1 A secondary.

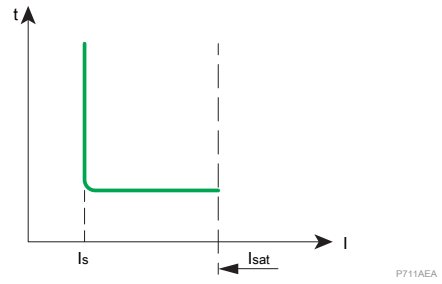
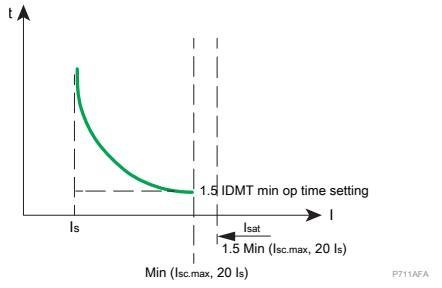
Sizing rules of line CTs can be specific for each function and depend on which function is being considered:

- Phase overcurrent (*PHPTOC*, ANSI 50/51)
- Ground fault overcurrent (*EFPTOC*, ANSI 50N/51N)
- Sensitive ground fault overcurrent (*VSEFPTOC*, ANSI 50SG/51SG)
- Biased differential protection (*PHPDIF*, ANSI 87)
- High impedance differential (*HIZPDIF*, ANSI 87/64REF)

General overcurrent protection

The CT must be sized to avoid saturation during steady state short circuit currents where accuracy is required, according to the rules described below for DT or IDMT operation.

The condition to be fulfilled by the CT saturation current (I_{sat}) depends on the type of overcurrent protection operation time:

Time Delay	Condition to be Fulfilled	Illustration
DT	I_{sat} > 1.5 x set point (Is)	
IDMT	I_{sat} > 1.5 x the smallest of the following values: • $I_{sc.max}$, maximum installation short-circuit current • 20 x Is (IDMT curve dynamic range) • > 1.5 x the IDMT min op time setting equivalent current setting	

The method for calculating the saturation current depends on the CT accuracy class.

Converting an IEC 185 CT standard protection classification to a kneepoint voltage

The suitability of an IEC standard protection class CT can be checked against the kneepoint voltage requirements specified previously.

For example, if the available CTs have a 15 VA 5P 10 designation, then an estimated kneepoint voltage can be obtained as follows:

$V_k = (VA \times ALF)/I_n + ALF \times I_n \times R_{CT}$

Where:
V_k = Required kneepoint voltage
VA = Current transformer rated burden (VA)
ALF = Accuracy limit factor
I_n = Current transformer secondary rated current (A)
R_{CT} = Resistance of current transformer secondary winding (Ω)

If R_{ct} is not available, then the second term in the above equation can be ignored.

Example: 400/5A, 15 VA 5P 10, R_{CT} = 0.2 Ω

$V_k = 15 \times 10/5 + 10 \times 5 \times 0.2$

Converting an IEC 185 CT standard protection classification to an ANSI/IEEE standard voltage rating

The PowerLogic P7 is compatible with ANSI/IEEE CTs as specified in the IEEE C57.13 standard. The applicable class for protection is class **C**, which specifies a non air-gapped core. The CT design is identical to IEC class **P**/**PX**, or British Standard class **X**, but the rating is specified differently.

The ANSI/IEEE **C** Class standard voltage rating required will be lower than an IEC knee point voltage. This is because the ANSI/IEEE voltage rating is defined in terms of useful output voltage at the terminals of the CT, whereas the IEC knee point voltage includes the voltage drop across the internal resistance of the CT secondary winding added to the useful output. The IEC/BS knee point is also typically 5% higher than the ANSI/IEEE knee point. Therefore:

V_c = (V_k - Internal voltage drop)/1.05 = (V_k - $I_n \times R_{CT}$ x ALF)/1.05
Where
V_c = **C** Class standard voltage rating
V_k = IEC Knee point voltage required
In = CT rated current = 5 A in USA
R_{CT} = CT secondary winding resistance
(for 5 A CTs, the typical resistance is 0.002 ohms/secondary turn)
ALF = The CT accuracy limit factor,
the rated dynamic current output of a **C** class CT (Kssc) is always 20 ×In

The IEC accuracy limit factor is identical to the 20 times secondary current ANSI/IEEE rating. Therefore:
$V_c = (V_k - 100 \times R_{CT})/1.05$

Calculating the saturation current in class P

A class P CT is characterized by:

- $I_{.prim.nom}$: Rated primary current (in A)
- $I_{.sec.nom}$: Rated secondary current (in A)
- Accuracy class, expressed by a percentage, 5P or 10P, followed by the Accuracy-Limit Factor (ALF), whose usual values are 5, 10, 15, 20, 30
- VA_{CT}: Rated burden, whose usual values are 2.5/5/7.5/10/15/30 VA
- R_{CT}: Resistance of the secondary winding (in Ω)

The installation is characterized by the burden resistance R_b at the CT secondary (wiring + protection relay). If the CT load complies with the rated burden, i.e. $R_{b.nom} \times I_{sec.nom}^2 = VA_{CT}$, the saturation current is equal to $I_{sat} = ALF \times I_{prim.nom}$.

If the CT winding resistance R_{CT} is known, it is possible to calculate the actual CT ALF, which takes account of the actual CT load. The saturation current then equals actual ALF × $I_{prim.nom}$, where:

$$\text{Actual ALF} = ALF \times \frac{R_{CT} \times I_{sec.nom}^2 + VA_{CT}}{(R_{CT} + R_b) \times I_{sec.nom}^2}$$

E71172A

Hence if the actual CT load is less than its nominal burden ($R_{b.act} < R_{b.nom}$), a higher short-circuit current can be transmitted without saturation.

Example:

A CT with the following characteristics is given:

- Transformation ratio: 100 A / 5 A
- Accuracy class and accuracy limit factor: 5P20
- Rated burden: 2.5 VA
- Resistance of the secondary winding: 0.1 Ω

To get an ALF of at least 20, i.e. a saturation current of 20 x $I_{prim.nom}$ = 2 kA, the load resistance R_b of the CT must be less than:

$$R_{b,max} = \frac{VA_{CT}}{I_{sec.nom}^2} = 0.1\ \Omega$$

E71173A

This represents 12 m (39 ft) of wire with cross-section 2.5 mm² (AWG 14) for a resistance per unit length of 8 mΩ/m (2.4 mΩ/ft) approximately.

For an installation with 50 m (164 ft) of wiring with section 2.5 mm² (AWG 14), the actual resistance is R_b = 0.4 Ω, and hence actual ALF is:

$$\text{Actual ALF} = ALF \times \frac{R_{CT} \times I_{sec.nom}^2 + VA_{CT}}{(R_{CT} + R_b) \times I_{sec.nom}^2} = \frac{0.1 \times 25 + 2.5}{(0.1 + 0.4) \times 25} = 8$$

E71174A

Therefore, the saturation current for this CT installation is:
$I_{sat} = 8\ x\ I_{prim.nom}$ = 800 A.

NOTE: The actual CT burden R_b connected on its secondary side is given as follows:

- For phase-to-ground faults: $R_b = 2\ R_W + R_{rel}$
- For phase-to-phase faults: $R_b = R_W + R_{rel}$

Where the wire lead burden is calculated as:

$$R_W = \rho \times \frac{l}{A}$$

E71159A

with ρ = specific conductor resistance, for example, for copper 0.021 Ω mm²/m at 75°C

l = wire length in [m]

A = wire cross section in [mm²]

The impedance of the PowerLogic P7 current inputs (R_{rel} = 4 mΩ) is often negligible compared to the wiring resistance.

Calculating the saturation current in class PX

A class PX CT is characterized by:

- $I._{prim.nom}$: Rated primary current (in A).
- $I._{sec.nom}$: Rated secondary current (in A).

- V_k: Rated knee-point voltage (in V).
- R_{CT}: Maximum resistance of the secondary winding (in Ω).

The saturation current is calculated by the load resistance R_b at the CT secondary (wiring + device):

$$I_{sat} = \frac{V_k}{R_{ct} + R_b} \times \frac{Inp}{Ins}$$ E71175A

Table 45 - Examples:

CT Transformation Ratio	V_k	R_{ct}	R_b	Saturation current
100 A/5 A	17.4 V	0.13 Ω	0.4 Ω	$I_{sat} = \frac{17.4}{0.13 + 0.4} \times \frac{Inp}{5} = 6.56 \times Inp = 656\ A$ E71176A
100 A/1 A	87.7 V	3.5 Ω	0.4 Ω	$I_{sat} = \frac{87.7}{3.5 + 0.4} \times \frac{Inp}{1} = 22.48 \times Inp = 2248\ A$ E71177A

Biased differential protection

ALF > 0.875 × K_r × K_{ssc}, minimum 25
K_r = remanence factor = 1 / (1 - remanence flux(pu))
$K_{ssc} = I_{psc} / I_{pr}$

- I_{psc}: Rated primary through short-circuit current
- I_{pr}: Rated primary current

This formula is based on using the default slope settings (K1, K2 and Slope 2 pickup). The saturation time constant should be set above the system time constant for stability with any CT type.

The worst-case remanence factor is usually assumed to be 4 (75% remanent flux) for high remanence CTs (5P, PX). A lower remanence determined in accordance with IEC 61869-2 can also be used.

High impedance differential protection

The current transformer requirements for phase faults with peak-to-peak measurement mode are:

$V_s = I_f \times (R_{CT} + 2R_L)$
$R_s = V_s / Is_1$
$V_K \geq 2\ V_s$
Where:
R_s = Value of stabilizing resistor (ohms)
I_f = Maximum secondary through fault current level (amps)
V_K = CT knee point voltage (volts)
I_{S1} = Current setting of differential element (secondary amps)
R_{CT} = Resistance of current transformer secondary winding (ohms)
R_L = Resistance of a single lead from relay to current transformer (ohms)
V_s = Stability voltage

Transformer differential protection

ALF > 0.875 × K_r × K_{ssc}, minimum 17.5
K_r = remanence factor = 1 / (1 - remanence flux(pu))
$K_{ssc} = I_{psc} / I_{pr}$

- I_{psc}: Rated primary short-circuit current
- I_{pr}: Rated primary current

This formula is based on using the default slope settings (K1, K2 and Slope 2 pickup).

The worst-case remanence factor is usually assumed to be 4 (75% remanent flux) for high remanence CTs (5P, PX). A lower remanence determined in accordance with IEC 61869-2 can also be used.

Core balanced CTs

Unlike a line CT, the rated primary current for a core balanced current transformer may not be equal to the load. This has been considered in the formula:

$V_K = 6 \times N \times In \times (R_{CT} + 2R_L + R_r)$
Where:
V_k = Minimum CT kneepoint voltage for through fault stability
In = Relay rated current
N = Ground fault current/Core balanced CT rated primary current
R_{CT} = Resistance of CT secondary winding (Ω)
R_L = Resistance of a single lead from relay to CT (Ω)
R_r = Resistance of any other protective relays sharing the CT (Ω)

NOTE: N should not be greater than 2. The core balance CT ratio should be selected accordingly. Requirements based on FFT measurement mode.

Independent and dependent characteristics

Description

The relationship between operate delay and characteristic quantity can be expressed by two types of characteristics:

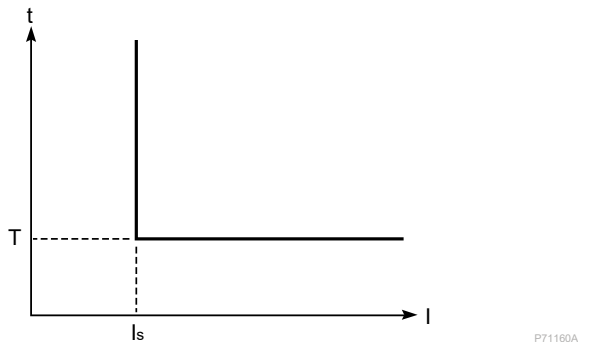
- Independent time characteristic (i.e. definite time delay)
- Dependent time characteristic (i.e. inverse time delay)

Independent time characteristic

The operate time in Definite Time (DT) mode is defined regardless of the fault value. It is activated immediately after the pickup value is reached.

For overcurrent functions, when the current exceeds the set threshold, the independent time characteristic is fixed to the defined operate delay.

Figure 75 - Overcurrent definite time characteristic



Dependent time characteristic

The dependent time characteristic is the Inverse Definite Minimum Time (IDMT) type of operation in accordance with standards IEC 60255-151, IEEE C-37.112 and BS 142.

The dependent time characteristic is available for several protection functions:

- Overcurrent protection
- Ground fault protection
- Negative Sequence (unbalance) protection
- Overvoltage protection
- Undervoltage protection

Dependent operate delay

A large number of dependent time characteristics can be selected for each overcurrent function. A minimum operate time can be defined for each overcurrent function. If the calculated operate delay is less than the set threshold, the operate signal is issued after the minimum operate time has elapsed.

The dependent time characteristics of overvoltage and undervoltage functions are described in the protection functions.

NOTE: Once a ratio *measured value*/*pickup value* (G/Gs) greater than 40 is reached, the tripping time is bounded on the lower end.

IEC, IEEE, ANSI dependent operate delay curves

The IEC, IEEE, ANSI dependent operate delay curves follow the equation below:

$$t = TMS \times \left[\frac{k}{\left(\frac{G}{Gs} \right)^{\alpha} - p} + c \right]$$

E71107A

where:

t is the operate delay in seconds;

G is the measured value;

Gs is the setting (pickup) value;

TMS is the time multiplier setting.

Table 46 - Operating characteristics

Description IEC 60255-151 standard	k	c	α	p	
Data attribute IEC 61850-7-3 standard	setParA	setParB	setParC	setParD	SetCharact
IEC Standard Inverse (IEC/A)	0.14	0	0.02	1	9
IEC Very Inverse (IEC/B)	13.5	0	1	1	10
IEC Extremely Inverse (IEC/C)	80	0	2	1	12
IEC Long Time Inverse	120	0	1	1	14
IEC Ultra Time Inverse	315.2	0	2.1	1	17
Rectifier Inverse	45900	0	5.6	1	18
RI	-4.2373	0	-1	1.43644	19
FR Short Time Inverse	0.05	0	0.04	1	20

Table 46 - Operating characteristics (Continued)

Description IEC 60255-151 standard	k	c	α	p	
Data attribute IEC 61850-7-3 standard	setParA	setParB	setParC	setParD	SetCharact
BPN (EDF)	1000	0.655	2	1	21
ANSI Moderately Inverse (IEC/D)	0.0515	0.114	0.02	1	4
ANSI Very Inverse (IEC/E)	19.61	0.491	2	1	2
ANSI Extremely Inverse (IEC/F)	28.2	0.1217	2	1	1
US Inverse (CO8)	5.95	0.18	2	1	22
US Short Time Inverse (CO2)	0.16758	0.11858	0.02	1	23
ANSI Normally Inverse	8.9341	0.17966	2.0938	1	24
ANSI Short Time Inverse	0.2663	0.03393	1.2969	1	25
ANSI Long Time Inverse	5.6143	2.18592	1	1	26

IAC dependent operate delay curves

The IAC dependent operate delay curves follow the equation below:

$$t = TMS \times \left[A + \frac{B}{\left(\frac{G}{Gs} - C \right)} + \frac{D}{\left(\frac{G}{Gs} - C \right)^2} + \frac{E}{\left(\frac{G}{Gs} - C \right)^3} \right]$$

E71108A

where:

t is the operate delay in seconds;

G is the measured value;

Gs is the setting (pickup) value;

TMS is the time multiplier setting.

Table 47 - Operating characteristics

Description	A	B	C	D	E	
Data attribute IEC 61850-7-3 standard	setParA	setParB	setParC	setParD	setParE	SetCharact
IAC Inverse	0.2078	0.863	0.8	-0.418	0.1947	28
IAC Very Inverse	0.09	0.7955	0.1	-1.289	7.959	29
IAC Extremely Inverse	0.004	0.6397	0.62	1.787	0.2461	30

RXIDG dependent operate delay curve

The RXIDG dependent operate delay curve follows the equation below:

$$t = TMS \times \left[5.8 - 1.35 \times \ln\left(\frac{G}{Gs} \right) \right]$$

E71109A

where:

t is the operate delay in seconds;

G is the measured value;

Gs is the setting (pickup) value;

TMS is the time multiplier setting.

The RXIDG dependent operate delay curve is number 31.

EPATR dependent operate delay curves

The EPATR curves are commonly used for time delayed sensitive ground fault protection in certain markets. This curve is only available in the Sensitive Ground Fault protection

The EPATR-C dependent operate delay curve is number 32 and follows the equation below:

Table 48 - Operating characteristics

Curve description	Primary current range	Equations
EPATR-C	0.5 A ≤ Ip ≤ 200 A	$t = TMS \times \frac{34.28}{Ip^{\frac{2}{3}}}$ E71115A
	Ip > 200 A	$t = TMS \times 1$ E71116A

where:

t is the operate delay in seconds;

Ip is the primary value;

TMS is the time multiplier setting.

Dependent reset time

The reset time characteristic is according to the following equation:

$$t = TMS \times \left[\frac{k}{1 - \left(\frac{G}{Gs} \right)^{\alpha}} \right]$$ E71117A

where:

t is the reset time in seconds;

G is the measured value;

Gs is the setting pickup value;

TMS is the time multiplier setting.

Dependent time reset is enabled by setting the reset characteristic to **Inverse Reset**. For all operate curves not listed in the table below, the reset timer is of DT type.

Table 49 - IDMT reset time characteristics

Curve description	k	α
IEC Standard Inverse (IEC/A)	8.2	6.45
IEC Very Inverse (IEC/B)	50.92	2.4
IEC Extremely Inverse (IEC/C)	44.1	3.03
IEC Long Time Inverse	40.62	0.4
ANSI Moderately Inverse (IEC/D)	4.85	2
ANSI Very Inverse (IEC/E)	21.6	2

Table 49 - IDMT reset time characteristics (Continued)

Curve description	k	α
ANSI Extremely Inverse (IEC/F)	29.1	2
US Inverse (CO8)	5.95	2
US Short Time Inverse (CO2)	2.261	2
ANSI Normally Inverse	9	2
ANSI Short Time Inverse	0.5	2
ANSI Long Time Inverse	15.75	2
IAC Inverse	0.99	2
IAC Very Inverse	4.678	2
IAC Extremely Inverse	6.008	2

Phase overcurrent (*PHPTOC*/*PHRDIR*, ANSI 50/51/ANSI 67)

Description

Phase overcurrent

The phase overcurrent function is applied to detect phase-to-phase short-circuit currents (phase-to-ground in specific cases). Discrimination is achieved because of the current threshold and operate delay of the different stages of the protection. The measurement type can be subject to the phase overcurrent function: either the fundamental value or the RMS value of the phase currents, or the fundamental minus the zero sequence current. Operation can be set to 1 of 3 or 2 of 3 mode. In 2 of 3 mode the element will only operate when 2 elements operate and will typically not operate for ground faults. The start signals are phase based, however, the timers will only start when the number of operating elements exceed the operating mode. A *Drop Out* output signal is provided to indicate the start has reset but the timers are being held by the reset timer.

Additional functions such as Selective Overcurrent Logic (SOL) and variable loading improve the behavior of the protection function in terms of stability or sensitivity.

Dynamic setting element

The element provides dynamic settings which allow it to adapt to different system conditions. Typical uses of dynamic settings can be one of the following:

- **Selective Overcurrent Logic (SOL)**

  This allows for close coordination with upstream and/or downstream protection. When SOL is configured and linked to this function, the current timer settings are replaced by the timer settings defined by the dynamic settings. Other dynamic settings are normally not changed.

- **Variable loading**

  The curve pickup can be changed during certain operating conditions to lift the pickup without affecting grading for the rest of the curve. This is typically applied for transformer applications where a higher pickup may be needed with one transformer out of service. In this case the status of the other transformer is brought to the device. When it is in service, the start factor multiplier is left at 1, but when it is out of service, it is set to 1.5.

Directional phase overcurrent

The directional phase overcurrent protection function is optionally linked to the phase overcurrent function, whose *Directional mode* can be selected as *forward*, *reverse*, or *non-directional*. When selected as *non-directional*, the directional element is ignored and only the phase overcurrent function is applied. When selected as *forward* or *reverse*, the current direction is determined based on the comparison of voltage and current angles, as detailed in Direction Determination, page 170.

NOTE: If selected as *forward* or *reverse*, the *PHPTOC* must use the same CT as the *PHRDIR* that contributes the *Dir* input signal to it. Otherwise the *PHRDIR* does not work as intended.

This function is applied to systems where phase-to-phase fault currents can flow in both directions, such as parallel feeders, ring feeders, and interlocked overcurrent busbar schemes. Depending on the application, the direction signal is used to generate either a tripping or a blocking.

Direction Determination

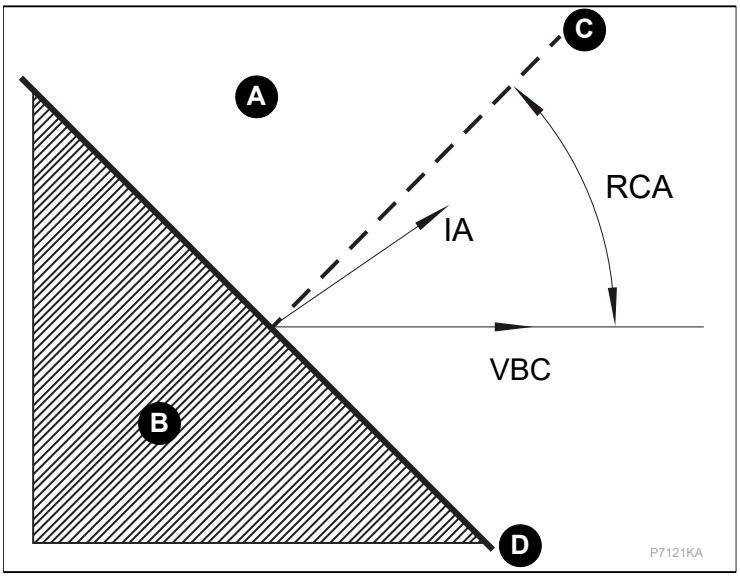
The determination of the fault current direction considers the quadrature voltage angle, the current angle, and the selected Relay Characteristic Angle (RCA) angle.

Forward	-90° < (angle(I) - angle(V) - RCA) < 90°
Reverse	90° < (angle(I) - angle(V) - RCA) < -90°

NOTE: Voltages are memorized when all phases are above 70% nominal and the memory voltage is available for 5s following any voltage loss to allow correct operation for bolted 3 phase faults. Memory voltage is used whenever the measured voltage is below the *Minimum line voltage* setting. Indication is provided when the memory voltage is used and for operation after expiry of the memory voltage. If all voltages are below the minimum line voltage, an additional indication is provided.

The following diagram shows the direction determination mechanism for a phase A fault.

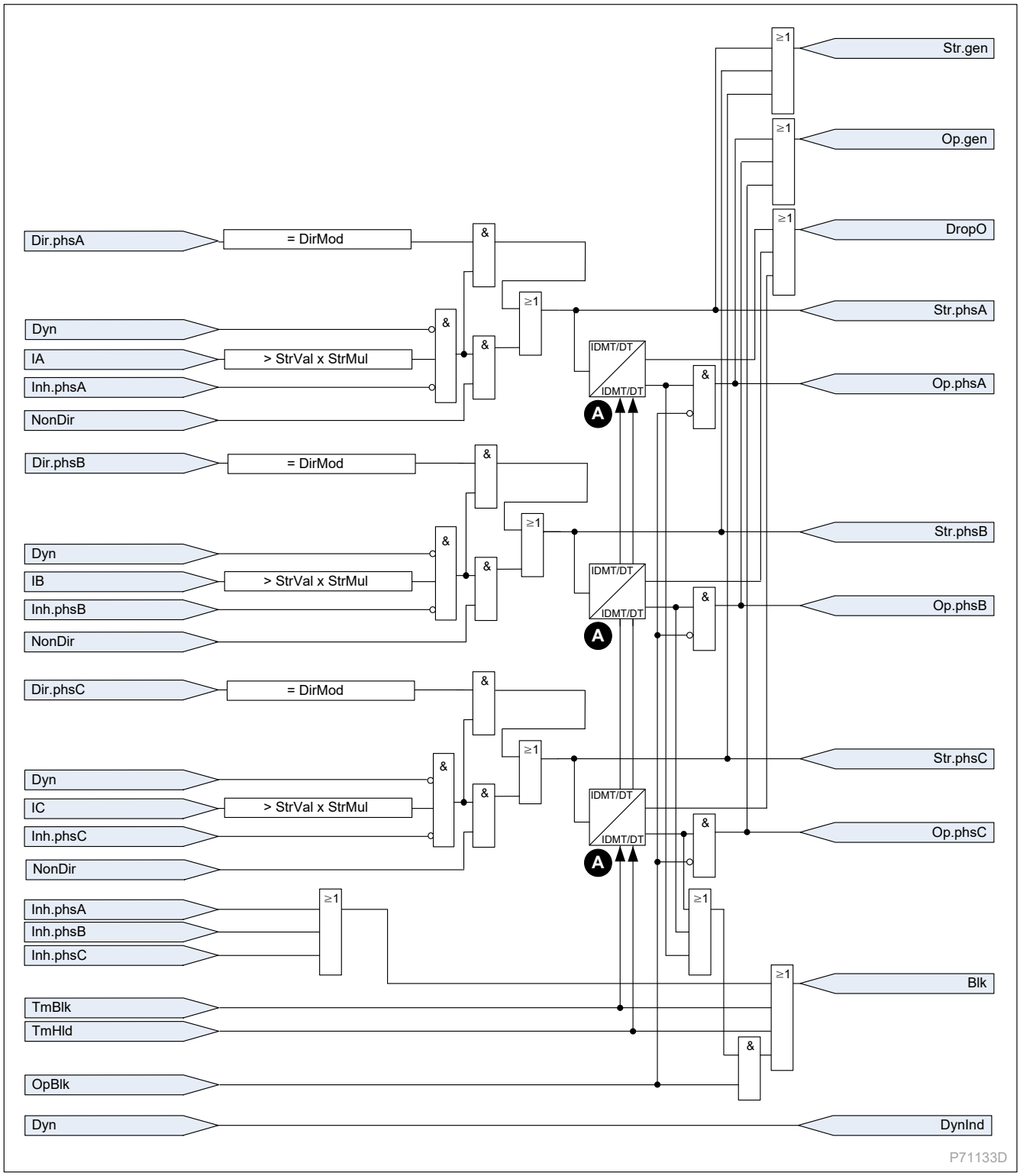
Figure 76 - Direction determination for a phase A fault



A	Forward direction	B	Backward direction
C	Maximum torque line	D	Zero torque (boundary) line

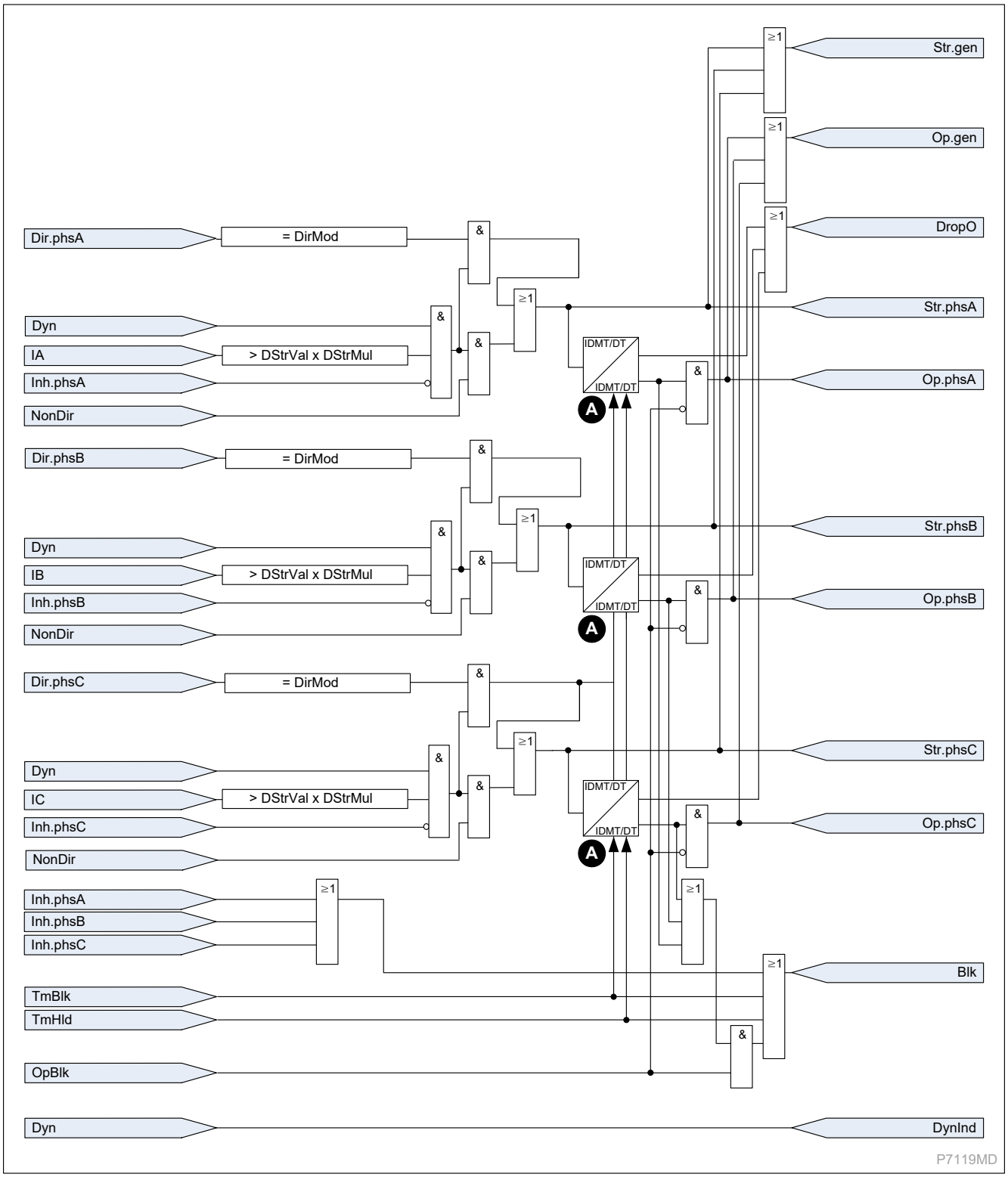
Block diagram

Figure 77 - Block diagram of the *PHPTOC* (with dynamic input low)



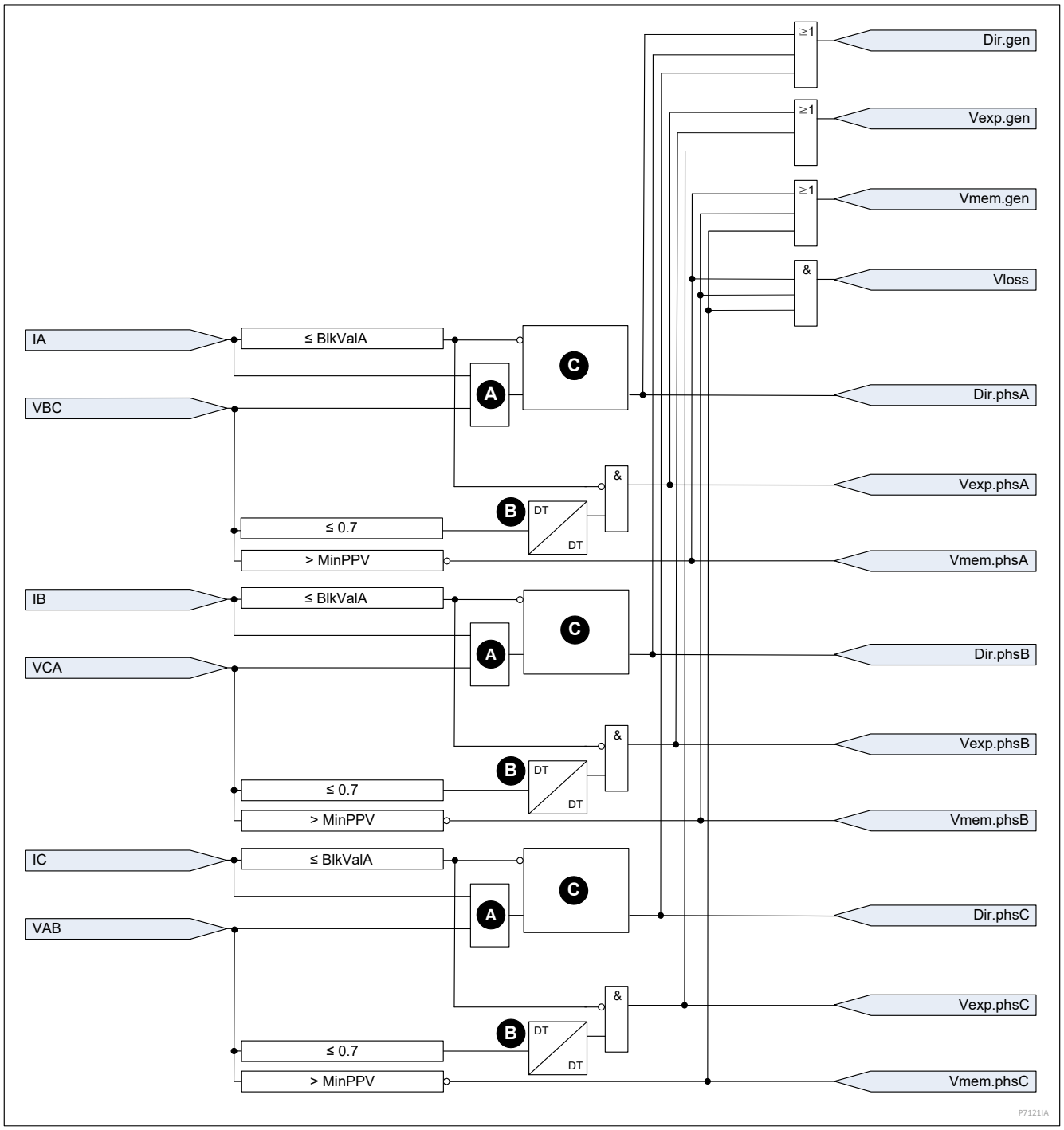
A DT Operate delay: *OpDITmms*
IDMT Operate delay: *TmACrv*, *TmMult*, *MinOpTmms*
DT Reset delay: *RsDITmms*
IDMT Reset delay: *TmACrv*, *TypRsCrv*

Figure 78 - Block diagram of the *PHPTOC* (with dynamic input high)



A	DT Operate delay: *DOpDITmms* IDMT Operate delay: *TmACrv*, *DTmMult*, *DMinOpTmms* DT Reset delay: *DRsDITmms* IDMT Reset delay: *TmACrv*, *TypRsCrv*

Figure 79 - Block diagram of the *PHRDIR*



A	Angle calculation • RotPh=ABC: alpha= angle_Ix-angle_Vpolx-ChrAng • RotPh=ACB: alpha= angle_Ix-angle_Vpolx-ChrAng+180° • mag_Vx > MinPPV: angle_Vpolx = angle_Vmeasurex • mag_Vx ≤ MinPPV: angle_Vpolx = angle_Vmemoryx
B	Memory time: 5 s
C	Direction determination

Input and output signals

Table 50 - Input signals of the *PHPTOC*

Name	Short label	Infotip
Inh[general;phsA;phsB; phsC]	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers
OpBlk	Op block	Output blocked when active (timers not held)
Dyn	Dynamic	Activate dynamic settings
Dir	Direction	Direction
IAIBIC	Phase current	Phase current
IAIBICRMS	Phase RMS current	Linked to phase current input source
I0	I0	Linked to phase current input source
NonDir	Non dir	Force non directional

Table 51 - Input signals of the *PHRDIR*

Name	Short label	Infotip
IAIBIC	Phase current	Phase current
UABUBCUCA	Line voltage	Line voltage

Table 52 - Output signals of the *PHPTOC*

Name	Short label	Infotip
Dyn	Dynamic settings	Dynamic settings active
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked

Table 53 - Output signals of the *PHRDIR*

Name	Short label	Infotip
Dir	Direction	Direction
Vmem	Memory voltage active	Memory voltage active
Vexp	Memory voltage expired	Memory voltage expired
Vloss	All voltages low	All voltages low
PhiA V2.2.1	Phase A measured angle	Phase A measured angle
PhiB V2.2.1	Phase B measured angle	Phase B measured angle
PhiC V2.2.1	Phase C measured angle	Phase C measured angle

Setting parameters

Table 54 - Settings of the *PHPTOC*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
MeasType	Measurement mode	Fast Fourier Transform (FFT) is usually used. RMS settings need to consider the measured value may be higher with offset waveforms. FFT-I0 can be applied to transformer star winding to improve sensitivity for phase to phase faults	• FFT • RMS • FFT-I0		FFT
OpStat	Operation mode	If 1/3 is selected any phase pickup will start the function. 2/3 requires 2 phases to pickup	• 1/3 • 2/3		1/3
DirMod	Directional mode	Directional mode	• Non directional • Forward • Reverse		Non direc-tional
TmACrv	Operating curve	Operating curve	• ANSI extremely inverse • ANSI very inverse • ANSI normal inverse • ANSI moderate inverse • Definite time • IEC normal inverse • IEC very inverse • IEC extremely inverse • IEC long inverse • IEC ultra inverse • Rectifier inverse • RI • FR short inverse • US inverse CO8 • US short inverse CO2 • ANSI short inverse • ANSI long inverse • IAC inverse • IAC very inverse • IAC extremely inverse		
StrVal	Start value	This is the base current used for operating curves. The operating time is based on the measured current as a multiple of this value	0.005...40 pu	0.001 pu	1 pu
StrMult	Start value multiplier	Multiplied by Start value to give the Start/Threshold/Pickup level	1...10	0.001	1
OpDlTmms	DT/IDMT adder op delay	Time delay in DT mode. In IDMT modes this time delay is added to the curve operating time delay	0...10000000 ms	1 ms	0 ms
TmMult	IDMT delay multiplier	IDMT time delay multiplier or TMS	0...20	0.001	1
MinOpTmms	IDMT min op delay	For IDMT curves this is the minimum tripping time delay excluding IDMT adder. Usually used to coordinate with downstream fuses. A zero setting means the curve determines the minimum time delay	0...100000 ms	1 ms	0 ms
TypRsCrv	Reset curve	Reset curve	• Definite time • Inverse		Definite time
RsDlTmms	DT reset delay	DT reset time delay	0...1000000 ms	1 ms	40 ms

Table 54 - Settings of the *PHPTOC* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
DStrVal	Dynamic start value	Active setting when the dynamic input is active	0.005...40 pu	0.001 pu	1 pu
DStrMult	Dyn start value multiplier	Active setting when the dynamic input is active	1...10	0.001	1
DOpDlTmms	Dyn DT/IDMT adder op delay	Active setting when the dynamic input is active	0...10000000 ms	1 ms	0 ms
DTmMult	Dyn IDMT delay multiplier	Active setting when the dynamic input is active	0...20	0.001	1
DMi-nOpTmms	Dyn IDMT min op delay	Active setting when the dynamic input is active	0...100000 ms	1 ms	0 ms
DRsDlTmms	Dyn DT reset delay	Active setting when the dynamic input is active	0...1000000 ms	1 ms	40 ms

Table 55 - Settings of the *PHRDIR*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
ChrAng	Characteristic angle	This is the maximum torque angle or the mid point between the directional boundaries of I and V quadrature (eg IA to VBC). It is typically set to 30 for transmission systems and 45 for distribution systems	30...45 deg	15 deg	45 deg
MinPPV	Minimum line voltage	When the measured quadrature voltage drops below this level the element will use memory voltage if available	0.01...2 pu	0.01 pu	0.7 pu
BlkValA	Minimum current	Minimum current for operation	0.01...40 pu	0.001 pu	0.01 pu

Characteristics

Table 56 - Characteristics of the *PHPTOC*

Characteristics		Values
Start value	Accuracy	±2% or ±0.001 pu (sinusoidal input) ±5% or ±0.002 pu (fully offset input) ±5% or ±0.005 pu (under Level 5 power frequency magnetic field)
	Reset ratio	98% ± 2%
	Transient overreach	< 5% with X/R up to 120
Minimum IDMT trip level	Accuracy	1.025 Is ± 2.5%
Operate delay	DT accuracy	±2% or ±10 ms
	IDMT accuracy	±5% or ±20 ms (with applicable factor according to IEC 60255-151)
Reset time	DT accuracy	±2% or ±30 ms
	IDMT accuracy	±5% or ±40 ms
Characteristic time	Start time	< 25 ms with non directional (≥ 2 Is) < 45 ms with directional Fwd or Rev (≥ 2 Is)
	Start reset time	< 30 ms at 0.9 Is

Table 56 - Characteristics of the *PHPTOC* (Continued)

	Disengaging time	< 30 ms at 0 Is
	Overshoot time	< 30 ms
	Changeover/back time (Dynamic input)	(Dynamic input) < 20 ms

Table 57 - Characteristics of the *PHRDIR*

Characteristics		Values
Boundary angle	Accuracy	±2°
Directional hysteresis	Accuracy	1°
MinPPV voltage	Accuracy	±1% or ±0.1 V
Characteristic time	Start time	< 20 ms (≥ 2 Is)
	Reset time	< 25 ms
	Voltage memory time	5 s ± 0.05 s

Ground overcurrent (*EFPTOC*/*EFRDIR*, ANSI 50N/51N/ANSI 67N)

Description

The ground overcurrent protection function is used on three wire systems to detect when one of the phases has come into contact with ground. This can be due to insulation failure in insulated cables or fallen wires/external contact in uninsulated applications.

The protection function can be provided by the summation of three-phase currents either numerically or physically.

- When the CT connection type is 3ph+N or 2ph+N, the protection function will use the measured value.
- When the CT connection type is 3ph, the protection function will use the derived value.
- When the CT connection type is 2ph, the input of the protection function will be invalid.

The ground overcurrent protection function can also be provided using a toroidal CT around all phases or the transformer neutral. The protection function does not need to consider the load so it can be set quite sensitively.

Dynamic setting element

The element provides dynamic settings which allow it to adapt to different system conditions. Typical uses of dynamic settings is:

- **Selective Overcurrent Logic (SOL)**

  This allows for close coordination with upstream and/or downstream protection. When SOL is configured and linked to this function, the current timer settings are replaced by the timer settings defined by the dynamic settings. Other dynamic settings are normally not changed.

Directional ground overcurrent

The directional ground overcurrent protection function is optionally linked to the ground overcurrent protection function which can then be selected as *forward*, *reverse*, or *non-directional*.

The *EFRDIR* is used when ground faults can flow in multiple directions:

- Parallel feeders
- Interlocked overcurrent busbar schemes
- Ring feeder protection

These systems will have directional overcurrent, but the directional ground fault is usually also applied for greater sensitivity. It applies to solid and low resistance grounded systems where ground current flows from a system ground to the fault. Several devices may see the fault simultaneously and graded operation is required. Primary ground fault current exceeds 100 A and will normally be measured using residual current either calculated from phase currents or using a Holmgreen connection.

The *EFRDIR* determines the fault direction based on comparison of voltage and current angles. When available zero sequence voltage is the preferred polarizing quantity using -VN and IN, but requires a 5 limb VT or 3 single phase VTs. Two winding VTs can be used but require negative sequence polarization using -V2 and I2 as the polarizing quantities.

Direction determination

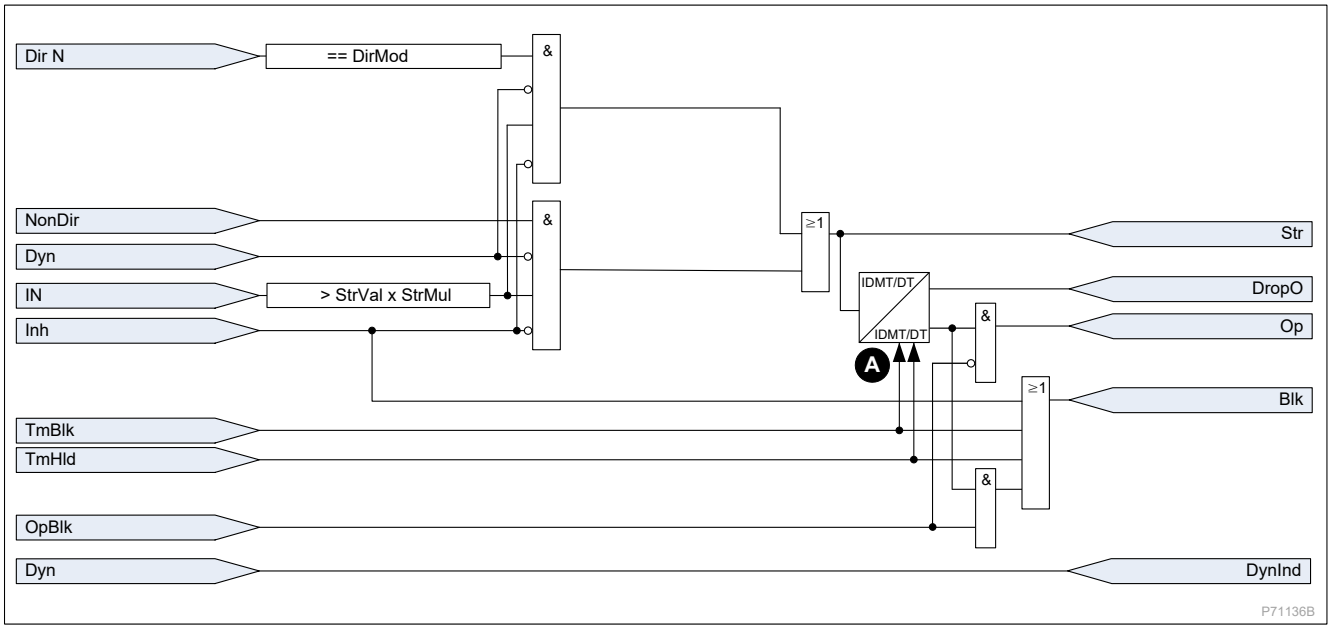
The determination of the fault current direction considers the polarizing voltage angle, the polarizing current angle, and the selected Relay Characteristic Angle (RCA) angle is shown in Direction calculation, page 178.

Table 58 - Direction calculation

Forward	-90° < (angle(I) - angle(V) - 180° - RCA) < 90°
Reverse	90° < (angle(I) - angle(V) - 180° - RCA) < -90°

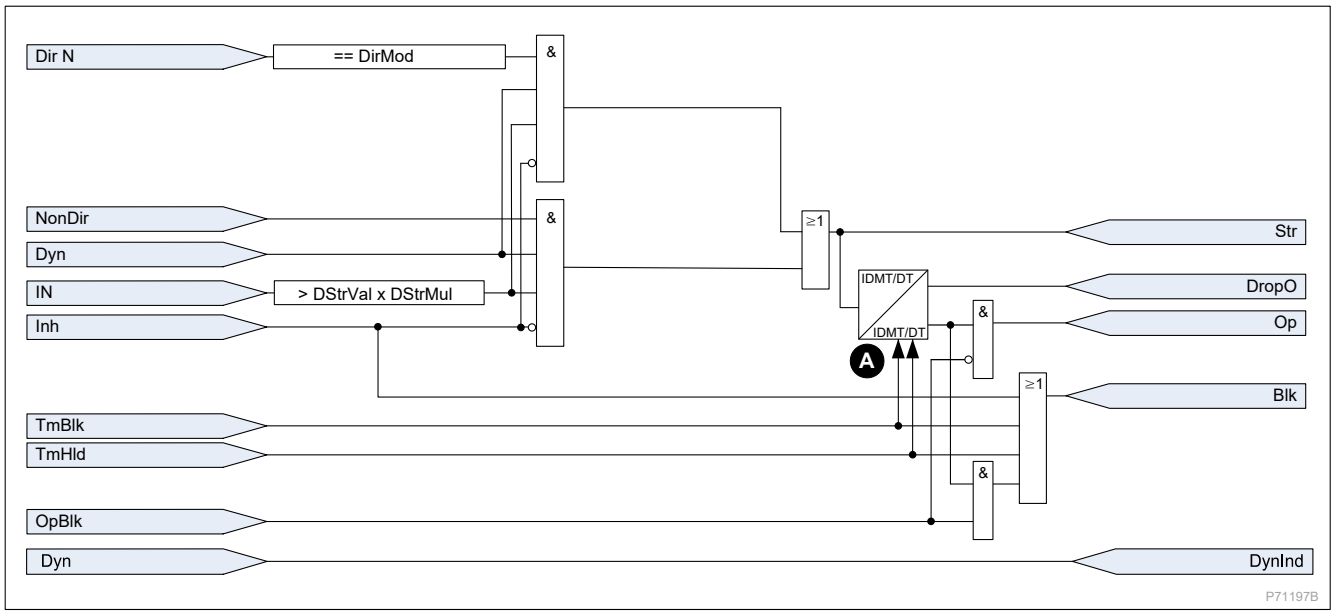
Block diagram

Figure 80 - Block diagram of the *EFPTOC* (with dynamic input low)



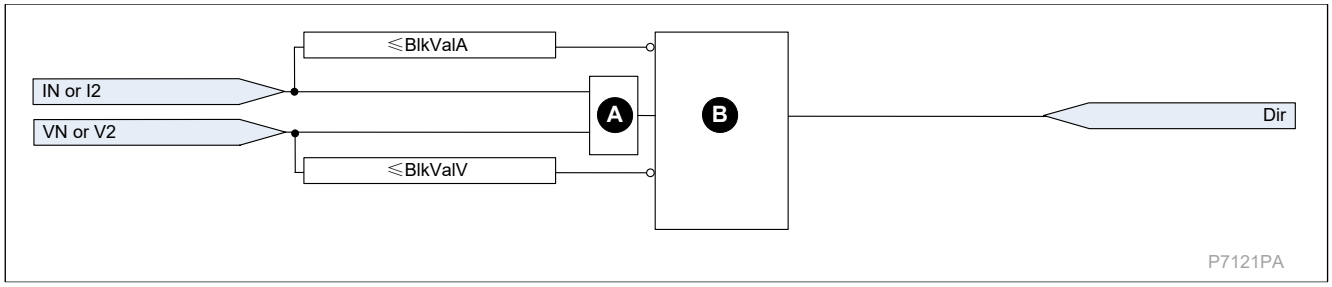
A	DT Operate delay: *OpDITmms* IDMT Operate delay: *TmACrv*, *TmMult*, *MinOpTmms* DT Reset delay: *RsDITmms* IDMT Reset delay: *TmACrv*, *TypRsCrv*

Figure 81 - Block diagram of the *EFPTOC* (with dynamic input high)



A	DT Operate delay: *DOpDITmms* IDMT Operate delay: *TmACrv*, *DTmMult*, *DMinOpTmms* DT Reset delay: *DRsDITmms* IDMT Reset delay: *TmACrv*, *TypRsCrv*

Figure 82 - Block diagram of the *EFRDIR*



A	Angle calculation	B	Direction determination

Input and output signals

Table 59 - Input signals of the *EFPTOC*

Name	Short label	Infotip
Inh[general; neut]	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers
OpBlk	Op block	Output blocked when active (timers not held)
Dyn	Dynamic	Activate dynamic settings
INFFT	IN	IN

Table 59 - Input signals of the *EFPTOC* (Continued)

Name	Short label	Infotip
INRMS	IN RMS	IN RMS
Dir	Direction	Direction
NonDir	Non dir	Force non directional

Table 60 - Input signals of the *EFRDIR*

Name	Short label	Infotip
IN	IN	IN
I2	I2	Linked to IN input source
VN	VN	VN
V2	V2	Linked to VN input source

Table 61 - Output signals of the *EFPTOC*

Name	Short label	Infotip
Dyn	Dynamic settings	Dynamic settings active
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked

Table 62 - Output signals of the *EFRDIR*

Name	Short label	Infotip
Dir	Direction	Direction
PhiN V2.2.1	Measured angle	Measured angle

Setting parameters

Table 63 - Settings of the *EFPTOC*

Name	Short label	Infotip	Setting Range	Step Size	Default Setting
SetMod	Function status	Function status	• On • Off		Off
MeasType	Measurement mode	Fast Fourier Transform (FFT) is usually used. RMS settings need to consider the measured value may be higher with offset waveforms	• FFT • RMS		FFT
DirMod	Directional mode	Directional mode	• Non directional • Forward • Reverse		Non directional
TmACrv	Operating curve	Operating curve	• ANSI extremely inverse • ANSI very inverse • ANSI normal inverse • ANSI moderate inverse • Definite time • IEC normal inverse • IEC very inverse • IEC extremely inverse		

Table 63 - Settings of the *EFPTOC* (Continued)

Name	Short label	Infotip	Setting Range	Step Size	Default Setting
			• IEC long inverse • IEC ultra inverse • Rectifier inverse • RI • FR short inverse • BPN • US inverse CO8 • US short inverse CO2 • ANSI short inverse • ANSI long inverse • IAC inverse • IAC very inverse • IAC extremely inverse • RXIDG		
StrVal	Start value	This is the base current used for operating curves. The operating time is based on the measured current as a multiple of this value	0.005...40 pu	0.001 pu	1 pu
StrMult	Start value multiplier	Multiplied by Start value to give the Start/Threshold/Pickup level	1...10	0.001	1
OpDlTmms	DT/IDMT adder op delay	Time delay in DT mode. In IDMT modes this time delay is added to the curve operating time delay	0...10000000 ms	1 ms	0 ms
TmMult	IDMT delay multiplier	IDMT time delay multiplier or TMS	0...20	0.001	1
MinOpTmms	IDMT min op delay	For IDMT curves this is the minimum tripping time delay excluding IDMT adder. Usually used to coordinate with downstream fuses. A zero setting means the curve determines the minimum time delay	0...100000 ms	1 ms	0 ms
TypRsCrv	Reset curve	Reset curve	• Definite time • Inverse		Definite time
RsDlTmms	DT reset delay	DT reset time delay	0...10000000 ms	1 ms	40 ms
DStrVal	Dynamic start value	Active setting when the dynamic input is active	0.005...40 pu	0.001 pu	1 pu
DStrMul	Dyn start value multiplier	Active setting when the dynamic input is active	1...10	0.001	1
DOpDlTmms	Dyn DT/IDMT adder op delay	Active setting when the dynamic input is active	0...10000000 ms	1 ms	0 ms
DTmMult	Dyn IDMT delay multiplier	Active setting when the dynamic input is active	0...20	0.001	1
DMi-nOpTmms	Dyn IDMT min op delay	Active setting when the dynamic input is active	0...100000 ms	1 ms	0 ms
DRsDlTmms	Dyn DT reset delay	Active setting when the dynamic input is active	0...1000000 ms	1 ms	40 ms

Table 64 - Settings of the *EFRDIR*

Name	Short label	Infotip	Setting Range	Step Size	Default Setting
SetMod	Function status	Function status	• On • Off		Off
ChrAng	Characteristic angle	This is the maximum torque angle or the mid point between the directional boundaries of IN and -VN. It is typically	-60...0 deg	15 deg	-45 deg

Table 64 - Settings of the *EFRDIR* (Continued)

Name	Short label	Infotip	Setting Range	Step Size	Default Setting
		set to -30 for transmission systems and -45 for distribution systems			
PolQty	Polarization mode	This is typically set to Zero sequence when available from the VT (3 single phase VTs or 5 limb). 3 limb VTs typically have only phase connections and require Negative sequence polarization	• Zero sequence • Negative sequence		Zero sequence
BlkValV	Minimum voltage	Minimum voltage for operation	0.01...2 pu	0.01 pu	0.05 pu
BlkValA	Minimum current	Minimum current for operation	0.01...40 pu	0.001 pu	0.01 pu

Characteristics

Table 65 - Characteristics of the *EFPTOC*

Characteristics		Values
Start value	Accuracy	±2% or ±0.001 pu (sinusoidal input) ±5% or ±0.002 pu (fully offset input)
	Reset ratio	98 % ± 2%
	Transient overreach	< 5% with X/R up to 120
Minimum IDMT trip level	Accuracy	1.025 Is ± 2.5%
Operate delay	DT accuracy	±2% or ±10 ms
	IDMT accuracy	±5% or ±20 ms (with applicable factor according to IEC 60255-151)
Reset time	DT accuracy	±2% or ±30 ms
	IDMT accuracy	±5% or ±40 ms
Characteristic time	Start time	< 25 ms with non directional (≥ 2 Is) < 45 ms with directional Fwd or Rev (≥ 2 Is)
	Overshoot time	< 30 ms
	Changeover/back time (Dynamic input)	< 20 ms

Table 66 - Characteristics of the *EFRDIR*

Characteristics		Values
Boundary angle	Accuracy	±2°
Directional hysteresis	Accuracy	1°
Characteristic time	Start time	< 20 ms (≥ 2 Is and ≥ 2 Vs)
	Reset time	< 25 ms

Sensitive ground fault overcurrent (*VSEFPTOC*, ANSI 50SG/51SG)

Description

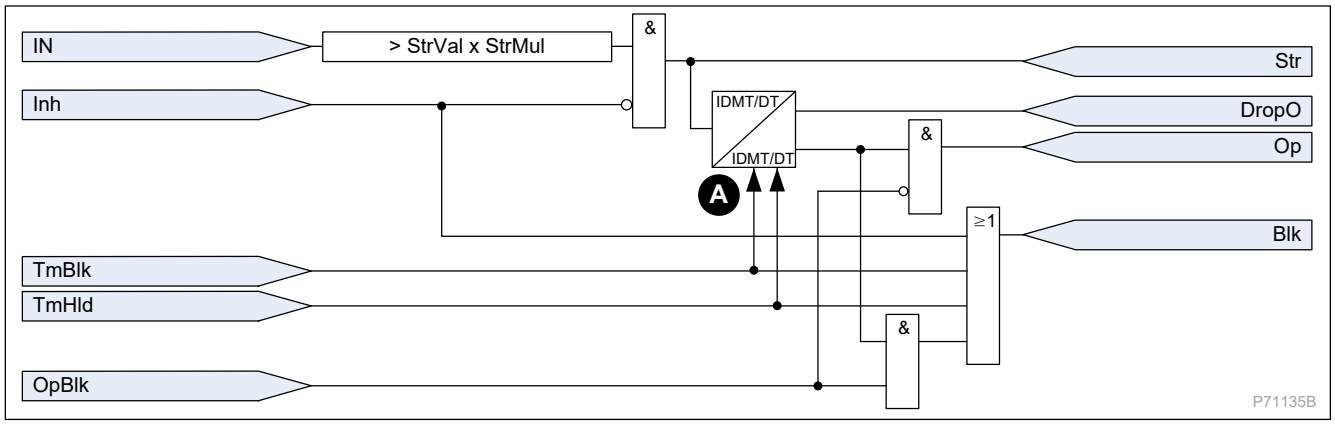
The sensitive ground fault overcurrent protection function is applied to the system in which a single phase ground fault is not detected by means of standard current operated ground fault protection. A fully discriminative ground fault protection is achieved by the *VSEFPTOC* that is used to detect the resultant imbalance in the system charging currents that occurs under ground fault conditions, usually achieved by direct measurement of ground current through a toroid on the ground connection or around all the phase connections.

The current measurement can come from a summated input (physical or numerical), standard 1 A/5 A CT input, or the 1 A core balance CT (when fitted). When summated inputs are used, CT errors may cause operation for settings below 1%.

- When the CT connection type is 3ph+N or 2ph+N, the protection function will use the measured value.
- When the CT connection type is 3ph, the protection will use the derived value.
- When the CT connection type is 2ph, the input of the protection will be invalid.

Block diagram

Figure 83 - Block diagram of the *VSEFPTOC*



A DT Operate delay: OpDITmms
IDMT Operate delay: TmACrv, TmMult, MinOpTmms
DT Reset delay: RsDITmms
IDMT Reset delay: TmACrv, TypRsCrv

Input and output signals

Table 67 - Input signals of the *VSEFPTOC*

Name	Short label	Infotip
Inh[general;neut]	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers
OpBlk	Op block	Output blocked when active (timers not held)
IVSEF	IN	IN

Table 68 - Output signals of the *VSEFPTOC*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked

Setting parameters

Table 69 - Settings of the *VSEFPTOC*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
TmACrv	Operating curve	Operating curve	• ANSI extremely inverse • ANSI very inverse • ANSI normal inverse • ANSI moderate inverse • Definite time • IEC normal inverse • IEC very inverse • IEC extremely inverse • IEC long-time inverse • IEC ultra inverse • Rectifier inverse • RI • FR short inverse • BPN • US inverse CO8 • US short inverse CO2 • EPATR-B • ANSI short inverse • ANSI long inverse • IAC inverse • IAC very inverse • IAC extremely inverse • RXIDG • EPATR-C		
StrVal	Start value	This is the base current used for operating curves. The operating time is based on the measured current as a multiple of this value	0.001...1 pu	0.001 pu	1 pu
StrMult	Start value multiplier	Multiplied by Start value to give the Start/Threshold/ Pickup level	1...10	0.001	1
OpDITmms	DT/IDMT adder op delay	Time delay in DT mode. In IDMT modes this time delay is added to the curve operating time delay	0...10000000 ms	1 ms	0 ms
TmMult	IDMT delay multiplier	IDMT time delay multiplier or TMS	0...20	0.001	1
MinOpTmms	IDMT min op delay	For IDMT curves this is the minimum tripping time delay excluding IDMT adder. Usually used to coordinate	0...100000 ms	1 ms	0 ms

Table 69 - Settings of the *VSEFPTOC* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
		with downstream fuses. A zero setting means the curve determines the minimum time delay			
TypRsCrv	Reset curve	Reset curve	• Definite time • Inverse		Definite time
RsDITmms	DT reset delay	DT reset time delay	0...10000000 ms	1 ms	40 ms

Characteristics

Table 70 - Characteristics of the *VSEFPTOC*

Characteristics		Values
Start value	Accuracy	> 0.005 pu: ±2% or ±0.001 pu (sinusoidal input) 0.002... 0.005 pu: ±5% or ±0.001 pu (sinusoidal input) 0.001...0.002 pu: ±10% or ±0.001 pu (sinusoidal input)
	Reset ratio	98% ± 2%
	Transient overreach	< 5% with X/R up to 120
Minimum IDMT trip level	Accuracy	1.025 Is ± 2.5%
Operate delay	DT accuracy	±2% or ±10 ms
	IDMT accuracy	±5% or ±20 ms at 10 Is (with applicable factor according to IEC 60255-151)
Reset time	DT accuracy	±2% or ±30 ms
	IDMT accuracy	±5% or ±40 ms
Characteristic time	Start time	< 25 ms at 2 Is
	Start reset time	< 30 ms at 0.9 Is
	Overshoot time	< 30 ms

Negative sequence overcurrent (*NPSPTOC*, ANSI 46)

Description

The negative sequence overcurrent protection gives greater sensitivity to detect phase-to-phase faults at the end of long lines, where phase overcurrent elements may not operate.

For rotating machine, the *NPSPTOC* provides the protection against a temperature rise caused by an unbalanced power supply, phase inversion, loss of phase, and unbalanced phase currents.

Dynamic setting element

The element provides dynamic settings which allow it to adapt to different system conditions. Typical uses of dynamic settings can be one of the following:

- **Selective Overcurrent Logic (SOL)**

  This allows for close coordination with upstream and/or downstream protection. When SOL is configured and linked to this function, the current timer settings are replaced by the timer settings defined by the dynamic settings. Other dynamic settings are normally not changed.

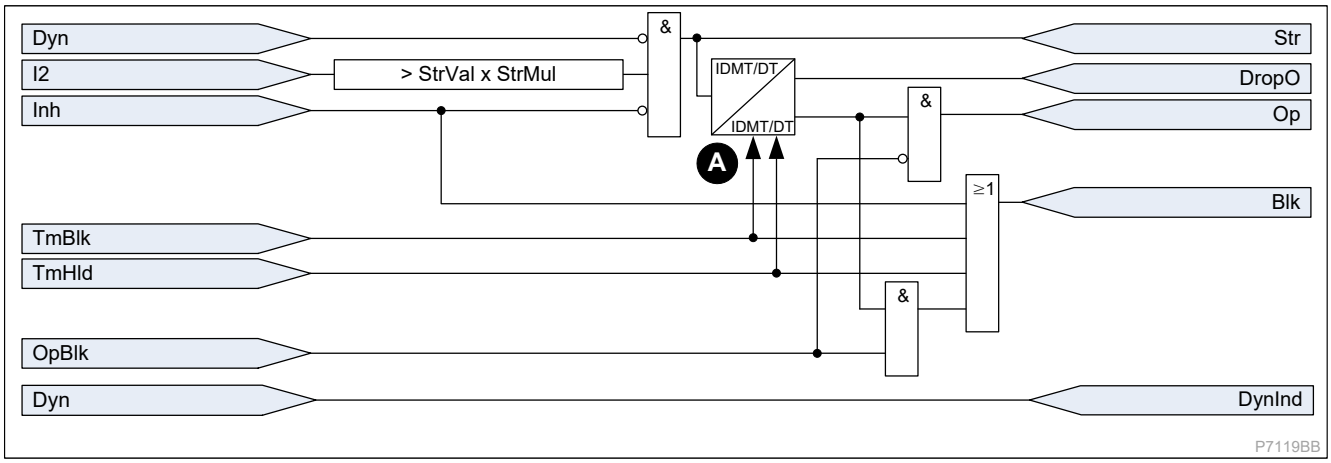
- **Variable loading**

  The curve pickup can be changed during certain operating conditions to lift the pickup without affecting grading for the rest of the curve. This is typically applied for transformer applications where a higher pickup may be needed with one transformer out of service. In this case the status of the other transformer is brought to the device.

  - When it is in service, the start factor multiplier is left at 1.
  - When it is out of service, the start factor multiplier is set to 1.5.

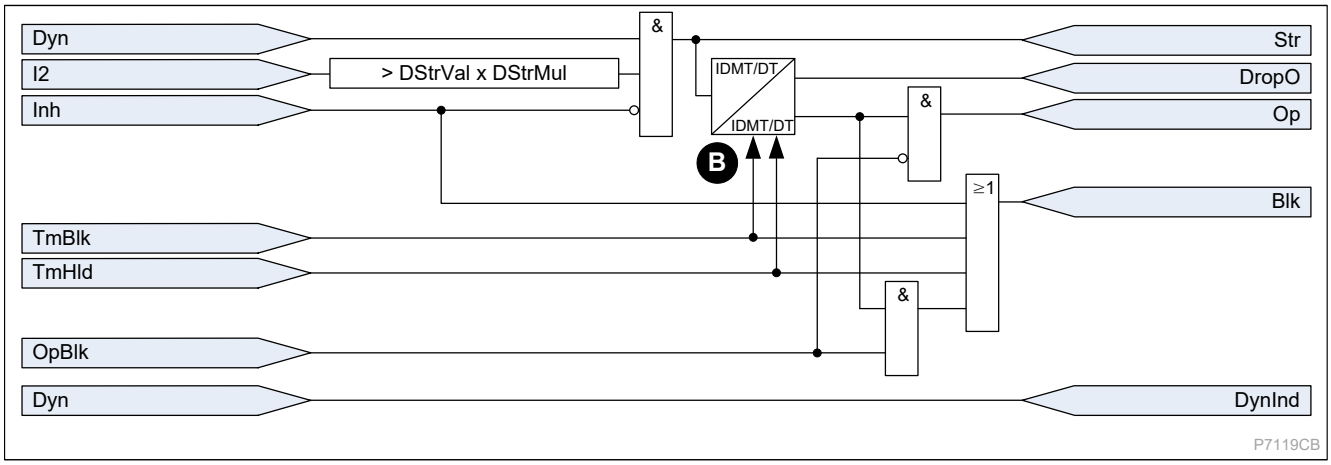
Block diagram

Figure 84 - Block diagram of the *NPSPTOC* (with dynamic input low)



A	DT Operate delay: *OpDITmms* IDMT Operate delay: *TmACrv*, *TmMult*, *MinOpTmms* DT Reset delay: *RsDITmms* IDMT Reset delay: *TmACrv*, *TypRsCrv*

Figure 85 - Block diagram of the *NPSPTOC* (with dynamic input high)



B	DT Operate delay: *DOpDITmms* IDMT Operate delay: *TmACrv*, *DTmMult*, *DMinOpTmms* DT Reset delay: *DRsDITmms* IDMT Reset delay: *TmACrv*, *TypRsCrv*

Input and output signals

Table 71 - Input signals of the *NPSPTOC*

Name	Short label	Infotip
Inh[general;]	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers
OpBlk	Op block	Output blocked when active (timers not held)
Dyn	Dynamic	Activate dynamic settings
I2	I2	I2

Table 72 - Output signals of the *NPSPTOC*

Name	Short label	Infotip
Dyn	Dynamic settings	Dynamic settings active
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked

Setting parameters

Table 73 - Settings of the *NPSPTOC*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
TmACrv	Operating curve	Operating curve	• ANSI extremely inverse • ANSI very inverse • ANSI normal inverse • ANSI moderate inverse • Definite time • IEC normal inverse • IEC very inverse • IEC extremely inverse • IEC long inverse • IEC ultra inverse • Rectifier inverse • RI • FR short inverse • US inverse CO8 • US short inverse CO2 • ANSI short inverse • ANSI long inverse • IAC inverse • IAC very inverse • IAC extremely inverse		
StrVal	Start value	This is the base current used for operating curves. The operating time is based on the measured current as a multiple of this value	0.005...40 pu	0.001 pu	1 pu

Table 73 - Settings of the *NPSPTOC* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
StrMult	Start value multiplier	Multiplied by Start value to give the Start/Threshold/ Pickup level	1...10	0.001	1
OpDlTmms	DT/IDMT adder op delay	Time delay in DT mode. In IDMT modes this time delay is added to the curve operating time delay	0...10000000 ms	1 ms	0 ms
TmMult	IDMT delay multiplier	IDMT time multiplier	0...20	0.001	1
MinOpTmms	IDMT min op delay	For IDMT curves this is the minimum tripping time delay excluding IDMT adder. Usually used to coordinate with downstream fuses. A zero setting means the curve determines the minimum time delay	0...100000 ms	1 ms	0 ms
TypRsCrv	Reset curve	Reset curve	• Definite time • Inverse		Definite time
RsDlTmms	DT reset delay	DT reset time delay	0...10000000 ms	1 ms	40 ms
DStrVal	Dynamic start value	Active setting when the dynamic input is active	0.005...40 pu	0.001 pu	1 pu
DStrMul	Dyn start value multiplier	Active setting when the dynamic input is active	1...10	0.001	1
DOpDlTmms	Dyn DT/IDMT adder op delay	Active setting when the dynamic input is active	0...10000000 ms	1 ms	0 ms
DTmMult	Dyn IDMT delay multiplier	Active setting when the dynamic input is active	0...20	0.001	1
DMinOpTmms	Dyn IDMT min op delay	Active setting when the dynamic input is active	0...100000 ms	1 ms	0 ms
DRsDlTmms	Dyn DT reset delay	Active setting when the dynamic input is active	0...10000000 ms	1 ms	40 ms

Characteristics

Table 74 - Characteristics of the *NPSPTOC*

Characteristics		Values
Start value	Accuracy	±2% or ±0.001 pu (sinusoidal input) ±5% or ±0.002 pu (fully offset input)
	Reset ratio	95% ± 5%
	Transient overreach	< 5% with X/R up to 120
Minimum IDMT trip level	Accuracy	1.025 Is ± 2.5%
Operate delay	DT accuracy	±2% or ±10 ms
	IDMT accuracy	±5% or ±20 ms (with applicable factor according to IEC 60255-151)
Reset time	DT accuracy	±2% or ±30 ms
	IDMT accuracy	±5% or ±40 ms
Characteristic time	Start time	< 25 ms with non directional at 2 Is
	Start reset time	< 30 ms at 0.9 Is
	Disengaging time	< 30 ms at 0 Is

Table 74 - Characteristics of the *NPSPTOC* (Continued)

Characteristics		Values
	Overshoot time	< 30 ms
	Changeover/back time (Dynamic input)	(Dynamic input) < 20 ms
Blocked	Block time	< 20 ms
	Reset time	20...40 ms

Inrush detection (*IDPHAR*, ANSI 68ID)

Description

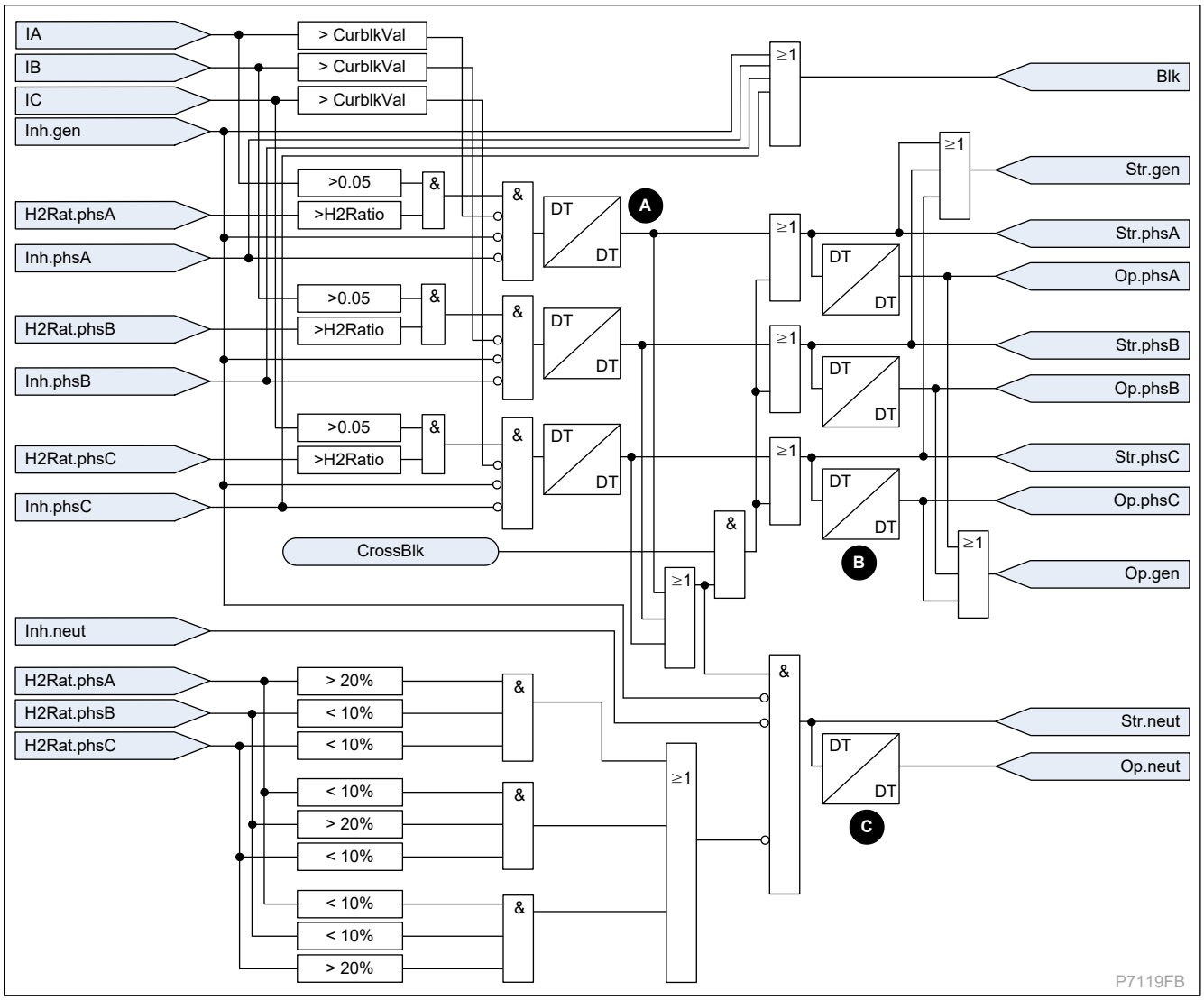
The Inrush Detection (ID) function detects high inrush current flows that occur when transformers or machines are connected (transformer differential uses its own inrush detection). The inrush current detection is determined by 2nd harmonic/fundamental current ratio. Inrush which is non directional could be used to block the following functions:

- 50/51: Phase overcurrent
- 50N/51N: Standard ground fault
- 50SG/51SG: Sensitive ground fault
- 46: Negative sequence overcurrent
- 32P/32Q: Overpower/Reactive overpower

Since the element is a blocking element, it can normally operate for any signal quality. When the CT signals are invalid, it also operates. For operation the fundamental current is higher than a fixed threshold (equal to 0.05 pu) on a per phase basis. On the other hand, when the fundamental input current value of each phase is higher than setting value of maximum phase current for inrush operation, all output signals of the inrush detection would reset. When the start output of one phase is asserted, if the cross blocking status is *Enabled*, the start output of the three phases are asserted at the same time. Whilst the element is normally used to block other elements, by connecting the inrush start to their inhibit input, a timer can also be set to operate an alarm or trip if the inrush is detected for an excessive time. If tripping is required, the start and trip signals from Inrush detection should be connected to the trip conditioning inputs. Elements to be blocked need to have a minimum delay of 30 ms to ensure the blocking is always received before operation.

Block diagram

Figure 86 - Block diagram of *IDPHAR*



A	Operate delay: 25 ms Reset delay: 0 ms	B	Operate delay: *MinOpTmms* Reset delay: 0 ms	C	Operate delay: *MinOpTmms* Reset delay: 0 ms

NOTE: Binary output of the start for ground fault protections (*Str.neut*) is asserted when the general start output (*Str.gen*) is high. It is inhibited when the 2H/1H ratio is higher than 20% on one phase and lower than 10% on the other two phases.

Input and output signals

Table 75 - Input signals of the *IDPHAR*

Name	Short label	Infotip
Inh[general;phsA;phsB;phsC;neut]	Inhibit	Inhibit function
IAIBIC	Phase current	Phase current
H2Rat	Phase current H2	Phase current H2

Table 76 - Output signals of the *IDPHAR*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
Blk	Blocked	Blocked

Setting parameters

Table 77 - Settings of the *IDPHAR*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
H2Ratio	H2/H1 start value	Percentage ratio of second harmonic to fundamental	5...70 %	1 %	20 %
CurBlkVal	Current block value	Fundamental current above this level will block the element	1...40 pu	0.001 pu	15 pu
MinOpTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	0 ms
CrossBlk	Cross block	All phases are operated for operation on any phase	• Off • On		Off

Characteristics

Table 78 - Characteristics of the *IDPHAR*

Characteristics		Values
2H/1H > set point	Accuracy	Threshold ± 5% (absolute value)
	Reset ratio	95% ± 5%
Start time	Accuracy	< 30 ms
LowSet threshold (I > 0.05 pu)	Accuracy	0.05 pu ± 5%
	Reset ratio	95% ± 5%
HighSet threshold (I > CurBlkVal)	Accuracy	Threshold ± 5%
	Reset ratio	95% ± 5%

Selective overcurrent logic (SOL) (*SOLGAPC*)

Description

The SOL function provides the ability to block or temporarily increase the time delay setting of the upstream devices. For example, the following upstream elements could be adapted by the SOL signal.

- 50/51: *PHPTOC*
- 50N/51N: *EFPTOC*
- 46: *NPSPTOC*

This function is the SOL order sender, and the SOL order receiver is the connected upstream device overcurrent functions. The SOL signal (GOOSE or wired) is connected to the dynamic or block input of selected functions in the input

matrix for that function. This connection makes the connected function a SOL receiver.

The creation of SOL order is dependent on the following signal inputs and settings:

- *Start* signals from *PHPTOC*, *EFPTOC* or *NPSPTOC*.
- *Input* signal from *RBRF*.

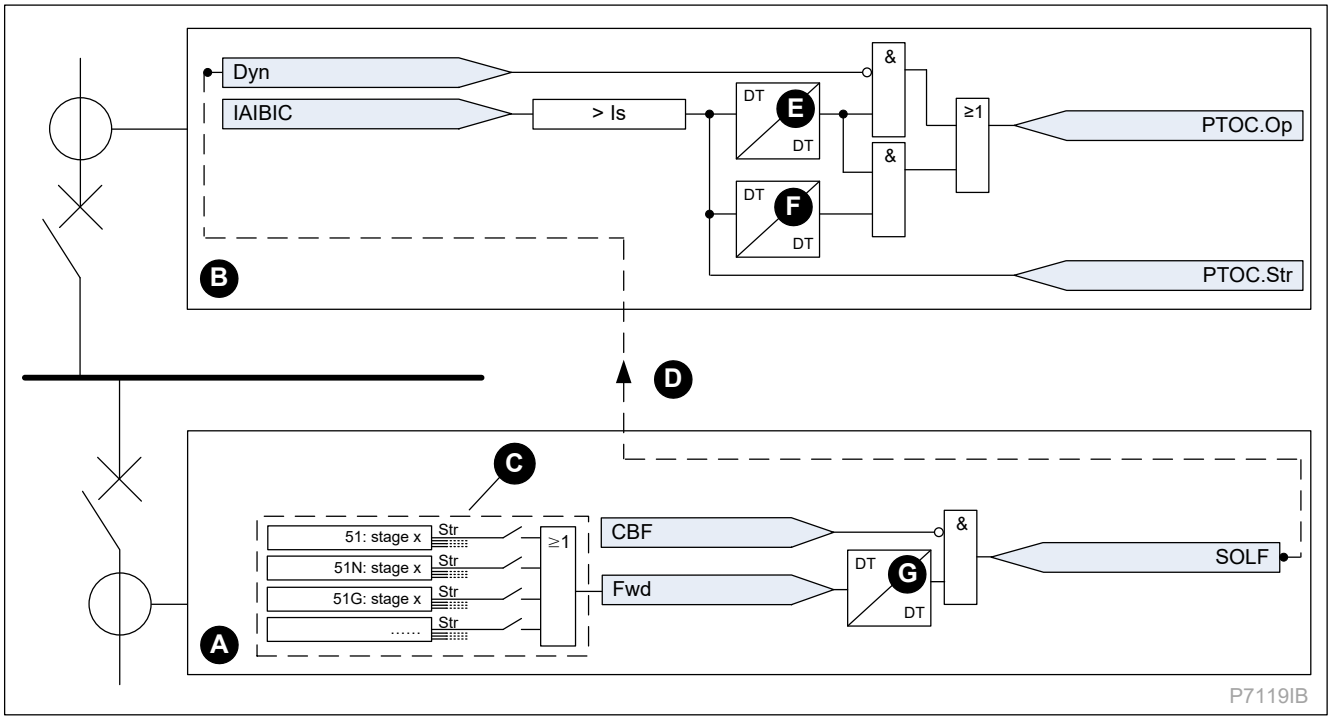
When a fault is cleared by the CB, the start signal of the protection is disengaging, and the SOL order is also disengaging. If the disengaging time between both devices (downstream and upstream) is not same (because the execution cycle is not synchronized between devices, or the ratio fault current/threshold is not same, which has an impact on the disengaging time, etc.), the SOL order is disengaged before disengaging of the start signal of the upstream device. In this situation, there could be a false trip of the upstream device, because the SOL order disappears before disengaging of the start signal and a short timer could elapse. An OFF-delay timing (e.g. 1 cycle-20 ms) is added after the OR of all start signals.

When the downstream CB fails to clear the fault, the SOL signal is reset by the downstream device unblocking the upstream device. Therefore, a CBF signal from *RBRF* function is used to reset the SOL signal.

For schemes with radial current flow only the forward inputs and outputs of the SOL are used. For schemes with bi-directional current flow, the SOL elements used need to be directional and the forward and reverse inputs and outputs of the scheme are used.

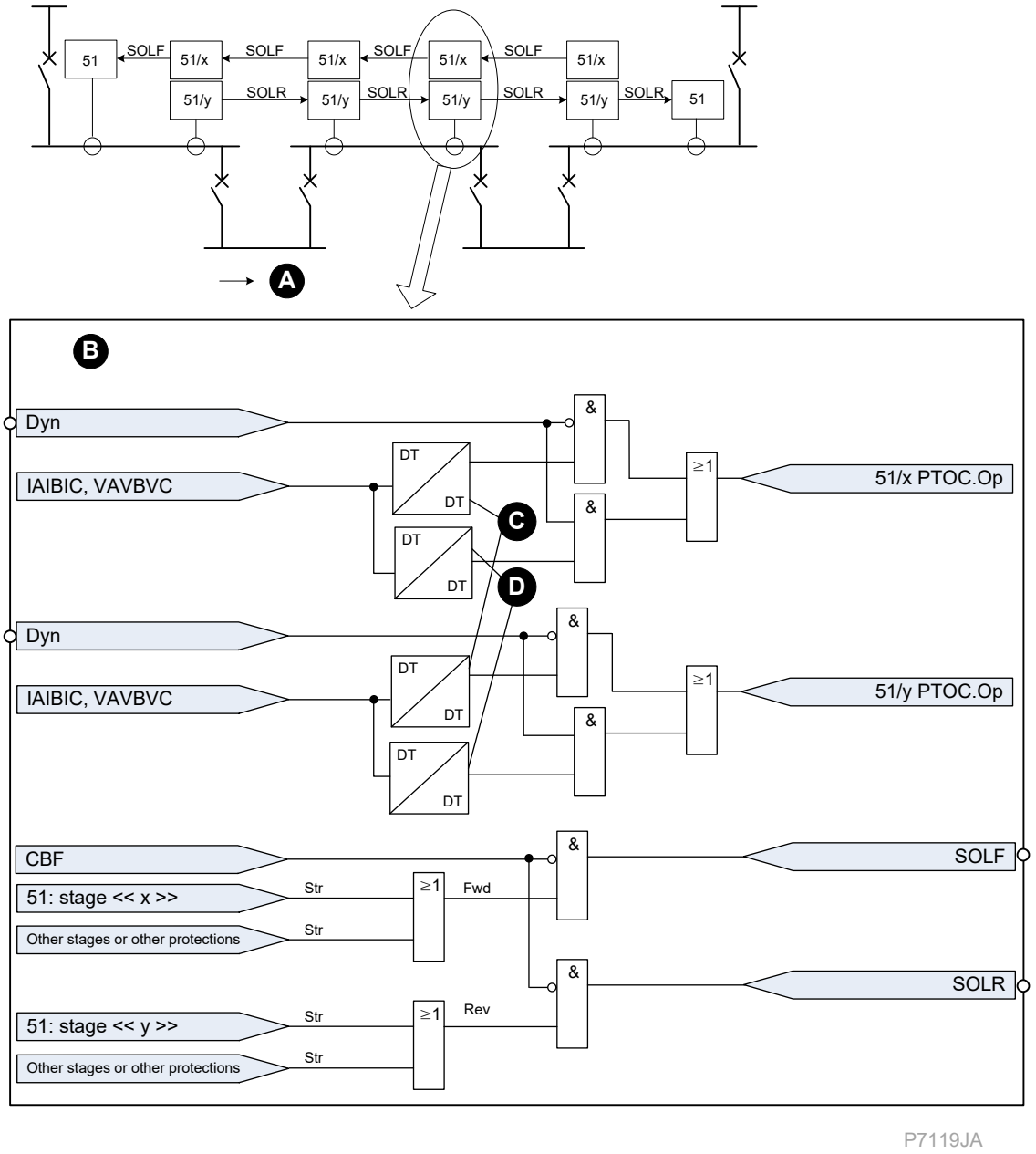
Block diagram

Figure 87 - Block diagram of *SOLGAPC* (with one SOL order)



A	Downstream IED (SOL order sender)	B	Upstream IED (SOL order receiver). e.g. SOL impact on PTOC function
C	Matrix link to input	D	SOL operate: wired logic I/O or GOOSE message
E	Normal setting	F	Dynamic setting
G	Operate delay: 0 ms Reset delay: 20 ms		

Figure 88 - Block diagram of *SOLGAPC* (with two SOL orders and overcurrent protection scheme)



A	Direction of blocking signal orders (SOL orders)	B	IED protection & closed loop. e.g. management of two SOL orders with two stages
C	Normal setting	D	Dynamic setting

Input and output signals

Table 79 - Input signals of the *SOLGAPC*

Name	Short label	Infotip
Inh[general;phsA;phsB; phsC;neut]	Inhibit	Inhibit function
Fwd[general;phsA; phsB;phsC;neut]	Forward	Operates forward output

Table 79 - Input signals of the *SOLGAPC* (Continued)

Name	Short label	Infotip
Rev[general;phsA;phsB; phsC;neut]	Reverse	Operates reverse output
CBF[general;phsA; phsB;phsC;neut]	CBF	Backtrip signal from CBF which resets forward and reverse outputs

Table 80 - Output signals the *SOLGAPC*

Name	Short label	Infotip
SOLF	Forward block	The forward input is active without CBF. Used to block upstream devices
SOLR	Reverse block	The reverse input is active without CBF. Used to block upstream devices
Blk	Blocked	Blocked

Characteristics

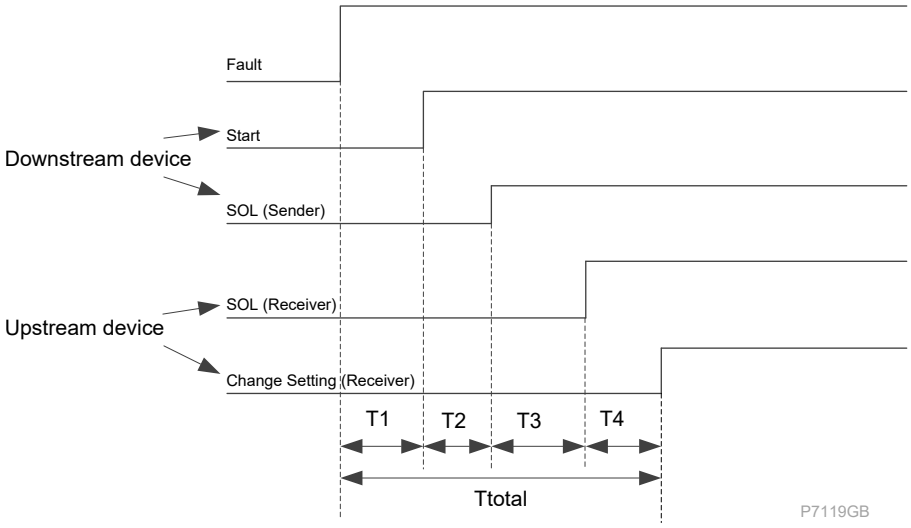
Table 81 - Characteristics of selective overcurrent logic

Characteristics	Values
SOL characteristics time	< 10 ms (based on start input)

The performance in the table above is just for SOL function alone (SOL order creation).

To allow time for the SOL operate order to initiate a change of setting, the protection time setting should be bigger than T_{total} in the figure below. If the setting is less than T_{total}, there is a risk that the upstream device operates before the SOL signal is received and processed..

Figure 89 - Chronogram for SOL order between two devices



Legends:

- *T1* is the time interval between a fault occurs and PTOC start is issued in the downstream device. This is the start time of the PTOC function which can vary depending on whether the element is set directional.
- *T2* is the time interval between PTOC start issued and SOL order issued. In general, *T2* is less than 5 ms.

- *T3* is the time delay of SOL order transmission between the downstream device and upstream device. For GOOSE transmission, this is the total transfer time. For wired transmission, this is the output relay and input filter delays.
- *T4* is the time interval between the SOL signal being processed by the device and the function adapting to the SOL condition. This time is based on the signal acquisition and the execution cycle of PTOC function and is typically 5 ms.
- T_{total} is the total time device between a fault occurs and the setting is changed. Typical values depend upon the type of logic (block or delay) and the communications used. T_{total} is used to determine the delay setting on the upstream device. In a blocking application a safety margin is normally added, a delay of 80 ms/200 ms typically being applied in non-directional/directional applications. For delay applications, the upstream device usually has a time delay characteristic similar to the downstream device. In this case, the delay needs to consider what percentage of operation has occurred before the SOL is received and to ensure that the downstream clearance does not cause operation on the new characteristic considering that the element is already partially operated.

Phase undercurrent (*PHPTUC*, ANSI 37)

Description

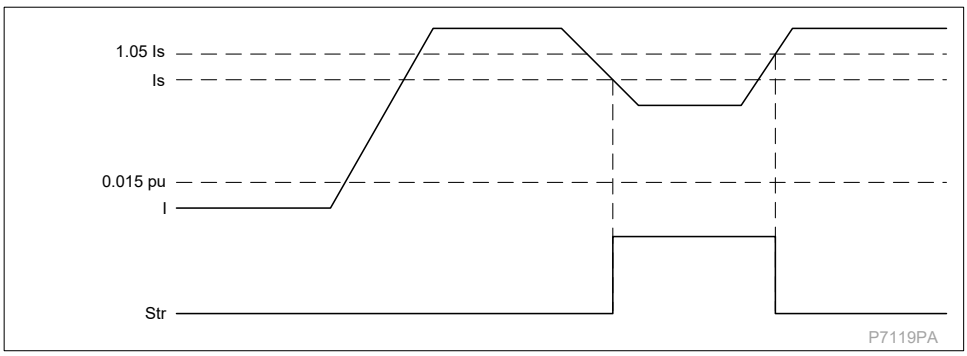
The phase undercurrent protection is used to detect under current conditions. This protection detects the loss of load in motor applications but can also be applied to other applications.

For low current self blocking, to make the difference between a normal operation of the Circuit Breaker (CB) and an undercurrent condition, a zero value setting is used to disable the function. The phase undercurrent protection is blocked when the maximum of the phase currents drops below 0.015 pu to avoid the unwanted tripping.

Starting logic

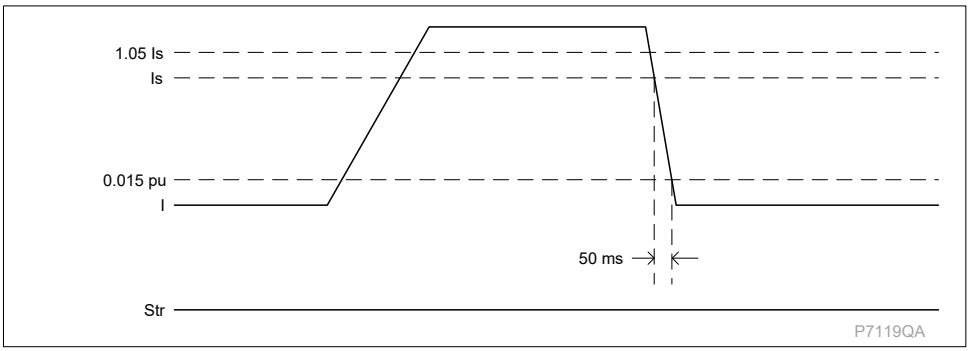
In the starting logic, to prevent the protection from maloperation when the CB is reclosed with some load, the current must first go above the drop-off value before asserting the start signal.

Figure 90 - Assert the start output signal



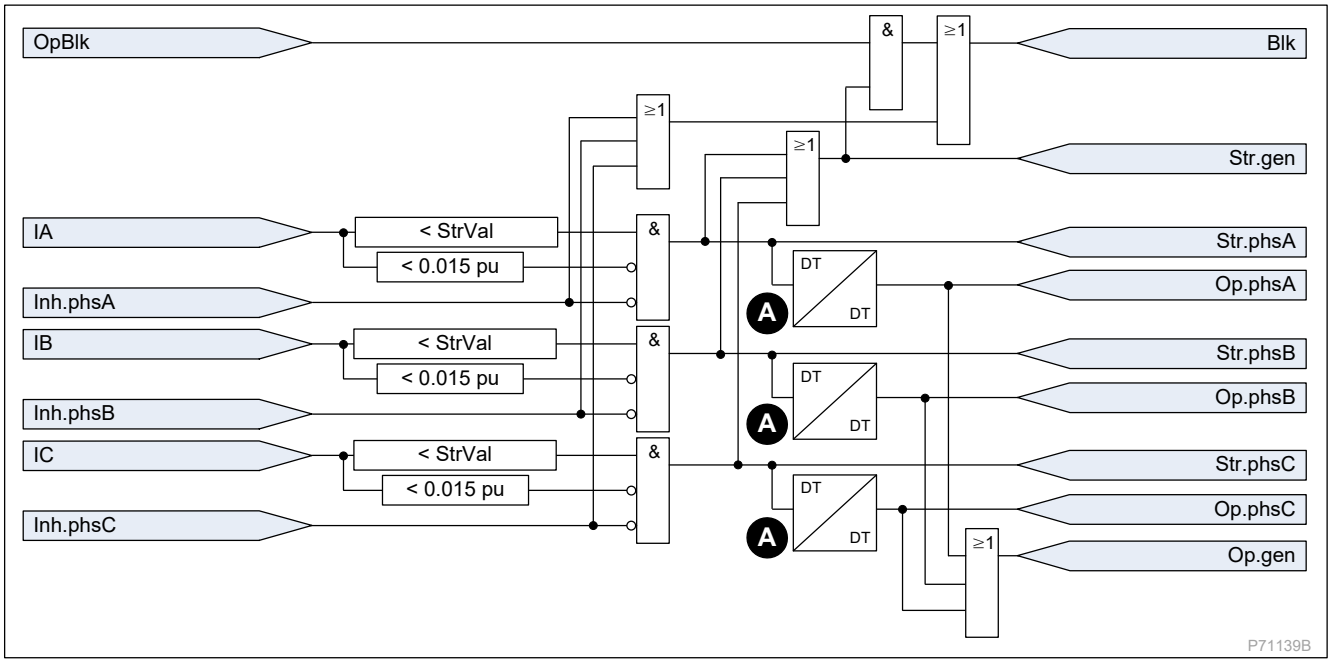
In the starting logic, to distinguish between the fault and the CB opening, when the current drops below 0.015 pu in less than 50 ms from the time when current is below the start threshold, the start signal will not be asserted.

Figure 91 - Deassert the start output signal



Block diagram

Figure 92 - Block diagram of the *PHPTUC*



A Operate delay: *OpDITmms*
Reset delay: *RsDITmms*

Input and output signals

Table 82 - Input signals of the *PHPTUC*

Name	Short label	Infotip
Inh[general;phsA;phsB;phsC]	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers
OpBlk	Op block	Output blocked when active (timers not held)
IAIBIC	Phase current	Phase current

Table 83 - Output signals of the *PHPTUC*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked

Setting parameters

Table 84 - Settings for the *PHPTUC*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrVal	Start value	Element starts for currents below this value and above 0.015pu	0.02...40 pu	0.001 pu	1 pu
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	0 ms
RsDlTmms	Reset delay	Reset time delay	0...10000000 ms	1 ms	0 ms

Characteristics

Table 85 - Characteristics of the *PHPTUC*

Characteristics		Values
Start value	Accuracy	±2% or ±0.001 pu (sinusoidal input)
	Reset ratio	105% ± 5%
Operate delay	Accuracy	±2% or ±10 ms
Characteristic time	Start time	< 100 ms (2...0.2 Is)
	Start reset time	< 30 ms at 2 Is
	Overshoot time	< 30 ms
Blocked	Block time	< 20 ms
	Reset time	20...40 ms

Voltage dependent overcurrent (*PHPVOC*, ANSI 51V)

Description

Voltage Dependent Overcurrent (VDO) calculates different settings during every protection execution in accordance with the measured voltage and the characteristic of VDO. The characteristic diagrams are shown as below.

Figure 93 - *PHPVOC* characteristic 1

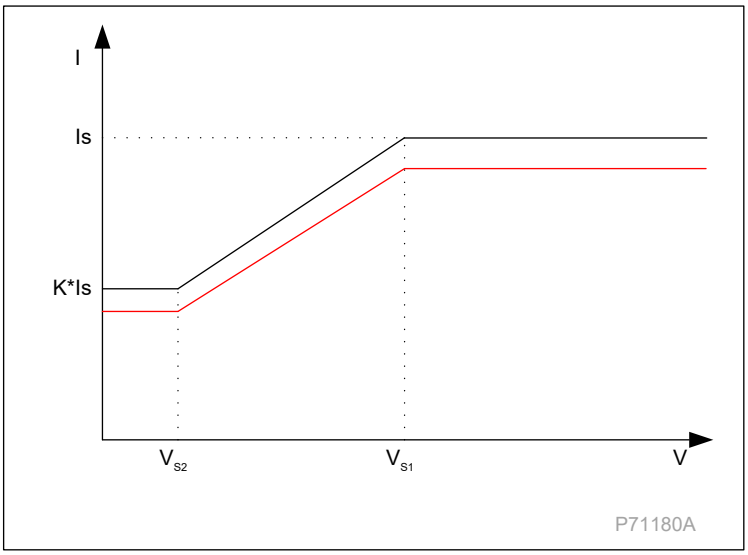
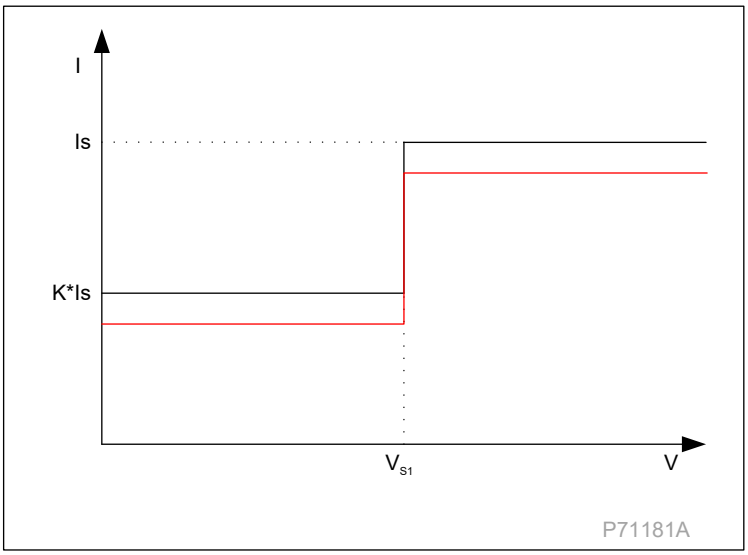


Figure 94 - *PHPVOC* characteristic 2



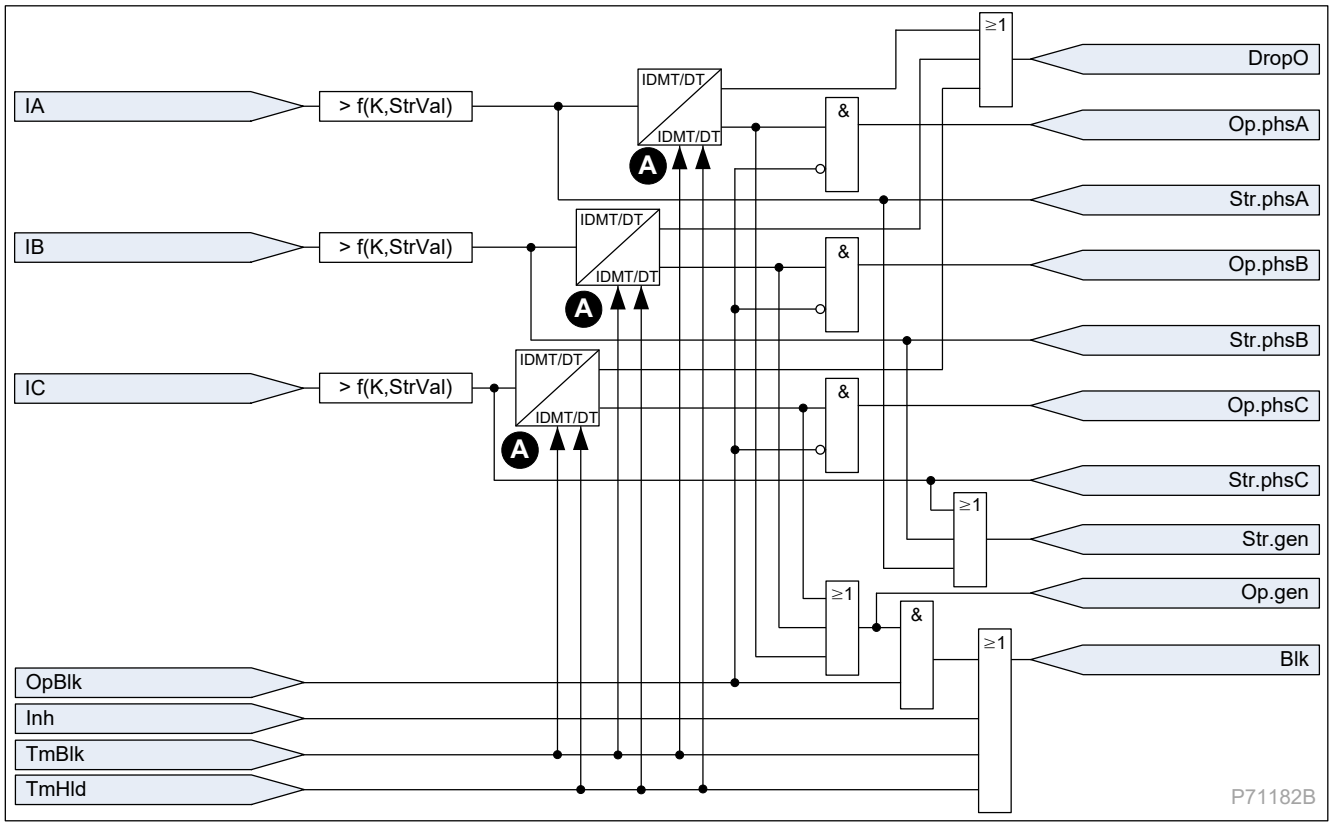
V_{S1} and V_{S2} are two set points of VDO, and K is the multiplying factor. When $V_{S2} < V_{S1}$, the function follows the *PHPVOC* characteristic 1, page 198. When $V_{S2} > V_{S1}$, the function follows the *PHPVOC* characteristic 2, page 198. The FB compares current magnitude with different threshold phase segregated. Take phase A for example, three kinds of setting cases are required, which depends on the comparation result between V_{S1} and V_{S2} and input voltage V_{AB}.

- Case 1: Current setting = I_S,
  ($V_{AB} > V_{S1} > V_{S2}$ or $V_{AB} > V_{S2} > V_{S1}$)
- Case 2: Current setting = $K \times I_S$,
  ($V_{AB} < V_{S2}$ and $V_{AB} < V_{S1}$)
- Case 3: Current setting = $K \times I_S + (1 - K) \times I_S \times (V_{AB} - V_{S2})/(V_{S1} - V_{S2})$,
  ($V_{S2} < V_{AB} < V_{S1}$)

The red line shows the corresponding drop-off level which is 0.95 multiple current setting for each of the cases above. Furthermore, the current setting I_S of case 1 is set as default, bad quality on voltage will force to case 1.

Block diagram

Figure 95 - Block diagram of the *PHPVOC*



A DT Operate delay: *OpDITmms*
IDMT Operate delay
DT Reset delay: *RsDITmms*
IDMT Reset delay

To avoid the maloperation, the function takes delay of 1/2 cycles in region between 100% Is to 120% Is.

Input and output signals

Table 86 - Input signals of the *PHPVOC*

Name	Short label	Infotip
Inh[general;phsA;phsB;phsC]	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers
OpBlk	Op block	Output blocked when active (timers not held)
IAIBIC	Phase current	Phase current
IAIBICRMS	Phase RMS current	Linked to phase current input source
I0	I0	Linked to phase current input source
UABUBCUCA	Line voltage	Line voltage

Table 87 - Output signals of the *PHPVOC*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked

Setting parameters

Table 88 - Settings of the *PHPVOC*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
MeasType	Measurement mode	Fast Fourier Transform (FFT) is usually used. RMS settings need to consider the measured value may be higher with offset waveforms. FFT-I0 can be applied to transformer star winding to improve sensitivity for phase to phase faults	• FFT • RMS • FFT-I0		FFT
TmACrv	Operating curve	Operating curve	• ANSI extremely inverse • ANSI very inverse • ANSI normal inverse • ANSI moderate inverse • Definite time • IEC normal inverse • IEC very inverse • IEC extremely inverse • IEC long inverse • IEC ultra inverse • Rectifier inverse • RI • FR short inverse • US inverse CO8 • US short inverse CO2 • ANSI short inverse • ANSI long inverse • IAC inverse • IAC very inverse • IAC extremely inverse		
StrVal	Start value	Start/Threshold/Pickup value	0.005...40 pu	0.001 pu	1 pu
OpDITmms	DT/IDMT adder op delay	Time delay in DT mode. In IDMT modes this time delay is added to the curve operating time delay	0...10000000 ms	1 ms	0 ms
TmMult	IDMT delay multiplier	IDMT time delay multiplier or TMS	0...20	0.001	1
Min-OpTmms	IDMT min op delay	For IDMT curves this is the minimum tripping time delay excluding IDMT adder. Usually used to coordinate with downstream fuses. A zero setting means the curve determines the minimum time delay	0...100000 ms	1 ms	0 ms
TypRsCrv	Reset curve	Reset curve	• Definite time • Inverse		Definite time

Table 88 - Settings of the *PHPVOC* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
RsDlTmms	DT reset delay	DT reset time delay	0...1000000 ms	1 ms	40 ms
VDOStrV-al1	Max dependent voltage	For voltages below this value the start current is proportionally reduced. If set the same as the minimum voltage then the element is voltage controlled	0.05...1.1 pu	0.01 pu	0.8 pu
VDOStrV-al2	Min dependent voltage	The start value is multiplied by the voltage dependent multiplier when the voltage is below this value	0.05...1.1 pu	0.01 pu	0.6 pu
VDOMult	Voltage dependent multiplier	The start value is multiplied by this value in proportion to max-min dependent voltage	0.1...1	0.005	0.25

Characteristics

Table 89 - Characteristics of the *PHPVOC*

Characteristics		Values
Start value	Accuracy	±2% or ±0.005 pu
	Reset ratio	95% ± 5%
	Transient overreach	< 5% with X/R up to 120
Max dependent voltage Min dependent voltage	Accuracy	±2% or ±0.005 pu
Operate delay	DT accuracy	±2% or ±10 ms
	IDMT accuracy	±5% or ±20 ms (with applicable factor according to IEC 60255-151)
Reset time	DT accuracy	±2% or ±30 ms
	IDMT accuracy	±5% or ±40 ms
Characteristic time	Start time	< 25 ms at 2 Is
	Overshoot time	< 30 ms

Sensitive directional earthfault (*PSDE*, ANSI 32N)

Description

The sensitive directional earthfault protection function (ANSI 32N) is applied for ground fault detection on petersen coil, isolated and high impedance grounded system. On these systems, the primary ground fault current is low. The grounded fault is detected by standard current measurement, but non-faulted circuits may have more current than faulted circuits. The *PSDE* is used to distinguish between faulted and non-faulted circuits when there is a grounded fault occurs in system.

This function provides three operating modes,

- *IN* mode
- *INcosΦ* mode
- *PN* mode

For IN mode, the element starts when all the following conditions are met:

- VN > *VN start value*, and the *VN Supervision time* is expired

- IN > *IN start value*
- Fault occurs in directional characteristic

For INcosΦ mode, the element starts when all the following conditions are met:

- VN > *VN start value*, and the VN Supervision time is expired
- |IN × cos(φN-Ang)| > *IN start value*
- Fault occurs in directional characteristic

For PN mode, the element starts when all the following conditions are met:

- VN > *VN start value*, and the VN Supervision time is expired
- IN > *IN start value*
- |VN × IN × cos (φN-Ang)| > *PN start value*
- Fault occurs in directional characteristic

The protection calculates the active and reactive neutral powers as follows:

PN = IN × VN × cosφN

The φ is the angle of IN relative to VN; IN and VN are inputs to the function.

This element can be set to either:

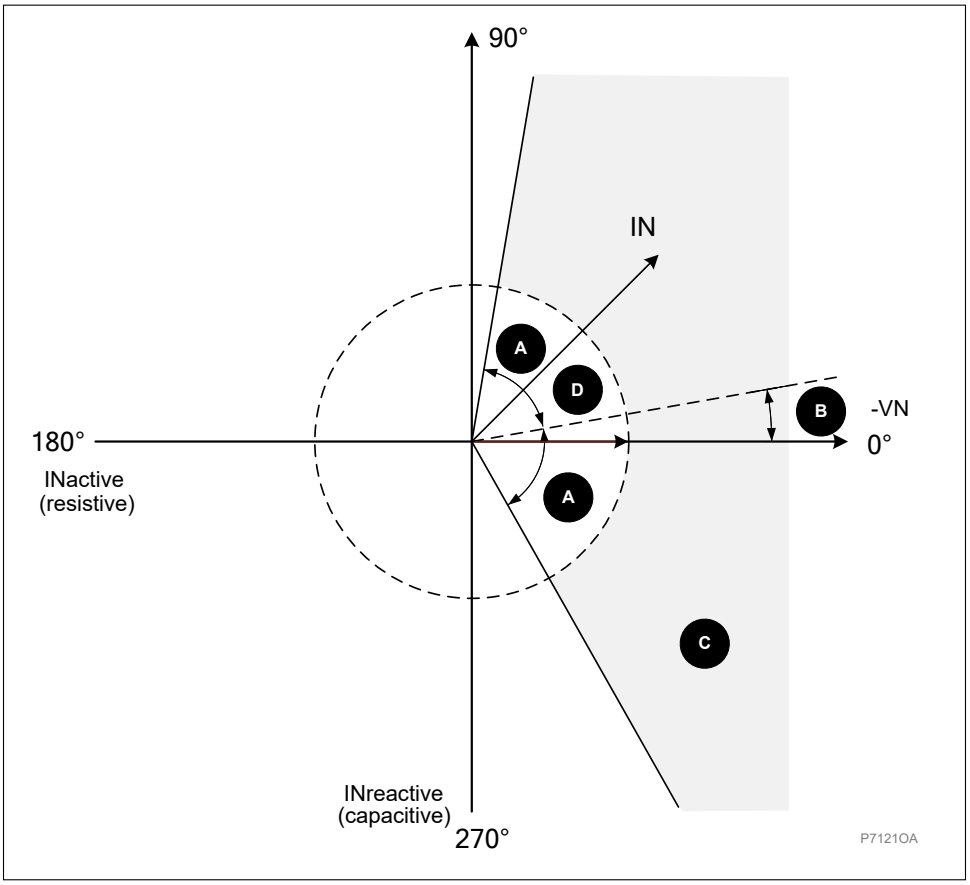
- forward fault zone
- reverse fault zone

The forward zone issues the signal or the trip command during a fault on the downstream side of the protection. The reverse zone issues a signal during a fault on the upstream side of the protection.

The operation area is defined by *Sector angle* and *Characteristic angle* from settings.

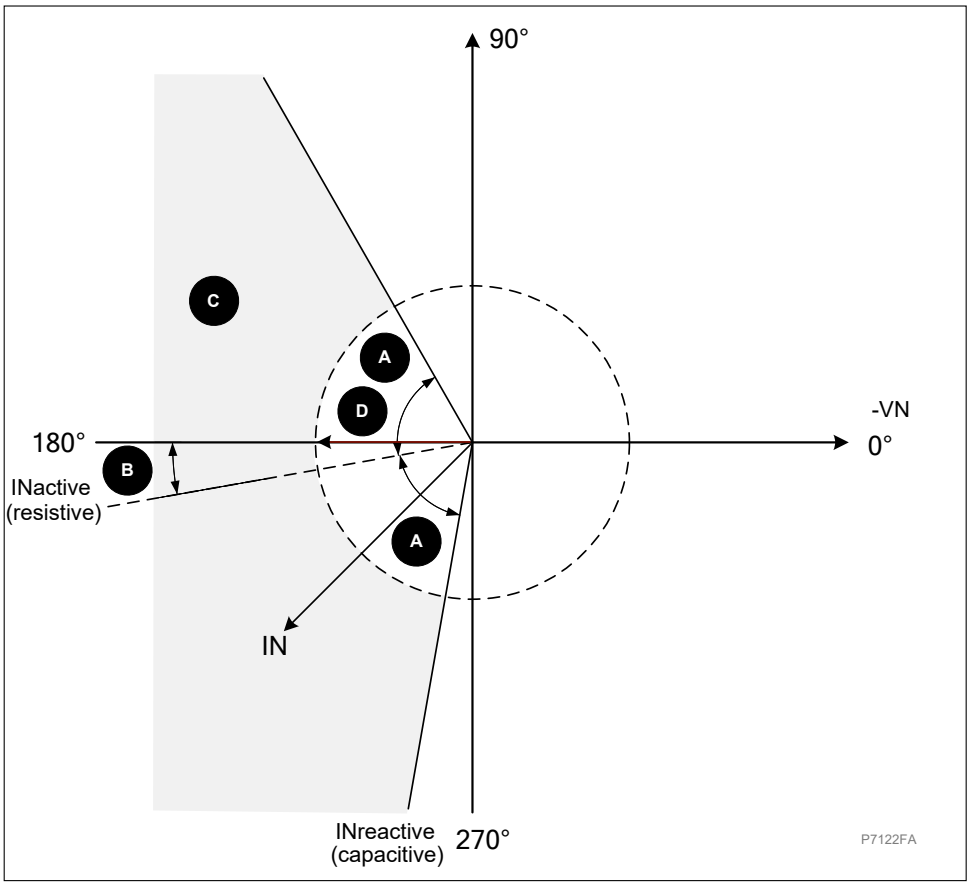
- Forward: 180°-sector+Ang < φN < 180°+sector+Ang
- Reverse: -sector+Ang < φN < sector+Ang

Figure 96 - Operating principle (forward)



A	Sector angle	B	Characteristic angle
C	Forward operate zone	D	Pick-up values

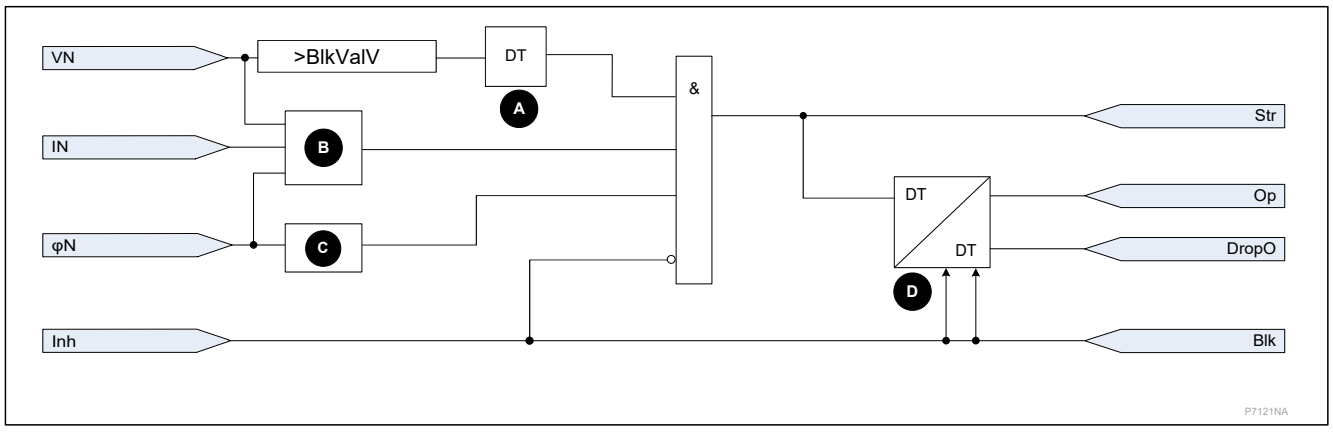
Figure 97 - Operating principle (reverse)



A	Sector angle	B	Characteristic angle
C	Reverse operate zone	D	Pick-up values

Block diagram

Figure 98 - Block diagram of the *PSDE*



A VN Supervision time: *VNSupDlTmms*

B Other pick-up rules:

- IN mode: IN > *IN start value*
- INcosΦ mode: |IN x cos(φN-Ang)| > *IN start value*

- PN mode: IN > *IN start value* & VN x |IN x cos(φN-Ang)| > *PN start value*

C Directional mode:
- Forward: 180°-sector+Ang < φN < 180°+sector+Ang
- Reverse: -sector+Ang < φN < sector+Ang

D DT operate delay: *OpDITmms*

Reset delay: *RsDITmms*

Input and output signals

Table 90 - Input signals of the *PSDE*

Name	Short label	Infotip
IN	IN	IN
VN	VN	VN
Inh[general; neut]	Inhibit	Inhibit function

NOTE: VN should be mapped from three phase VT or single phase VT, and IN should be mapped from single phase CT.

Table 91 - Output signals of the *PSDE*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop Out
Blk	Blocked	Blocked
Phi	Measured angle	Measured angle

Setting parameters

Table 92 - Settings of the *PSDE*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
OpMod	Operation mode	Selects operation based on IN, IN cos (phi) or PN (wattmetric)	• IN • IN cos(phi) • PN		IN
GndStr	IN start value	This must be exceeded in all modes for the element to start	0.001...1 pu	0.001 pu	0.1 pu
BlkValV	VN start value	This must be exceeded in all modes for the element to start	0.01...2 pu	0.01 pu	0.1 pu
BlkValP	PN start value	Wattmetric (PN) start value	0...2 pu	0.001 pu	0 pu
VNSupDITmms	VN supervision time	VN must be present for this period before starting can be confirmed	0...10000000 ms	1 ms	60 ms
OpDITmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	1000 ms
RsDITmms	Reset delay	Reset time delay	0...10000000 ms	1 ms	40 ms

Table 92 - Settings of the *PSDE* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
DirMod	Directional mode	Forward compares IN to -VN. Reverse compares IN to VN.	• Forward • Reverse		Forward
Ang	Characteristic angle	This is the maximum torque angle or the mid point between the directional boundaries of IN to -VN	-179...180 deg	1 deg	0 deg
Sector	Sector angle	This is the angle from the Characteristic angle to the boundary in both directions. Will only affect PN if it crosses its characteristic	1...135 deg	1 deg	90 deg

Characteristics

Table 93 - Characteristics of the *PSDE*

Characteristics		Values
PN start value	Accuracy	±5% or ±0.005 pu
	Reset ratio	90% ± 5%
IN start value	Accuracy	±2% or ±0.001 pu
	Reset ratio	95% ± 5%
VN start value	Accuracy	±2% or ± 0.01 pu
	Reset ratio	98% ± 2%
Boundary	Accuracy	±2°
	Reset ratio	1°
Measured angle	Accuracy	±4°
VN supervision time	Accuracy	±2% or ±10 ms
Operate delay	Accuracy	±2% or ±10 ms
Reset time	Accuracy	±2% or ±30 ms
Characteristic time	Start time	< 40 ms (1.2 Is)
	Reset delay	< 100 ms (0.8 Is)
	Disengaging time	< 50 ms (0 Is)
	Overshoot time	< 50 ms from 10 Is to 0.9 Is

Switch-onto-fault (*PSOF*, ANSI 50HS)

Description

The switch-onto-fault (*PSOF*) is beneficial in situations where an operator closes a circuit breaker onto a fault, such as inadvertently left line earths in the circuit.

For basic protections like the *PHPTOC*, the *PSOF* is often not necessary because these basic protective measures can eventually clear the fault.

However, for applications using directionality, such as directional and distance protection functions, the *PSOF* is normally applied when the Voltage Transformer (VT) is situated on the line side. For a dead short situation, the voltage will be zero and the fault direction cannot be determined. This will normally prevent the high

speed protection function operation. If the protection response is delayed, it will result in a slower trip which may lead to a wider power outage.

The *PSOF* protection function addresses the following two distinct scenarios:

- The *PSOF* activates specific protective elements when a fault is detected upon the manual closing of a circuit breaker. The rapid response can help prevent damage and minimize disruptions.
- Trip on reclose (*TOR*) is triggered by a persistent fault during the auto-reclosing sequence of the circuit breaker, it helps ensure a rapid response to clear the fault.

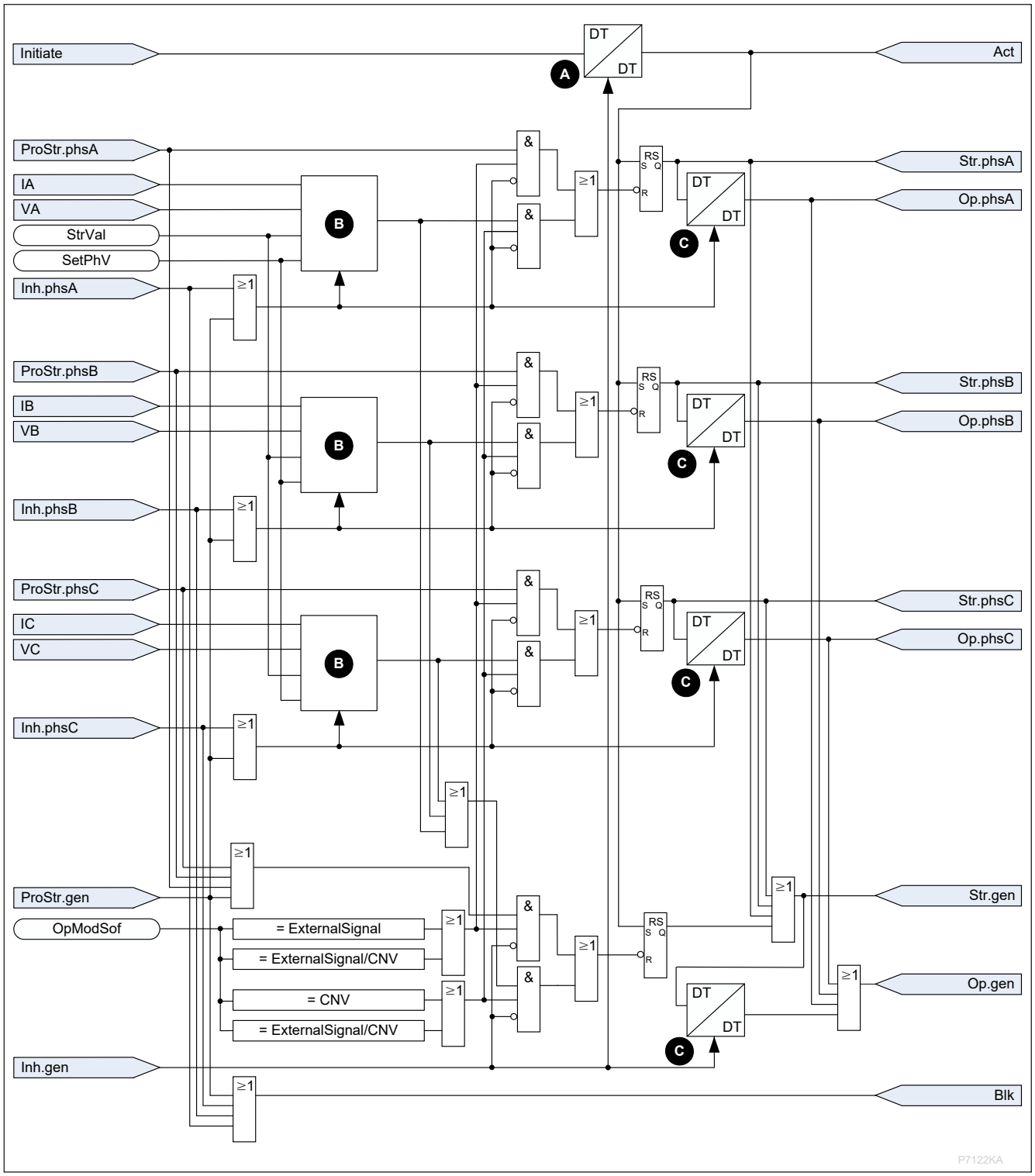
Both the *PSOF* and the *TOR* are integral components of the Trip on close (*TOC*) functionality, which is part of a comprehensive protection strategy for circuit breakers.

Feature overview

- Activation conditions: The system provides the capability to activate the *PSOF* or *TOR* logic using an initiate input signal. This matrix mapped input signal will activate the function with an *activation delay time* and a *release time*.
  - When the *PSOF* or *TOR* is activated by CB closing command signal, the *activation delay time* should be set to *0* ms.
  - When the *PSOF* is activated by bay dead conditions, the *activation delay time* serves to distinguish between a standard open-close sequence where grounding switch closing may not be possible, and the situations where grounding switch closing may be present. It is normally around *200* s.
  - When the *TOR* is activated by bay dead conditions, the *activation delay time* must not exceed the minimum dead time required for auto-reclose as both times start simultaneously and the *TOR* protection must be ready by the time of CB closing on potentially persistent faults.
- Response to operating conditions: If an operating condition, such as an input signal or Current No Volts (CNV) is detected, when the element is activated, the *PSOF* element will initiate operation, including the *Definite Time* (DT) delay operation if required.
- Matrix mapped operating conditions: The operating condition for the element is based on a single input mapped to multiple application function blocks, providing flexibility in the system integration and response.
- *TOR*: The *TOR* operates during the auto reclosing sequence with a reduced activation time when activated by Bay Dead conditions. The basic logic of *TOR* is consistent with *PSOF*. That means *PSOF* is also applicable in scenarios where *TOR* is utilized.

Block diagram

Figure 99 - Block diagram of the *PSOF*

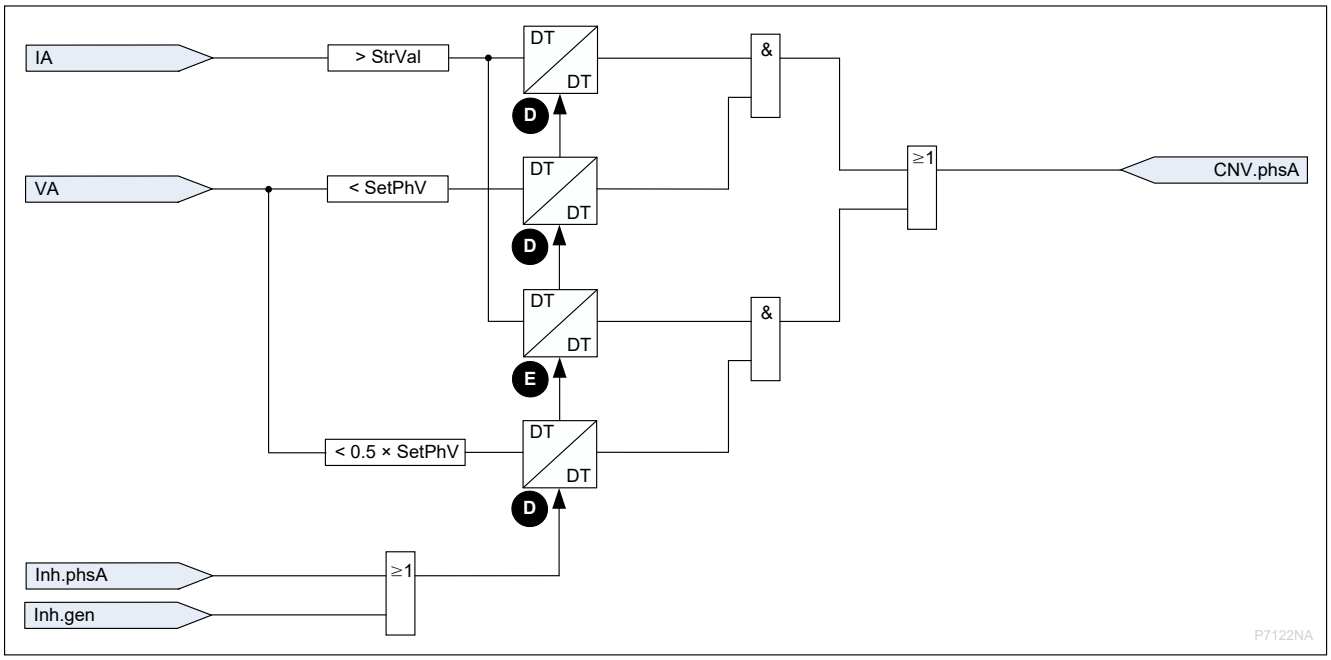


A Activation delay time: *EnaDlTmms*
Release time: *EnaTmms*

B CNV logic

C Operate delay: *OpDlTmms*
Reset delay: 0 ms

Figure 100 - Block diagram of CNV logic (per phase)



D Operate delay: 20 ms
Reset delay: 0 ms

E Operate delay: 10 ms
Reset delay: 0 ms

NOTE: The CNV logic diagram shows the logic of single phase (phase A) and it is the same for other phases.

Input and output signals

Table 94 - Input signals of the *PSOF*

Name	Short label	Infotip
IAIBIC	Phase current	Phase current
VAVBVC	Phase voltage	Phase voltage
Inh[general;phsA; phsB;phsC]	Inhibit	Inhibit function
Initiate	Initiate	Initiate
ProStr[general; phsA;phsB;phsC]	Start	External start signal from protection

Table 95 - Output signals of the *PSOF*

Name	Short label	Infotip
Act	Active	Active
Str	Start	Start
Op	Operate	Operate
Blk	Blocked	Blocked

Setting parameters

Table 96 - Settings of the *PSOF*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
EnaDlTmms	Activation delay	The element is active if the initiate input is active for this period	0...1000000 ms	1 ms	200000 ms
EnaTmms	Release delay	When active the element looks for a start for this period after the initiation deactivates. If a start occurs in this period the element will operate if initiation is maintained for the operate delay	100...10000 ms	1 ms	500 ms
OpModSof	Operation mode	This sets operation based on the start input or current without voltage or both	• External start • Current No Voltage • External start or CNV		External start or CNV
SetPhV	Undervoltage threshold	Phase undervoltage limit for CNV modes	0.02...1.2 pu	0.01 pu	0.6 pu
StrVal	Overcurrent threshold	Phase overcurrent limit for CNV modes	0.005...40 pu	0.001 pu	1 pu
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	0 ms

Characteristics

Table 97 - Characteristics of the *PSOF*

Characteristics		Values
Phase current limit for CNV detector	Accuracy	±2% or ±0.001 pu (sinusoidal input) ±5% or ±0.002 pu (fully offset input) ±5% or ±0.005 pu (under Level 5 power frequency magnetic field)
	Reset ratio	95% ± 5%
Phase voltage limit for CNV detector	Accuracy	±2% or ±0.05 pu
	Reset ratio	102% ± 2%
Activation delay time	Accuracy	±2% or ±20 ms
Operate delay	DT Accuracy	±2% or ±20 ms
Release time	Accuracy	±2% or ±20 ms
Characteristic time	Start time	< 35 ms (2 *StrVal*, 0 *SetPhV*) for *CNV* operation mode < 10 ms for *ExternalSignal* operation mode
	Overshoot time	< 30 ms (2 *StrVal*...0.9 *StrVal*, 0.9 *SetPhV*...1.2 *SetPhV*)

Ground admittance (*EFPADM*, ANSI 21N)

Description

The ground admittance protection function is applied for ground-fault detection on high-resistance grounded, ungrounded or compensated power systems.

This function uses neutral current and voltage to calculate the admittance (YN). Angle correction can be achieved via settings of 1ph CT group if needed.

YN = GN + jBN = IN / -VN = 3I0 / -3V0

Conductance (Gn) is the real part of YN while susceptance (Bn) is the imaginary part of YN.

This function supports over-admittance, over-conductance, over-susceptance or any combination of the three elements. When any of the selected elements meets its operation criteria for the configured operate delay, the function trips.

NOTE:

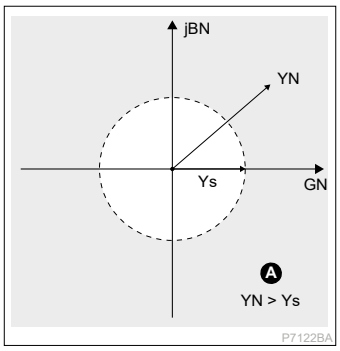
This function starts working only when both the following two conditions are met:

- The neutral voltage is above its configured threshold for the time defined in the *VN supervision time* setting.
- The neutral current is above its configured threshold.

Operation of over-admittance

The over-admittance element is non-directional and trips when the magnitude of admittance exceeds the YN start value for the operate delay.

Figure 101 - Operate zone of over-admittance

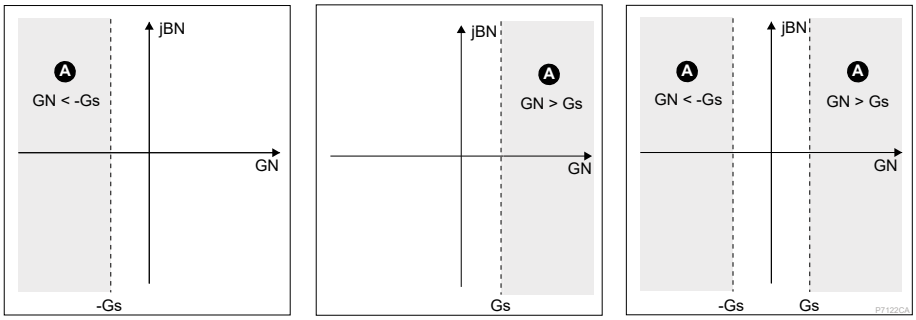


A Operate zone

Operation of over-conductance

The over-conductance element can be set to *reverse*, *forward*, or *non-directional*. When the directional criteria is met and the magnitude of conductance exceeds the GN start value for the operate delay, the element trips.

Figure 102 - Operate zones of over-conductance, for reverse, forward, and non-directional respectively

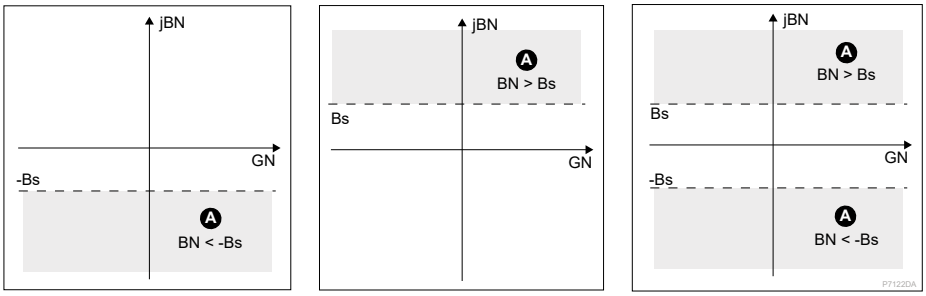


A Operate zone

Operation of over-susceptance

The over-conductance element can be set to *reverse*, *forward*, or *non-directional*. When the directional criteria is met and the magnitude of susceptance exceeds the BN start value for the operate delay, the element trips.

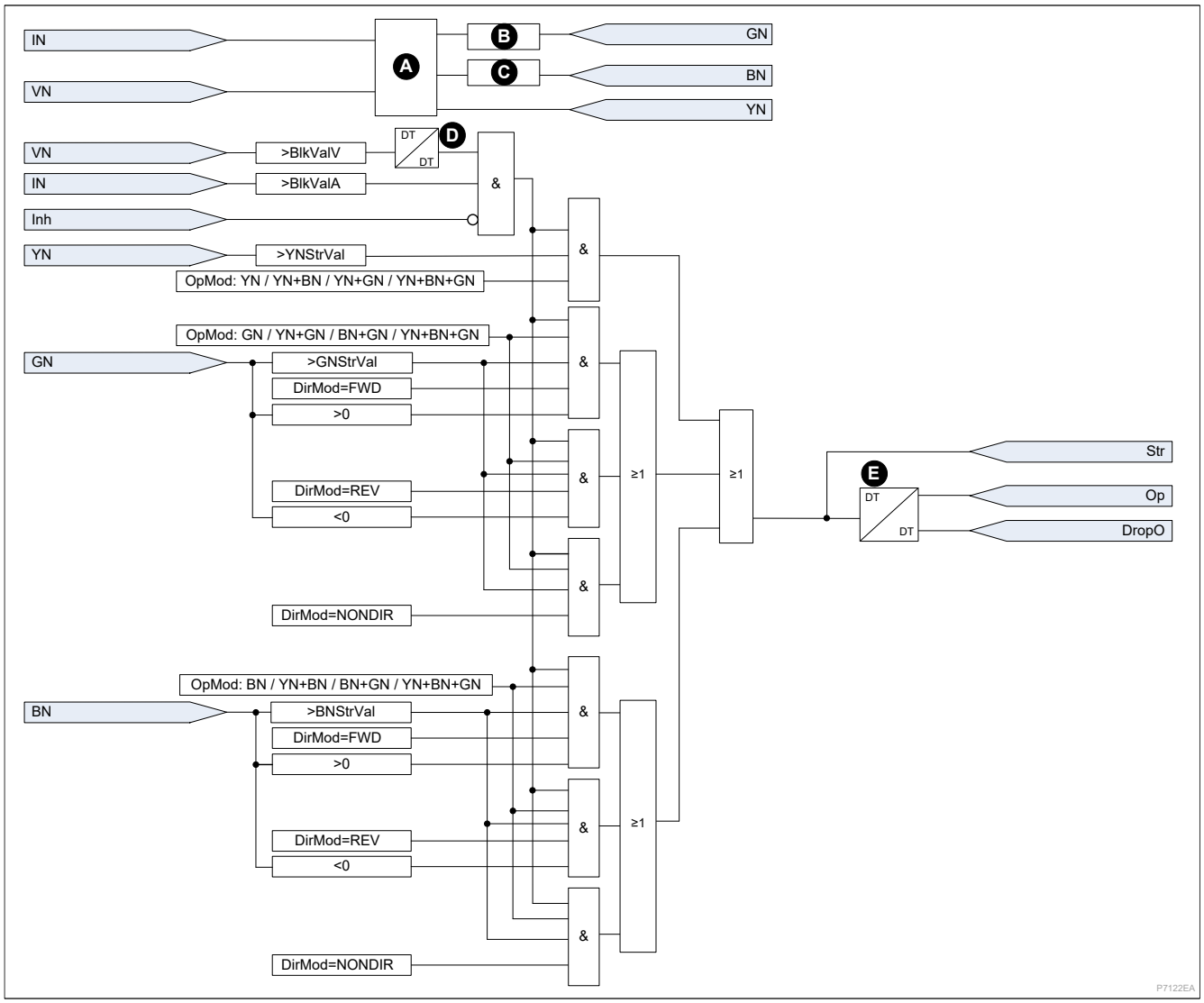
Figure 103 - Operate zones of over-susceptance, for reverse, forward, and non-directional respectively



A Operate zone

Block diagram

Figure 104 - Block diagram of the *EFPADM*



A	Divide	B	Real	C	Imaginary
D	Start Delay: *StrDlTmms*	E	Operate delay: *OpDlTmms* Reset delay: *RsDlTmms*		

Input and output signals

Table 98 - Input signals of the *EFPADM*

Name	Short label	Infotip
Inh[general;neut]	Inhibit	Inhibit function
IN	IN	IN
VN	VN	VN

Table 99 - Output signals of the *EFPADM*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked
YN	YN	YN
BN	BN	BN
GN	GN	GN

Setting parameters

Table 100 - Settings of the *EFPADM*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
OpMod	Operation mode	Select between ground admittance (YN), conductance (GN), susceptance (BN) or a combination of the three	• YN • BN • GN • YN+BN • YN+GN • BN+GN • YN+BN+GN		YN
DirMod	Directional mode	Directional mode of BN/GN	• Non directional • Forward • Reverse		Non direc-tional
YNStrVal	YN start value	YN start value	0.01...2.5 pu	0.01 pu	0.5 pu
BNStrVal	BN start value	BN start value	0.01...1.25 pu	0.01 pu	0.05 pu
GNStrVal	GN start value	GN start value	0.01...1.25 pu	0.01 pu	0.05 pu
StrDlTmms	VN supervision time	VN must be present for this period before starting can be confirmed	0...10000000 ms	1 ms	60 ms
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	1000 ms
RsDlTmms	Reset delay	Reset time delay	0...10000000 ms	1 ms	0 ms

Table 100 - Settings of the *EFPADM* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
BlkValA	Minimum current	Minimum current for operation	0.001...1 pu	0.001 pu	0.1 pu
BlkValV	Minimum voltage	Minimum voltage for operation	0.01...2 pu	0.01 pu	0.1 pu

Characteristics

Table 101 - Characteristics of the *EFPADM*

Characteristics		Values
Start value	Accuracy	±5% or ±0.005 pu
	Reset ratio (hysteresis)	90% ± 5%
VN	Accuracy	±2% or ± 0.01 pu
IN	Accuracy	±2% or ± 0.001 pu
YN, BN, GN	Accuracy	±5% or ±0.005 pu
Boundary BN, GN	Accuracy	±2°
Operate delay	Accuracy	±2% or ±10 ms
	Reset time	<50 ms at 0 Start value)
	Reset time accuracy	±2% or ±30 ms
Characteristic time	Start time	< 100 ms at 1.2 Start value
	Start reset time	< 100 ms at 0.8 Start value
	Overshoot time	< 50 ms (0.9...10 Start value)
Blocked	Block time	< 20 ms
	Reset time	< 40 ms

Undervoltage (*PHPTUV*, ANSI 27)

Description

The undervoltage protection function is used to detect undervoltage conditions to help protect plant under conditions such as:

- Increased system loading which normally is handled by voltage regulating equipment.
- Faults which cause a reduction in the phase voltages associated with the fault.
- Loss of busbar voltage that requires isolation of output circuits.
- Excessive voltage dips that cause motor loads to stall.

The function can measure phase-to-phase or phase-to-neutral voltages and operation can be based on one, two or three elements dropping below the start setting, and a start signal is issued. If the fault situation remains on longer than the operate delay setting, a trip signal is issued. The input voltage may be configured as phase-to-phase or phase-to-ground for 1, 2 or 3 VT phases.

Start signal decision

The function of the start signal decision block is to determine which start signal of the phase will be triggered according to the measurement mode. For example,

- For phase to phase measurements, when VAB is below the threshold, both the start signal of phase A and phase B will be triggered together.
- For phase to ground measurements, when VA is below the threshold, the start signal of phase A will be triggered.

Output condition

The function of the output condition block is to determine which operate signal of the phase will be the output according to the setting *Operation mode*. For example,

- If *Operation mode* = *Three phase*, the operate signal of the three phases will be triggered.
- If *Operation mode* = *Two phase*, when any output of the operate delay of the two phases is true, and the operate signal of the two phases will be triggered; otherwise, the operate signal of the two phases is false.
- If *Operation mode* = *One phase*, the status of the operate signal is the same as the output of operate delay.

Operate characteristic

The undervoltage function operates with either the DT or the IDMT characteristic that is selected. The IDMT characteristic follows the equation below:

$$t = TMS \times \frac{1}{1 - \frac{G}{Gs}}$$

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where:

- t is the operate delay in seconds;
- G is the measured value;
- Gs is the setting value;
- TMS is the time multiplier setting.

Remanent undervoltage application

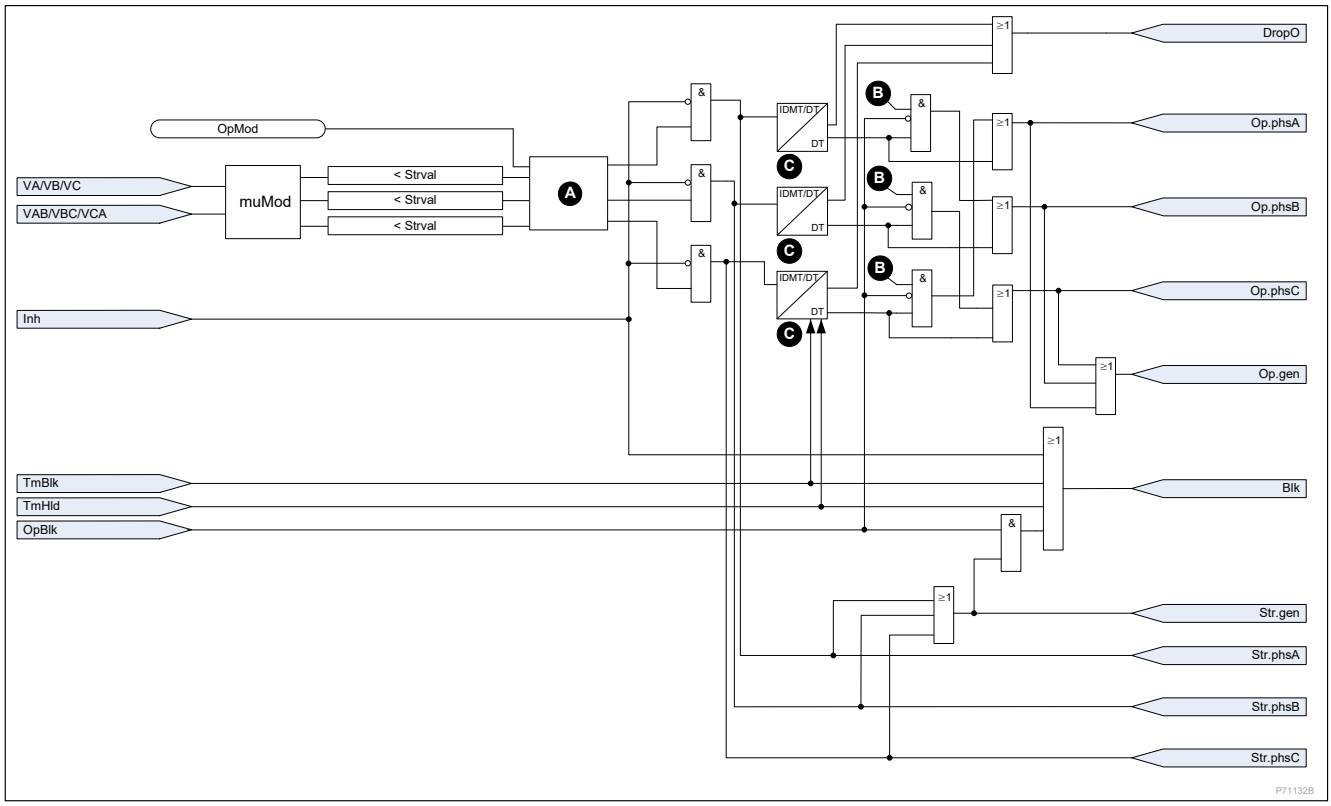
This is used in auto transfer schemes to ensure large motors have been disconnected or run down before transferring to the alternate supply. This helps avoid system shock and possible damage to the motor shaft and windings.

In this application the undervoltage element is measuring the busbar voltage. When the incomer or an upstream breaker opens, the motor will start to run down and back feed other loads if present. Normally the motor breaker will trip on undervoltage, but until this occurs the motor will output a voltage at a frequency proportional to the speed.

The undervoltage element can be used for this application and will function down to 10 Hz. The element will operate when the voltage is below the setting or 10 Hz and indicates to the auto transfer scheme there is no remanent voltage on the bus. It is normally set to 20% nominal volts with a short delay of 100 ms.

Block diagram

Figure 105 - Block diagram of the *PHPTUV*



A	Operation mode.	B	Measurement mode.	C	DT Operate delay: *OpDITmms* IDMT Operate delay: *TmVCrv*, *TMS* Reset delay: *RsDITmms*

Operation mode has three options:

- One phase
- Two phase
- Three phase

When the measurement mode is phase-to-ground, VA is one element triggered (same to VB and VC).

When the measurement mode is phase-to-phase, VAB lower than start value is one element triggered (same to VBC and VCA).

When the triggered elements are more than the setting of operation mode, the start signals can be triggered. Otherwise, even if VA is lower than the start value, but the operation mode is two elements, the start signal of phase A cannot be triggered.

Input and output signals

Table 102 - Input signals of the *PHPTUV*

Name	Short label	Infotip
Inh[general;phsA;phsB;phsC]	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers
OpBlk	Op block	Output blocked when active (timers not held)

Table 102 - Input signals of the *PHPTUV* (Continued)

Name	Short label	Infotip
VAVBVC	Phase voltage	Linked to line voltage input source
UABUBCUCA	Line voltage	Line voltage

Table 103 - Output signals of the *PHPTUV*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked

Setting parameters

Table 104 - Settings of the *PHPTUV*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
MuMod	Measurement mode	Measurement mode	• Phase-phase • Phase-neutral		Phase-phase
OpMod	Operation mode	Selects the number of phases required to start the element	• One phase • Two phase • Three phase		Three phase
TmVCrv	Operating curve	Operating curve	• Inverse • Definite time		
StrVal	Start value	Start value	0.02...1.2 pu	0.01 pu	0.8 pu
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	10 ms	100 ms
Tms	IDMT delay multiplier	IDMT time delay multiplier or TMS	0...20	0.001	1
RsDlTmms	Reset delay	Reset time delay	0...100000 ms	10 ms	100 ms

Characteristics

Table 105 - Characteristics of *PHPTUV*

Characteristics		Values
Start value	Accuracy	±2% or ± 0.05 pu
	Reset ratio	102% ± 2%
Operate delay	DT accuracy	±2% or ±20 ms
	IDMT accuracy	±5% or ±20 ms (according to IEC 60255-127)
Reset time	Accuracy	±2% or ±20 ms
Characteristic time	Start time	< 55 ms (1.2...0.9 pu)
	Overshoot time	< 30 ms (1.2...0.9 pu)

Overvoltage (*PHPTOV*, ANSI 59)

Description

The overvoltage protection function is used to detect system voltages that are too high.

The function measures either phase-to-phase or phase-to-neutral voltage and operation can be on one, two or three elements exceeding the start value.

Start signal decision

The start signal decision block is to determine which start signal of the phase will be triggered according to the measurement mode. For example,

- For phase to phase measurements, when VAB is over the threshold, both the start signal of phase A and phase B will be triggered together.
- For phase to ground measurements, when VA is over the threshold, the start signal of phase A will be triggered.

Output condition

The output condition block is to determine which operate signal of the phase will be the output according to the setting of the operation mode. For example,

- If the setting is three-phase, the operate signal of the three-phase will be triggered.
- If the setting is two-phase, when any output of the operate delay of the two-phase is true, the operate signal of these two-phase will be triggered, otherwise, the operate signal of all phases is false.
- If the setting is any phase, the status of the operate signal is same as the output of operate delay.

Operate characteristic

The overvoltage function operates with either the DT or the IDMT characteristic that is selected. The IDMT characteristic follows the equation below:

$$t = TMS \times \frac{1}{\frac{G}{Gs} - 1}$$

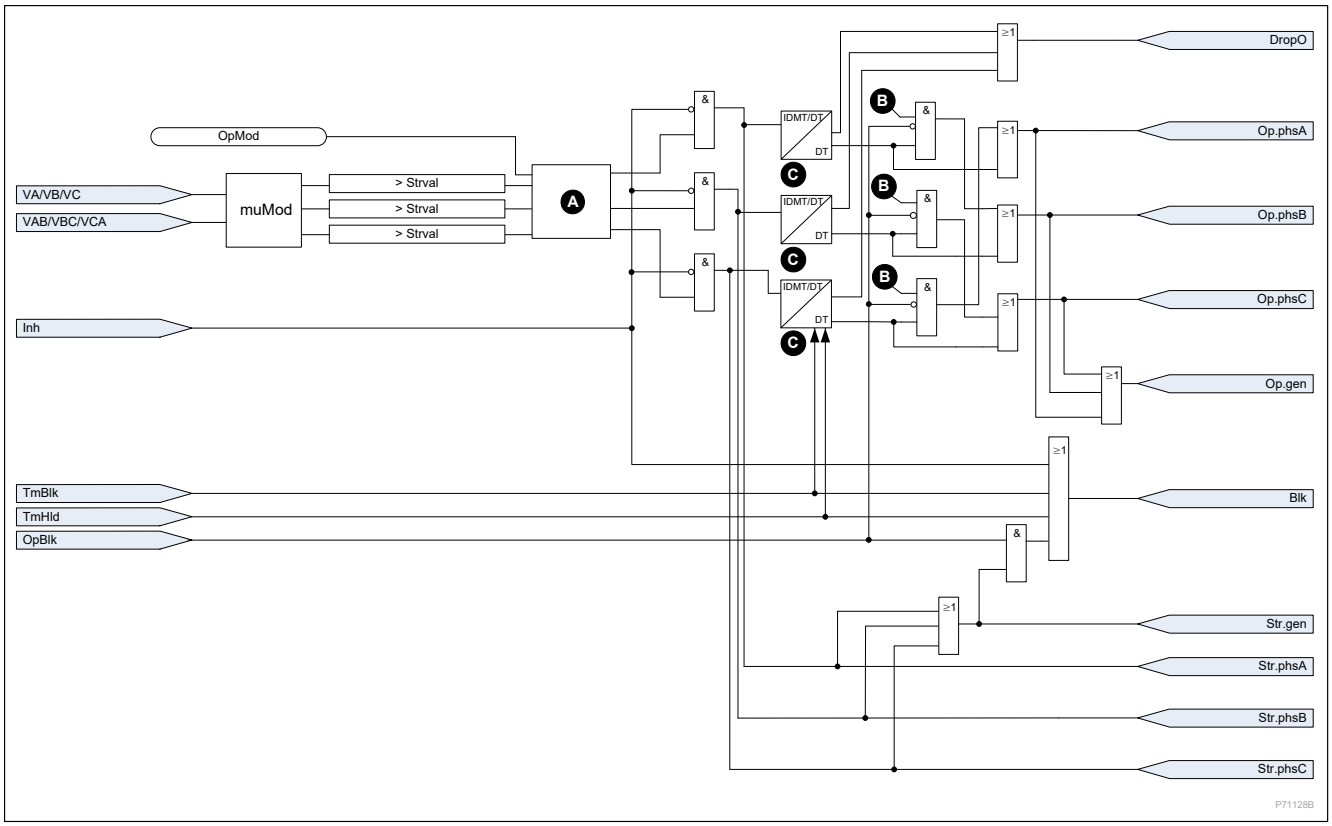
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where:

- *t* is the operate delay in seconds;
- *G* is the measured value;
- *Gs* is the setting value;
- *TMS* is the time multiplier setting.

Block diagram

Figure 106 - Block diagram of the *PHPTOV*



A	Operation mode	B	Measurement mode	C	DT Operate delay: *OpDITmms* IDMT Operate delay: *TmVCrv*, *TMS* Reset delay: *RsDITmms*

Operation mode has three options:

- any element
- two elements
- three elements

When the measurement mode is phase-to-ground, VA is one element triggered (same to VB and VC).

When the measurement mode is phase-to-phase, VAB is one element (same to VBC and VCA).

When the triggered elements are more than the setting of operation mode, the start signals can be triggered. Otherwise, even if VA is lower than the start value, but the operation mode is two elements, the start signal of phase A cannot be triggered.

Input and output signals

Table 106 - Input signals of the *PHPTOV*

Name	Short label	Infotip
Inh[general;phsA;phsB;phsC]	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers
OpBlk	Op block	Output blocked when active (timers not held)

Table 106 - Input signals of the *PHPTOV* (Continued)

Name	Short label	Infotip
VAVBVC	Phase voltage	Linked to line voltage input source
UABUBCUCA	Line voltage	Line voltage

Table 107 - Output signals of the *PHPTOV*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked

Setting parameters

Table 108 - Settings of the *PHPTOV*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
MuMod	Measurement mode	Measurement mode	• Phase-phase • Phase-neutral		Phase-phase
OpMod	Operation mode	Selects the number of phases required to start the element	• One phase • Two phase • Three phase		Three phase
TmVCrv	Operating curve	Operating curve	• Inverse • Definite time		
StrVal	Start value	Start value	0.02...1.5 pu	0.01 pu	1.2 pu
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	10 ms	100 ms
Tms	IDMT delay multiplier	IDMT time delay multiplier or TMS	0...20	0.001	1
RsDlTmms	Reset delay	Reset time delay	0...100000 ms	10 ms	100 ms

Characteristics

Table 109 - Characteristics of the *PHPTOV*

Characteristics		Values
Start value	Accuracy	±2% or ± 0.05 pu
	Reset ratio	98% ± 2%
Operate delay	DT accuracy	±2% or ±20 ms
	IDMT accuracy	±5% or ±20 ms (according to IEC 60255-127)
Reset time	Accuracy	±2% or ±20 ms
Characteristic time	Start time	< 50 ms (0.9...1.1 pu)
	Overshoot time	< 30 ms (0.9...1.1 pu)

Positive phase sequence undervoltage (*PPSPTUV*, ANSI 27P)

Description

The positive phase sequence undervoltage protection function helps protect motors against faulty operation due to insufficient or unbalanced network voltage.

This undervoltage protection function calculates the positive sequence of the fundamental frequency component *V1*.

By using the positive sequence, all three phases are supervised, with one value, and if the motor loses the connection to the network (loss of mains), the undervoltage situation is detected even if the frequency decreases significantly from nominal frequency.

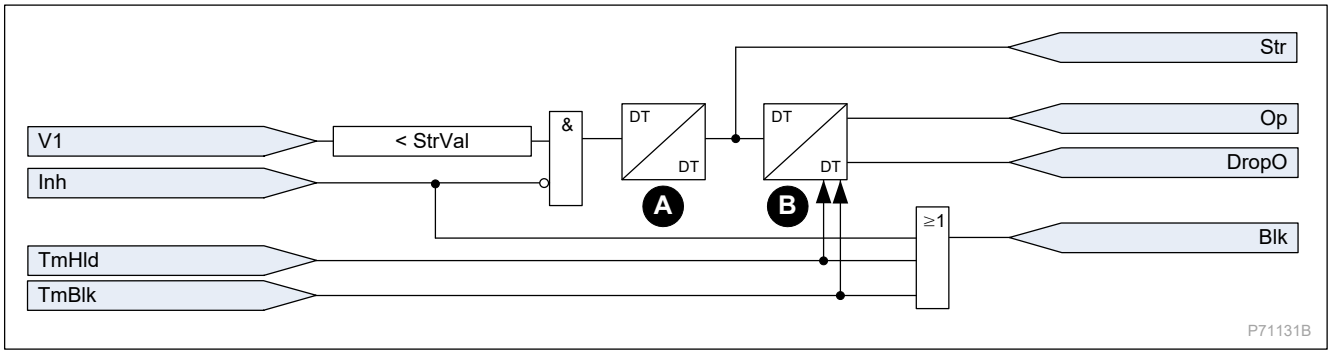
Whenever the positive sequence voltage *V1* drops below the start setting of a particular stage, this stage activates and a start signal is issued. If the fault situation remains on longer than the time defined in the operate delay setting, a trip signal is issued.

Blocking during breaker open

As this element is normally used for starting supervision, it is not blocked by default when the bay is dead. If the element is used for tripping, the *BayDead* signal can be linked to the inhibit operation when the breakers are open.

Block diagram

Figure 107 - Block diagram of the *PPSPTUV*



A	Operate delay: 20 ms Reset delay: 0 ms	B	Operate delay: *OpDITmms* Reset delay: *RsDITmms*

Input and output signals

Table 110 - Input signals of the *PPSPTUV*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers

Table 110 - Input signals of the *PPSPTUV* (Continued)

Name	Short label	Infotip
OpBlk	Op block	Output blocked when active (timers not held)
V1	V1	V1

Table 111 - Output signals of the *PPSPTUV*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked

Setting parameters

Table 112 - Settings of the *PPSPTUV*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrVal	Start value	Start value	0.01...2 pu	0.01 pu	0.7 pu
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	0 ms
RsDlTmms	Reset delay	Reset time delay	0...10000000 ms	1 ms	0 ms

Characteristic

Table 113 - Characteristics of the *PPSPTUV*

Characteristics		Values
Start value	Accuracy	±1% or ± 0.05 pu
	Reset ratio	102% ± 2%
Operate delay	Accuracy	±1% or ±10 ms
Reset time	Accuracy	±2% or ±30 ms
Characteristic time	Start time	< 50 ms
	Overshoot time	< 70 ms

Positive phase sequence overvoltage (*PPSPTOV*, ANSI 59)

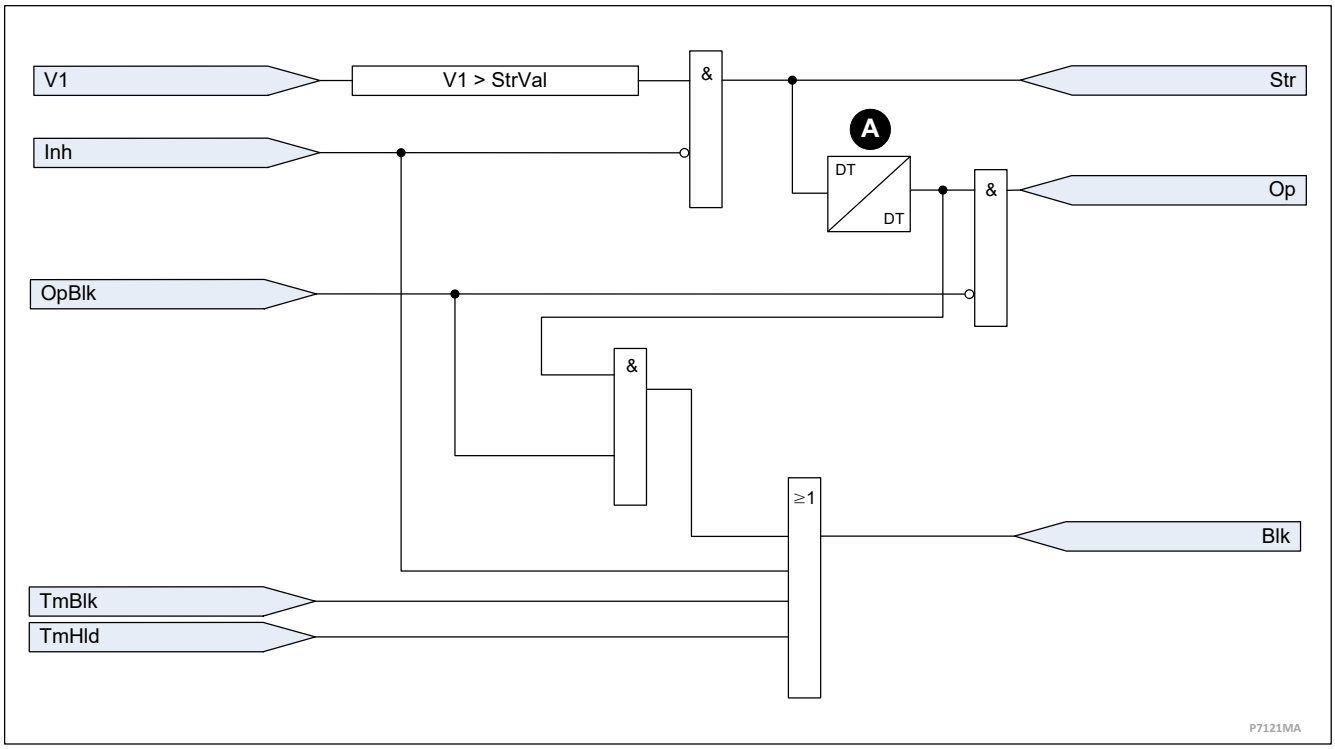
Description

The positive phase sequence overvoltage protection function is applied to help protect plant from faulty operation caused by network overvoltage.

This function uses the positive sequence voltage as its main input to supervise all three phases. Once the positive sequence voltage exceeds the start value, a start signal is issued. If the fault condition remains longer than the operate delay setting, a trip signal is issued.

Block Diagram

Figure 108 - Block diagram of the *PPSPTOV*



A Operate delay: *OpDITmms*
Reset delay: *RsDITmms*

Input and output signals

Table 114 - Input signals of the *PPSPTOV*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers
OpBlk	Op block	Output blocked when active (timers not held)
V1	V1	V1

Table 115 - Output signals of the *PPSPTOV*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked

Setting parameters

Table 116 - Settings of the *PPSPTOV*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrVal	Start value	Start value	0.01...2 pu	0.01 pu	1.1 pu
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	0 ms
RsDlTmms	Reset delay	Reset time delay	0...10000000 ms	1 ms	0 ms

Characteristics

Table 117 - Characteristics of the *PPSPTOV*

Characteristics		Values
Start value	Accuracy	±1% or ± 0.05 pu
	Reset ratio	98% ± 2%
Operate delay	Accuracy	±1% or ±10ms
Characteristic time	Start time	< 50 ms at 1.2 Vs
	Reset delay	±2% or ± 20 ms
	Overshoot time	< 70 ms

Neutral overvoltage (*EFPTOV*, ANSI 59N)

Description

The neutral overvoltage protection function is used as non-selective backup for ground faults and also for selective ground fault protection for motors having a unit transformer between the motor and the busbar.

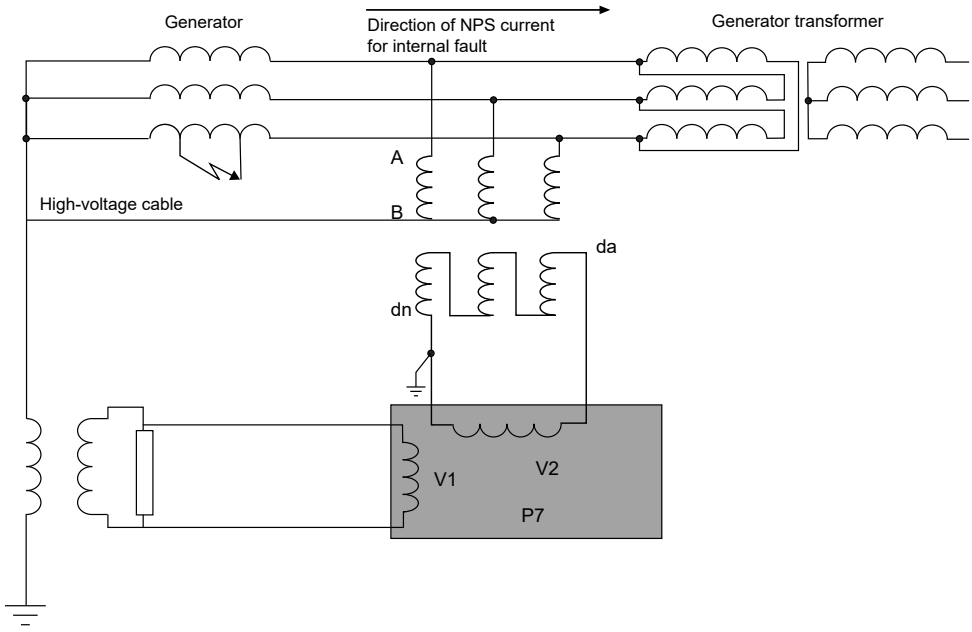
This function is sensitive to the fundamental frequency component of the neutral displacement voltage. The attenuation of the third harmonic is more than 60 dB because the third harmonics is present between the neutral point and ground even when there is no ground fault.

Whenever the measured value exceeds the start setting of a particular stage, this stage starts and issues a start signal. If the fault situation is present longer than the operate delay setting, a trip signal is issued.

Generator inter-turn overvoltage application

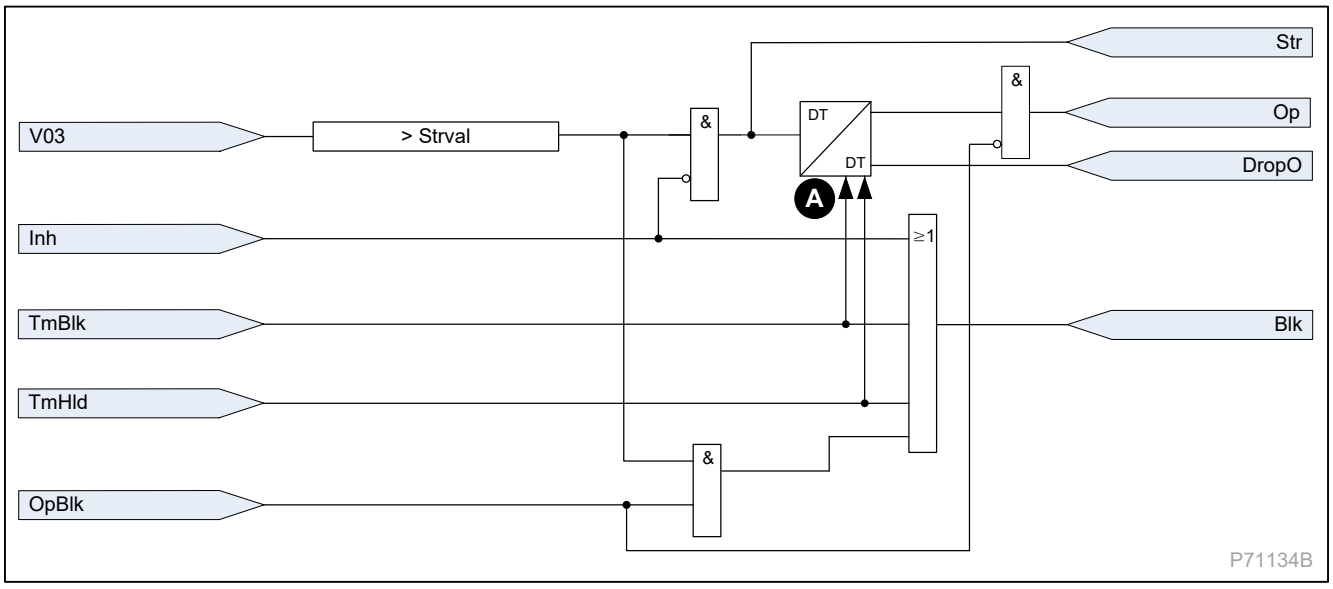
Inter-turn faults in a generator with a single winding can be detected by observing the zero sequence voltage across the machine. Normally, no zero sequence voltage should exist but a short circuit of one or more turns on one phase will cause the generated Electro Motive Force (EMF) to contain some zero sequence component. This method of inter-turn protection requires a dedicated insulated VT with its neutral connected to the generator star point. The VT will normally provide a broken delta secondary which can be monitored by an *EFPTOV* element.

Figure 109 - Inter-turn protection (V2) and ground fault protection (V1) by zero sequence voltage



Block diagram

Figure 110 - Block diagram of the *EFPTOV*



A Operate delay: *OpDITmms*
Reset delay: *RsDITmms*

Input and output signals

Table 118 - Input signals of the *EFPTOV*

Name	Short label	Infotip
Inh	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers

Table 118 - Input signals of the *EFPTOV* (Continued)

Name	Short label	Infotip
OpBlk	Op block	Output blocked when active (timers not held)
VEF	VN	VN

Table 119 - Output signals of the *EFPTOV*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked

Setting parameters

Table 120 - Settings of the *EFPTOV*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrVal	Start value	Start value	0.005...2 pu	0.001 pu	0.2 pu
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	100 ms
RsDlTmms	Reset delay	Reset time delay	0...10000000 ms	1 ms	100 ms

Characteristics

Table 121 - Characteristics of the *EFPTOV*

Characteristics		Values
Start value	Accuracy	±2% or ±0.001 pu
	Reset ratio	98% ± 2%
Operate delay	Accuracy	±2% or ±10 ms
Reset time	Accuracy	±2% or ±30 ms
Characteristic time	Start time	< 50 ms at 1.2 Vs
	Start reset time	< 30 ms at 0.9 Vs
	Disengaging time	< 30 ms 0 Vs
	Overshoot time	< 30 ms

Negative phase sequence overvoltage (*NPSPTOV*, ANSI 47)

Description

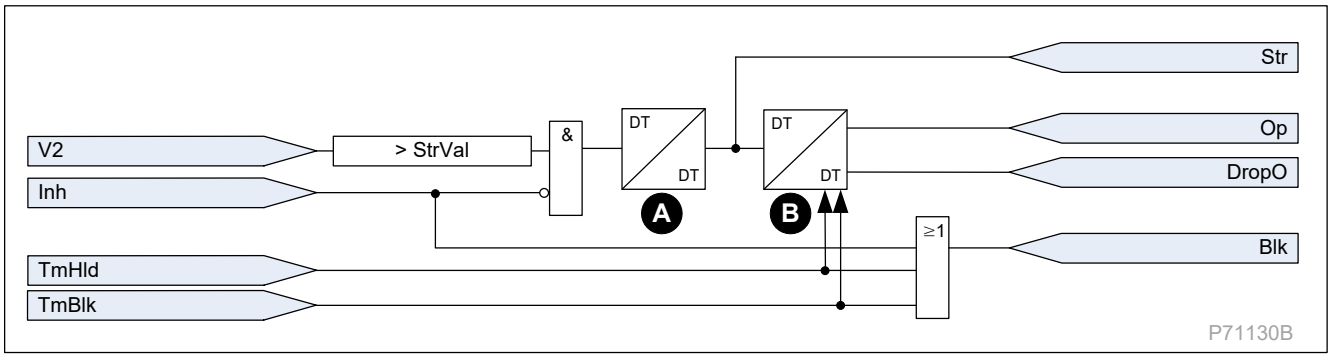
The negative phase sequence overvoltage protection monitors the voltage phase sequence detecting a reverse rotation or voltage unbalance due to a missing

(asymmetrical) phase. The detection of these conditions is used to trip the machine and prevent damage to both the motor and the mechanically coupled process. If the negative sequence voltage input exceeds the voltage setting, this function starts instantaneously, and it operates with the definite time delay.

This protection stage has a settable *Reset delay* that enables the detection of intermittent faults. This means that the Operate delay timer does not reset immediately after the fault is cleared, but resets after the *Reset delay* has elapsed. If the fault appears again before the *Reset delay* has elapsed, the Operate delay timer continues from the previous value, the function eventually trips if faults are occurring often enough.

Block diagram

Figure 111 - Block diagram of the *NPSPTOV*



A	Operate delay: 20 ms Reset delay: 0 ms	B	Operate delay: *OpDITmms* Reset delay: *RsDITmms*

Input and output signals

Table 122 - Input signals of the *NPSPTOV*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers
OpBlk	Op block	Output blocked when active (timers not held)
V2	V2	V2

Table 123 - Output signals of the *NPSPTOV*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked

Setting parameters

Table 124 - Settings of the *NPSPTOV*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrVal	Start value	Start value	0.01...2 pu	0.01 pu	0.2 pu
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	0 ms
RsDlTmms	Reset delay	Reset time delay	0...10000000 ms	1 ms	0 ms

Characteristics

Table 125 - Characteristics of the *NPSPTOV*

Characteristics		Values
Start value	Accuracy	±2% or ± 0.001 pu
	Reset ratio	95% ± 5%
Operate delay	Accuracy	±2% or ±10 ms
Reset time	Accuracy	±2% or ±30 ms
Characteristic time	Start time	< 50 ms at 1.2 Vs
	Start reset time	< 30 ms at 0.9 Vs
	Disengaging time	< 30 ms at 0 Vs
	Overshoot time	< 30 ms

Inter-turn overvoltage (*ITPTOV*, ANSI 59IT)

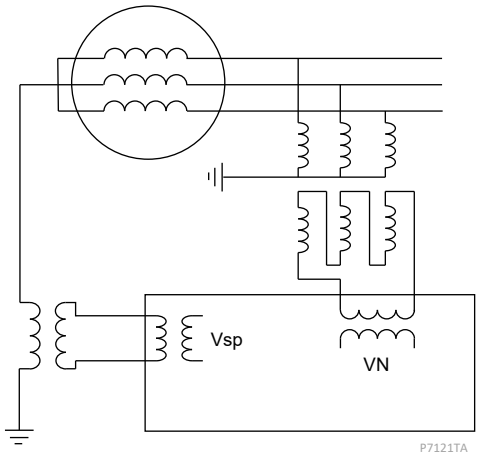
Description

The inter-turn overvoltage protection function is applied to help detect inter-turn faults. For higher sensitivity, this function is normally applied to generators whose stator winding has limited branches and turns, such as large steam generators.

This function does not require a dedicated inter-turn VT, but instead uses the inter-turn voltage calculated from the star point voltage (Vsp) and the summated three-phase voltage (VN). When the calculated inter-turn voltage exceeds the start value for the configured operate delay, a trip signal is sent.

The third harmonic voltage generated by the stator winding imbalance is filtered out for better performance.

Figure 112 - Measurement points for inter-turn voltage calculation



Inter-turn voltage calculation

The inter-turn voltage is calculated as follows:

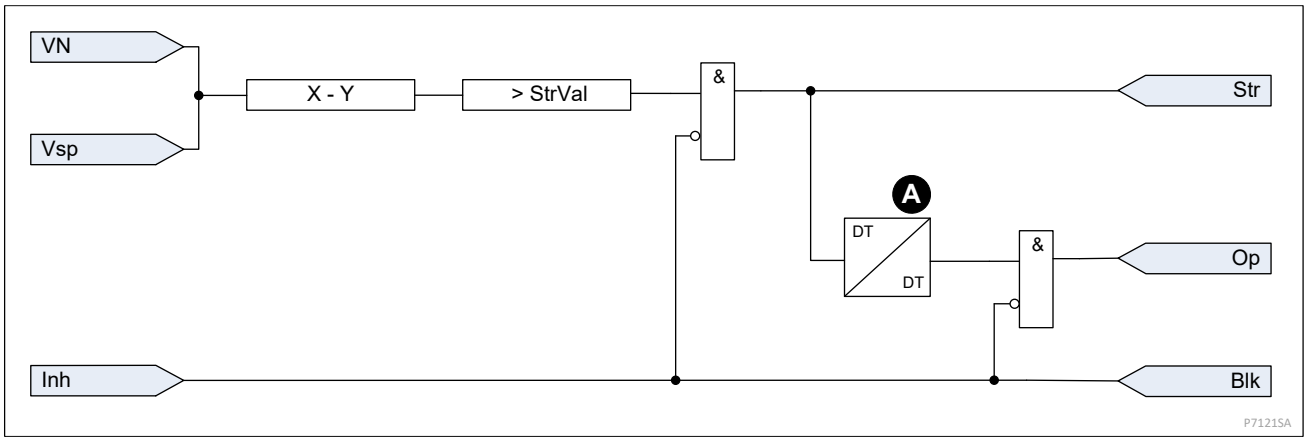
$$V_{IT} = VN - V_{sp}$$ P7121UA

VN is the summated three-phase voltage, which is either calculated by adding all three phase voltages together for the 3ph connection, or directly measured for the 3ph+N and 2pp+N connections.

Vsp is the measured star point voltage.

Block diagram

Figure 113 - Block diagram of the *ITPTOV*



A Operate delay: *OpDITmms*
Reset delay: 0 ms

Input and output signals

Table 126 - Input signals of the *ITPTOV*

Name	Short label	Infotip
Inh	Inhibit	Inhibit function
VEF	Terminal VN	Terminal VN
VSPN	Star point VN	Star point VN

Table 127 - Output signals of the *ITPTOV*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
Blk	Blocked	Blocked

Setting parameters

Table 128 - Settings of the *ITPTOV*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrVal	Start value	Start value	0.005...5 pu	0.001 pu	0.01 pu
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	100 ms

Characteristics

Table 129 - Characteristics of the *ITPTOV*

Characteristics		Values
Start value	Accuracy	±2% or ±0.001pu
	Reset ratio (hysteresis)	95% ± 5%
Operate delay	Accuracy	±2% or ±10 ms
	Reset time	< 30 ms at 0 Vs
Characteristic time	Start time	< 25 ms at 1.2 Vs
	Start reset time	< 30 ms at 0.9 Vs
	Overshoot time	< 30 ms at 0.9...10 Vs
Blocked	Block time	< 20 ms
	Reset time	< 40 ms

Overfluxing (*PVPH*, ANSI 24)

Description

The overfluxing protection function is applied to help protect transformers and generators from excessive magnetic flux, which induces excessive magnetizing

current and, in turn, results in overheating and possible insulation failure. Excessive magnetic flux can be caused by voltage increase, frequency decrease, or both. The higher the V/Hz ratio, the greater the magnetic flux and the risk of damage.

This function uses the V/Hz ratio to monitor the magnetic flux in the iron core of the plant. When calculating the V/Hz ratio, the voltage value is taken from the maximum of the phase-to-phase voltages for delta windings, the maximum of the phase-to-ground voltages for solidly earthed star windings, or the maximum phase to phase voltage minus zero sequence voltage for resistance earthed windings.

When the V/Hz ratio exceeds the alarm threshold setting long enough, an alarm is raised. When the V/Hz ratio exceeds the start value setting, the functions uses either a DT timer or IDMT curves to determine the operate delay, after which the function trips.

NOTE:

- If the V/Hz ratio returns below the alarm threshold before an alarm is raised, the alarm timer instantly resets.
- If the V/Hz ratio returns below the start value before a trip is triggered, the start signal resets after the configured *Reset time*.
- If the operate delay is lower than the *Time to operate alarm value* setting, an alarm is raised.

Operate delay

When *Operating curve* is set to *Definite Time*, the operate delay is fixed to the value from setting *DT/IDMT adder op delay*.

Otherwise, the operate delay is the sum of the calculated t_{op} and *DT/IDMT adder op delay*, as detailed below:

- When *Operating curve* is set to *Type A*, t_{op} is calculated with the following formula:

$$t_{op} = \frac{TMS}{(M-1)^{0.5}}$$ E71199E

- When *Operating curve* is set to *Type B*, t_{op} is calculated with the following formula:

$$t_{op} = \frac{TMS}{(M-1)}$$ E71199D

- When *Operating curve* is set to *Type C*, t_{op} is calculated with the following formula:

$$t_{op} = \frac{TMS}{(M-1)^{2}}$$ E71199C

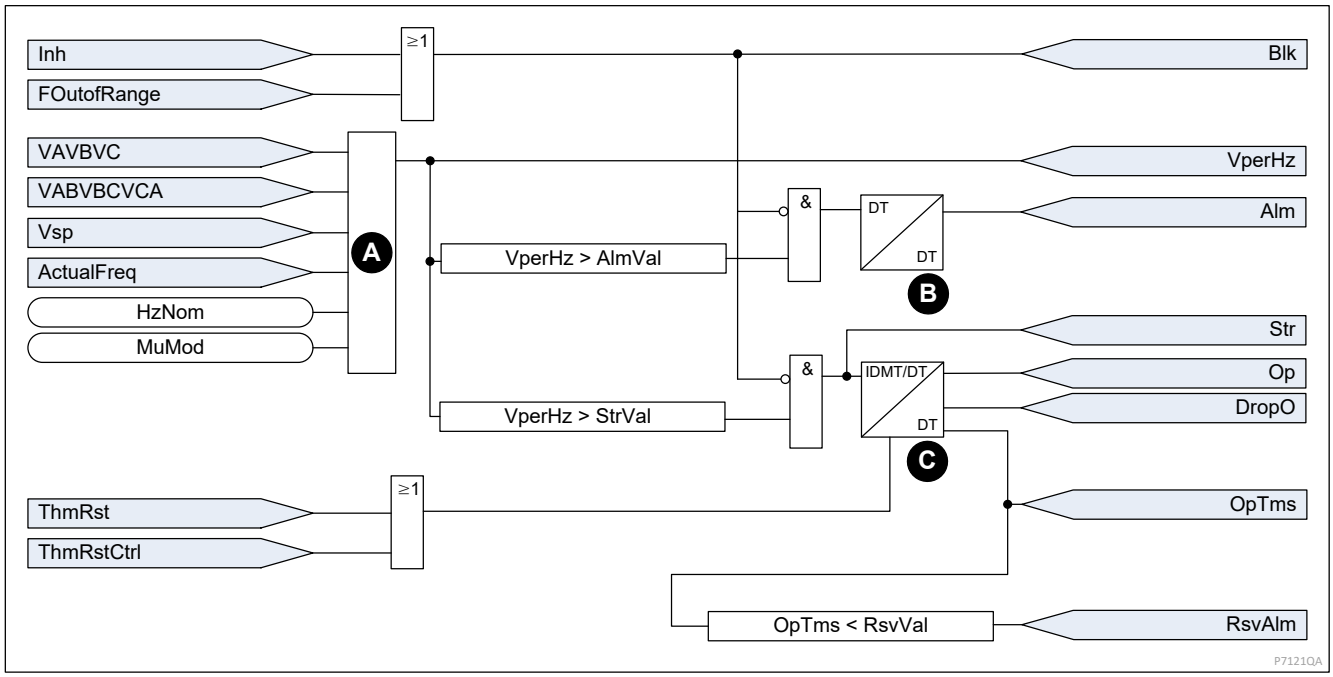
TMS is the *IDMT delay multiplier* setting;

M is the V/Hz ratio divided by the start value.

NOTE: When the calculated t_{op} exceeds *Max op delay*, *Max op delay* is used as t_{op}; when the calculated t_{op} is lower than *Min op delay*, *Min op delay* is used as t_{op}.

Block diagram

Figure 114 - Block diagram of the *PVPH*



A	VperHz calculation	B	Alarm delay: *AlmDlTmms* Alarm Reset delay: 0 ms
C	DT Operate delay: *OpDlTmms* IDMT Operate delay: Calculated with *TmMult*, *OpDlTmms*, *MinOpTmms*, *MaxOpTmms* DT Reset delay: *RsDlTmms* IDMT Reset delay: *RsDlTmms*		

Input and output signals

Table 130 - Input signals of the *PVPH*

Name	Short label	Infotip
VAVBVC	Phase voltage	Linked to line voltage input source
UABUBCUCA	Line voltage	Line voltage
V0	V0	Linked to line voltage input source
ActualFreq	Frequency	Internal signal from FTGAPC1
Inh[general;phsA;phsB;phsC]	Inhibit	Inhibit function

Table 131 - Output signals of the *PVPH*

Name	Short label	Infotip
Alm	Alarm	Alarm
Str	Start	Start
OpTms	Time to operate	Time to operate
RsvAlm	Time to operate alarm	Time to operate Alarm
Op	Operate	Operate
DropO	Drop out	Drop out

Table 131 - Output signals of the *PVPH* (Continued)

Name	Short label	Infotip
Blk	Blocked	Blocked
VperHz	V/Hz	V/Hz

Setting parameters

Table 132 - Settings of the *PVPH*

Name	Short label	Infotip	Setting Range	Step Size	Default Setting
SetMod	Function status	Function status	• On • Off		Off
MuMod	Measurement mode	Measurement mode	• Phase-phase • Phase-neutral • Phase-neutral - V0		Phase-phase
AlmVal	Alarm value	Alarm value	1...2 pu	0.01 pu	1.05 pu
AlmDlTmms	Alarm delay	Alarm time delay	0...10000000 ms	1 ms	10000 ms
StrVal	Start value	Start value	1...2 pu	0.01 pu	1.1 pu
VHzCrv	Operating curve	Type A is an inverse curve. Type B is very inverse and Type C is extremely inverse	• Definite time • Type A • Type B • Type C		
OpDlTmms	DT/IDMT adder op delay	Time delay in DT mode. In IDMT modes this time delay is added to the curve operating time delay	0...10000000 ms	1 ms	0 ms
TmMult	IDMT delay multiplier	IDMT time delay multiplier or TMS	0.01...12	0.01	1
MinOpTmms	Min op delay	For IDMT curves this is the minimum tripping time delay excluding IDMT adder. Usually used to coordinate with downstream fuses. A zero setting means the curve determines the minimum time delay	0...100000 ms	1 ms	0 ms
MaxOpTmms	Max op delay	Maximum operating time when V/Hz exceeds the start value excluding the IDMT adder	10000...10000000 ms	1 ms	100000 ms
RsDlTmms	Reset delay	Reset time delay	0...10000000 ms	1 ms	100 ms
RsvVal	Time to operate alarm value	Time to operate alarm value	1...1000 s	1 s	60 s

Characteristics

Table 133 - Characteristics of the *PVPH*

Characteristics		Values
Start value	Accuracy	±2%
	Reset ratio (hysteresis)	98% ± 2%
Operate delay	DT accuracy	±2% or ±20 ms
	IDMT accuracy	±5% or ±40 ms
V/Hz	Accuracy	±2%

Table 133 - Characteristics of the *PVPH* (Continued)

Characteristics		Values
Time to operate	Accuracy	±5% or ± 40ms
Time to operate alarm value	Accuracy	±5% or ± 40ms
Characteristic time	Start time (non-directional)	< 40 ms (0.9...1.1 Start value)
	Start reset time	< 50 ms (0.9...1.1 Start value)
	Overshoot time	< 40 ms (0.9...1.1 Start value)
	Block pickup time	< 20 ms
	Block reset time	20...40 ms

Overfrequency (*PTOF*, ANSI 81O)

Description

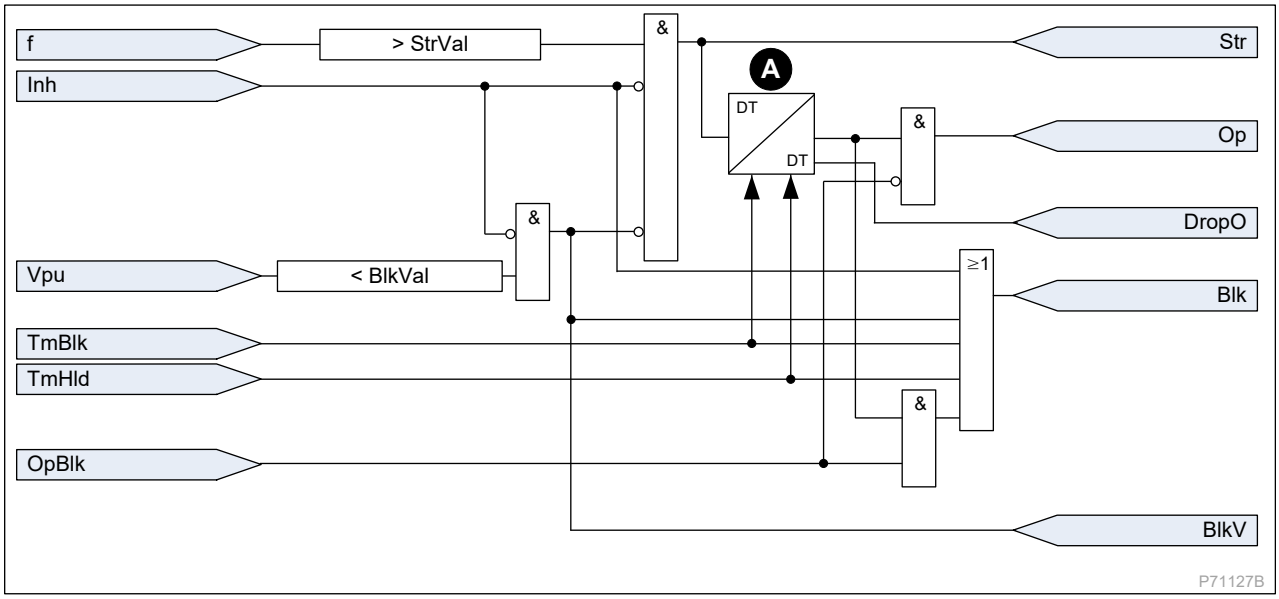
The overfrequency protection function detects the abnormally high frequency compared to the rated frequency to monitor power supply quality or help protect a generator against overspeed conditions.

The overfrequency protection function is generally applied where the generation capacity is greater than the connected load to prevent the system frequency from increasing above a specified threshold and subjecting the generator to an overspeed condition.

This protection is used in load restoration schemes to detect that the power system frequency is recovered sufficiently to allow load which is previously shed to be reconnected. The frequency measurement is fixed to the bay VT input.

Block diagram

Figure 115 - Block diagram of the *PTOF*



A Operate delay: *OpDITmms*
Reset delay: *RsDITmms*

Input and output signals

Table 134 - Input signals of the *PTOF*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers
OpBlk	Op block	Output blocked when active (timers not held)
Freq	Frequency	Internal signal from FTGAPC1
V1	V1	Internal signal from PHTVTT1

Table 135 - Output signals of the *PTOF*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO V2.2.1	Drop out	Drop out
BlkV	UV inhibit	Undervoltage inhibit active
Blk	Blocked	Blocked

Setting parameters

Table 136 - Settings of the *PTOF*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrVal	Start value	Start value	40...65 Hz	0.01 Hz	51 Hz
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	0 ms
RsDlTmms V2.2.1	Reset delay	Reset time delay	0...10000000 ms	1 ms	0 ms
BlkVal	UV inhibit value	The element is blocked for voltage below this level	0.1...1 pu	0.01 pu	0.7 pu

Characteristics

Table 137 - Characteristics of the *PTOF*

Characteristics		Values
Start value	Accuracy	±0.01 Hz (Phase-to-neutral voltage range: 40...300 V)
	Reset ratio	0.02 ± 0.01 Hz
UV inhibit value	Accuracy	±5% or ±0.5 V (secondary)
	Reset ratio	105% ± 2%
Operate delay	Accuracy	±2% or ±10 ms
Reset delay	Accuracy	±2% or ±30 ms

Table 137 - Characteristics of the *PTOF* (Continued)

Characteristics		Values
Characteristic time	Start time	< 100 ms
	Overshoot time	< 100 ms
	Disengaging time	< 100 ms

Underfrequency (*PTUF*, ANSI 81U)

Description

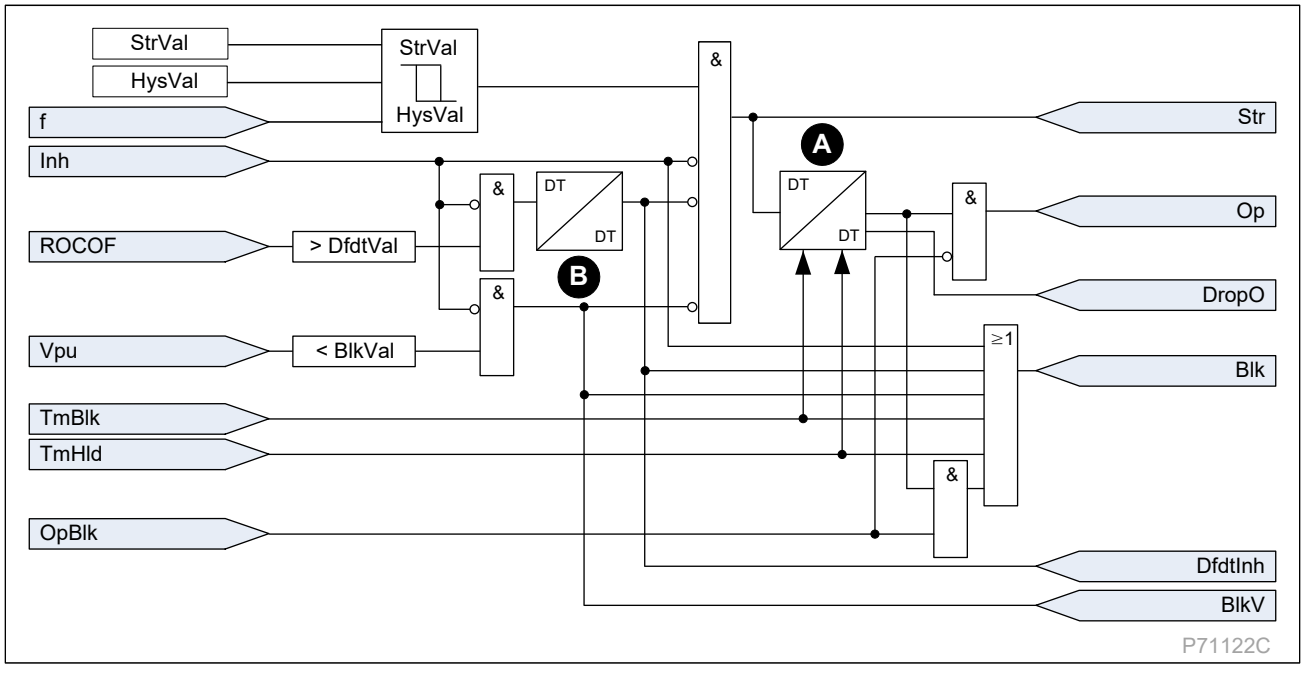
The underfrequency protection function detects the abnormally low frequency compared to the rated frequency to monitor power supply quality. The protection is used for overall tripping or load shedding.

The underfrequency protection function is generally applied where the generation capacity is less than the connected load to prevent the system frequency from decreasing below a specified threshold.

This protection is used in load shedding schemes, often in conjunction with the rate of change of frequency protection, to cover slow or fast reductions in frequency caused by the prevailing system conditions, including consideration of rotating loads. The frequency measurement is fixed to the bay VT input.

Block diagram

Figure 116 - Block diagram of the *PTUF*



A Operate delay: *OpDITmms*
Reset delay: *RsDITmms*

B Operate delay: 0 ms
Reset delay: 100 ms

Input and output signals

Table 138 - Input signals of the *PTUF*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers
OpBlk	Op block	Output blocked when active (timers not held)
Freq	Frequency	Internal signal from FTGAPC1
ROCOF	ROCOF	Internal signal from FTGAPC1
V1	V1	Internal signal from PHTVTT1

Table 139 - Output signals of the *PTUF*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO V2.2.1	Drop out	Drop out
BlkV	UV inhibit	Undervoltage inhibit active
DfdtInh	ROCOF inhibit	Rate of change of frequency inhibit active
Blk	Blocked	Blocked

Setting parameters

Table 140 - Settings of the *PTUF*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrVal	Start value	Start value	40...65 Hz	0.01 Hz	49 Hz
HysVal V2.2.1	Hysteresis value	The element will reset at this level above the start value	0.01...10 Hz	0.01 Hz	0.02 Hz
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	0 ms
RsDlTmms V2.2.1	Reset delay	Reset time delay	0...10000000 ms	1 ms	0 ms
BlkVal	UV inhibit value	The element is blocked for voltage below this level	0.1...1 pu	0.01 pu	0.7 pu
DfdtVal	ROCOF inhibit value	Rate of change of frequency above this level will inhibit element operation. Used to avoid operation during motor backfeeds to isolated buses.	0.1...20 Hz/s	0.1 Hz/s	5 Hz/s

Characteristics

Table 141 - Characteristics of the *PTUF*

Characteristics		Values
Start value	Accuracy	±0.01 Hz (Phase-to-neutral voltage range: 40...300 V)
Hysteresis value	Accuracy	± 0.01 Hz
UV inhibit value	Accuracy	±5% or ±0.5 V (secondary)
	Reset ratio	105% ± 2%
ROCOF inhibit value	Accuracy	±5% or 50 MHz/s
	Reset ratio	95%
Operate delay	Accuracy	±2% or ±10 ms
Reset delay	Accuracy	±2% or ±30 ms
Characteristic time	Start time	< 100 ms (start time without ROCOF inhibit)
	Overshoot time	< 100 ms
	Disengaging time	< 100 ms

Underfrequency load shedding (*LSPTUF*, ANSI 81LS)

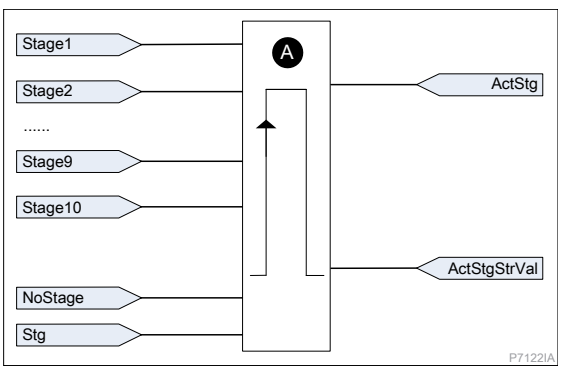
Description

The underfrequency load shedding (*UFLS*) protection function is applied to trip the load when the system frequency is dropping due to generation and load imbalance. The underfrequency setting can be adapted for up to 10 thresholds to allow feeders to be prioritized for tripping. To avoid further frequency collapse, feeders are only shed when they are not generating back into the system. A block CB closing signal is also available to ensure closing only occurs when the system frequency has recovered sufficiently.

Active stage selection

The *UFLS* protection function has up to 10 settable underfrequency thresholds. Only one threshold is active at a time.

Figure 117 - Active stage selection



A Stage activation logic

- *Stage 1* to *Stage 10* inputs are used to select the active stage. The activation is based on the rising edge. When two inputs are received simultaneously, the higher stage is selected. If the selected stage is not enabled, out of the range defined by *NumStg*, its input will be ignored, and the active stage does not change.
- *ActStg* displays the active stage and can be controlled to select the active stage. The selected stage must be in the range defined by *NumStg*, or its input will be ignored.
- *NoStage* is to deactivate all stages, but it does not disable the external input.
- *ActStgStrVal* is the start value of the activated stage.

Active power blocking

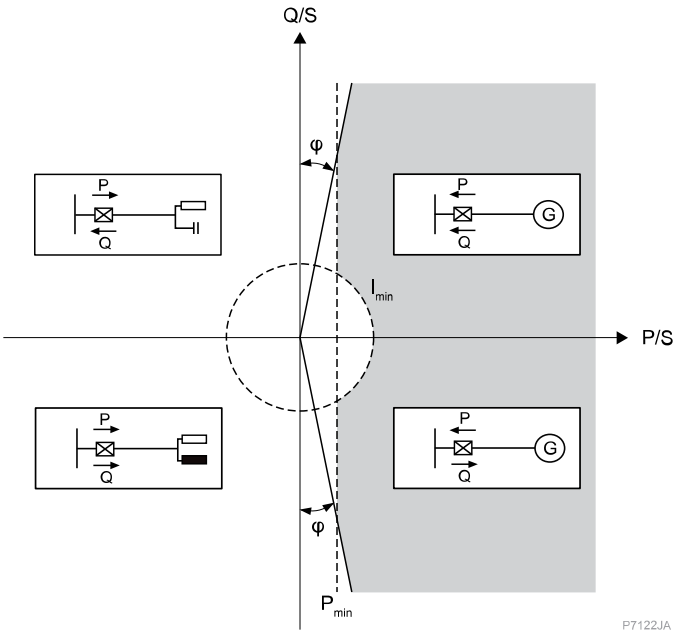
To help ensure the load is tripped and the generation is retained, the *UFLS* function includes an active power blocking element which blocks tripping when the power is flowing to the busbar.

The active power blocking is triggered when all the following three conditions are met, as shown in the figure below.

- All three-phase currents exceed the minimum current I_{min}.
- The active power exceeds the minimum power P_{min}.
- The angle between the active power and the apparent power is within the range of *90°-Sector*.

The blocking of the protection stages is indicated as the gray zone in the following figure. The minimum current I_{min} is indicated as the circle centered at the origin of the coordinates. The minimum power P_{min} is indicated as the dashed straight line. The symbol φ in the figure represents the setting value of the parameter *Sector*.

Figure 118 - Blocking of the *UFLS*



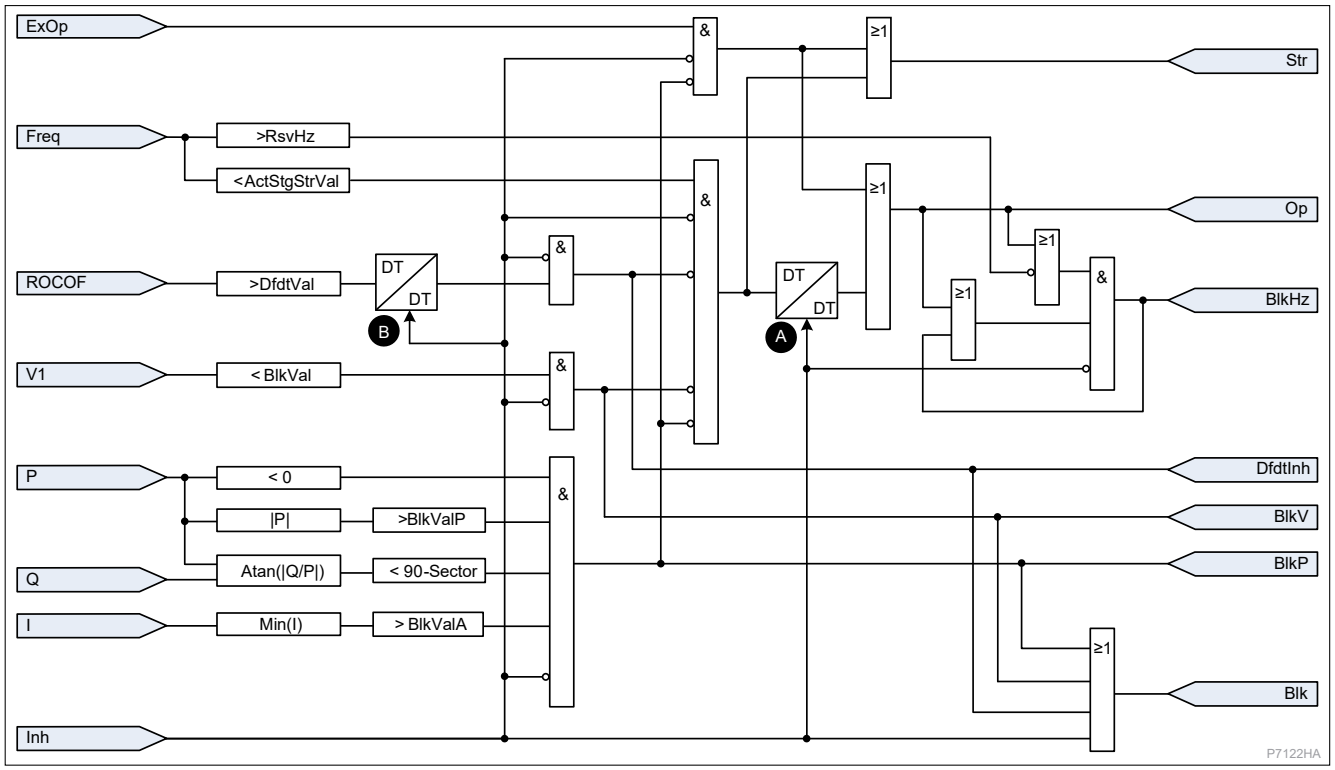
φ Sector angle

External operation

An external operation signal (*ExOp*) is available to connect the *UFLS* to other functions, such as *PTUF* and *PFRC*, to allow them to trip through a common *UFLS* element.

Block diagram

Figure 119 - Block diagram of the *LSPTUF*



A	Operate delay: *OpDITmms* Reset time: 0 ms	B	Operate delay: 0 ms Reset time: 100 ms

Input and output signals

Table 142 - Input signals of the *LSPTUF*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
Stage1	Stage 1	Activate stage 1
Stage2	Stage 2	Activate stage 2
Stage3	Stage 3	Activate stage 3
Stage4	Stage 4	Activate stage 4
Stage5	Stage 5	Activate stage 5
Stage6	Stage 6	Activate stage 6
Stage7	Stage 7	Activate stage 7
Stage8	Stage 8	Activate stage 8
Stage9	Stage 9	Activate stage 9
Stage10	Stage 10	Activate stage 10
NoStage	No stage	Disable all stages
ExOp[general]	External op	External operation with power check
Freq	Frequency	Internal signal from FTGAPC1
ROCOF	ROCOF	Internal signal from FTGAPC1
V1	V1	Internal signal from TVTT1

Table 142 - Input signals of the *LSPTUF* (Continued)

Name	Short label	Infotip
P	Power	Internal signal from PWRGAPC1
Q	Reactive power	Internal signal from PWRGAPC1

Table 143 - Output signals of the *LSPTUF*

Name	Short label	Infotip
ActStg	Active stage	Active stage
Str	Start	Start
Op	Operate	Operate
BlkHz	Block closing	This signal is set after a trip and resets when the frequency exceeds the reclose frequency
DfdtInh	ROCOF inhibit	ROCOF inhibit
BlkV	UV inhibit	UV inhibit
BlkP	Power inhibit	Power inhibit
Blk	Blocked	Blocked

Setting parameters

Table 144 - Settings of the *LSPTUF*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
NumStg	Number of stages	Number of stages	0...10	1	1
Stg1StrVal	Stage 1 start value	Stage 1 start value	40...65 Hz	0.01 Hz	49 Hz
Stg2StrVal	Stage 2 start value	Stage 2 start value	40...65 Hz	0.01 Hz	49 Hz
Stg3StrVal	Stage 3 start value	Stage 3 start value	40...65 Hz	0.01 Hz	49 Hz
Stg4StrVal	Stage 4 start value	Stage 4 start value	40...65 Hz	0.01 Hz	49 Hz
Stg5StrVal	Stage 5 start value	Stage 5 start value	40...65 Hz	0.01 Hz	49 Hz
Stg6StrVal	Stage 6 start value	Stage 6 start value	40...65 Hz	0.01 Hz	49 Hz
Stg7StrVal	Stage 7 start value	Stage 7 start value	40...65 Hz	0.01 Hz	49 Hz
Stg8StrVal	Stage 8 start value	Stage 8 start value	40...65 Hz	0.01 Hz	49 Hz
Stg9StrVal	Stage 9 start value	Stage 9 start value	40...65 Hz	0.01 Hz	49 Hz
Stg10StrVal	Stage 10 start value	Stage 10 start value	40...65 Hz	0.01 Hz	49 Hz
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	0 ms
DfdtVal	ROCOF inhibit value	ROCOF inhibit value	0.1...20 Hz/s	0.1 Hz/s	5 Hz/s
BlkVal	UV inhibit value	UV inhibit value	0.1...1 pu	0.01 pu	0.7 pu
BlkValP	Power blocking value	Power blocking value	0...0.5 pu	0.001 pu	0.05 pu
BlkValA	Current blocking value	Current blocking value	0...0.5 pu	0.001 pu	0.05 pu
Sector	Sector blocking angle	Sector blocking angle	0...30 deg	1 deg	5 deg
RsvHz	Reclose frequency	Reclose frequency	40...65 Hz	0.01 Hz	49 Hz

Characteristics

Table 145 - Characteristics of the *LSPTUF*

Characteristics		Values
Start value	Accuracy	±0.01 Hz (Phase-to-neutral voltage range: 40...300 V)
	Reset ratio (hysteresis)	0.02 Hz ± 0.01 Hz
Operate delay	DT timer accuracy	±2% or ±10 ms
Block closing	Accuracy	±0.01 Hz
ROCOF inhibit	Accuracy	±5% or 50 MHz/s
	Reset ratio (hysteresis)	0.08 Hz/s
UV inhibit	Accuracy	±5% or ±0.5 V (secondary)
	Reset ratio (hysteresis)	105% ± 2%
Power blocking value	Accuracy	±2% or ±0.001 pu (0.01...4 pu) ±10% or ±0.001 pu (0.005...0.01 pu) 0.002 pu (0.003...0.005 pu) 0.001 pu (0.001...0.003 pu)
	Reset ratio (hysteresis)	95% ± 5%
Current blocking value	Accuracy	±2% or ±0.001 pu (sinusoidal input) ±5% or ±0.002 pu (fully offset input) ±5% or ±0.005 pu (under Level 5 power frequency magnetic field)
	Reset ratio (hysteresis)	95% ± 5%
Sector blocking angle	Accuracy	±2°
	Reset ratio (hysteresis)	1°
Blocked	Block time	< 20 ms
	Reset time	< 40 ms
Characteristic time	Start time	Internal stage: < 100 ms (with an applied signal from f < +0.5 Hz to f < -0.5 Hz) External stage: 5 ms
	Overshoot time	< 100 ms

Rate of change of frequency (*PFRC*, ANSI 81R)

Description

The rate of change of frequency (ROCOF) protection function is applied to detect the immediate condition of power imbalance, and can help shed the load in a more timely manner to reduce the possibility of a widespread network collapse.

The frequency is determined by the frequency tracking function which then uses the elements measuring window to determine the ROCOF. A longer measuring window improves accuracy but also increases operate time. The *Operation mode* can be set as *Falling*, *Rising*, or *Both*, with details shown below:

- If the *Operation mode* is set as *Falling*, the function is frequency-supervised RoCoF for underfrequency. When the absolute value of RoCoF exceeds the start value and the measured frequency is below the *Frequency release value* setting, a start signal is sent. If the start signal continues for the configured operate delay, the function trips.

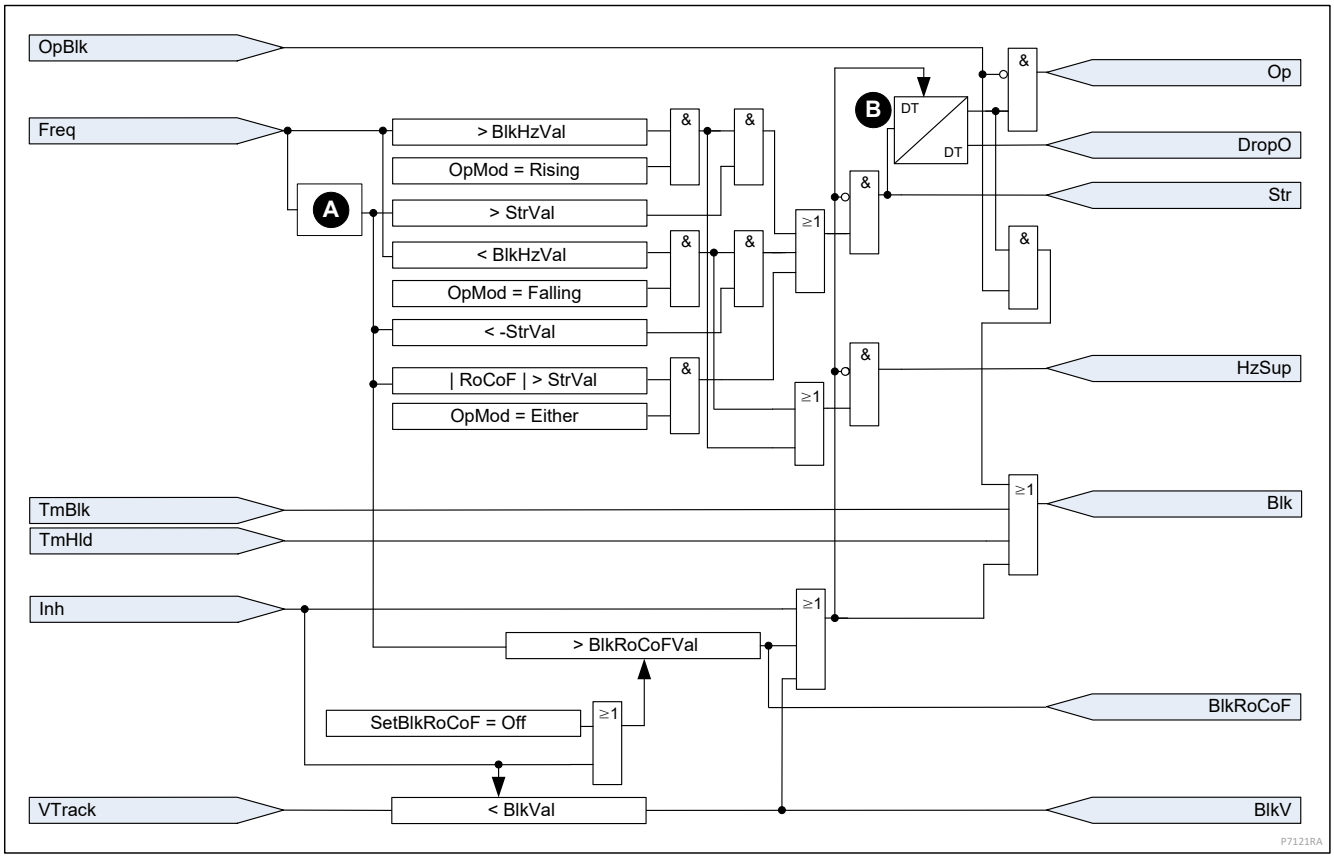
- If the *Operation mode* is set as *Rising*, the function is frequency-supervised RoCoF for overfrequency. When the absolute value of RoCoF exceeds the start value and the measured frequency is above the *Frequency release value* setting, a start signal is sent. If the start signal continues for the configured operate delay, the function trips.
- If the *Operation mode* is set as *Both*, the function is plain RoCoF for underfrequency or overfrequency. The function trips when the absolute value of RoCoF exceeds the start value for the configured operate delay.

NOTE:

- To disable frequency supervision in the falling or rising mode, set *Frequency release value* as *65 Hz* or *40 Hz*, respectively.
- The function can be inhibited by any of the following cases:
  - The frequency or RoCoF is invalid.
  - Input *Inh* is true.
  - The absolute value of RoCoF is above the *ROCOF inhibit value* setting when *High ROCOF blocking* is set to *On*.
  - The positive sequence voltage is below the *UV inhibit value* setting.

Block diagram

Figure 120 - Block diagram of the *PFRC*



A	RoCoF calculation	B	Operate delay: *OpDlTmms* Reset delay: *RsDlTmms*

Input and output signals

Table 146 - Input signals of the *PFRC*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers
OpBlk	Op block	Operate block
Freq	Frequency	Internal singal from FTGAPC1
VTrack	V1	Internal signal from PHTVTT1

Table 147 - Output signals of the *PFRC*

Name	Short label	Infotip
Str	Start	Start
HzSup	Frequency release	This is only active in rising and falling ROCOF modes. In these modes the frequency release and ROCOF start values need to be exceeded for starting
Op	Operate	Operate
DropO	Drop out	Drop out
BlkV	UV inhibit	UV inhibit
BlkRoCoF	ROCOF inhibit	Rate of change of frequency inhibit active
Blk	Blocked	Blocked
RoCoF	ROCOF	Rate of change of frequency

Setting parameters

Table 148 - Settings of the *PFRC*

Name	Short label	Infotip	Setting Range	Step Size	Default Setting
SetMod	Function status	Function status	• On • Off		Off
ClcIntvPer	Measuring window	Measurement period used for ROCOF. Set above low frequency oscillation periods.	50...1000 ms	5 ms	50 ms
StrVal	Start value	This is the ROCOF start value. If the operation mode is both the element will start if this value is exceeded. If the operation mode is rising or falling it will start if this value is exceeded and the frequency value above the frequency release value for rising or below the frequency release value for falling	0.1...10 Hz/s	0.1 Hz/s	1 Hz/s
OpMod	Operation mode	Operation mode	• Rising • Falling • Both		Falling
BlkHzVal	Frequency release value	When operation mode is rising the frequency must also be above this value for operation. When operation mode is falling the frequency must also be below this value.	40...65 Hz	0.01 Hz	50 Hz
OpDlTmms	Operate delay	Operate time delay	0...100000 ms	1 ms	500 ms
RsDlTmms	Reset delay	Reset time delay	0...100000 ms	1 ms	0 ms

Table 148 - Settings of the *PFRC* (Continued)

Name	Short label	Infotip	Setting Range	Step Size	Default Setting
BlkVal	UV inhibit value	Voltage below this level will inhibit element operation	0.1...1 pu	0.01 pu	0.7 pu
SetBlkRoCoF	High ROCOF blocking	The element is blocked for Rate Of Change Of Frequency (ROCOF) above this level	• Off • On		On
BlkRoCoFVal	ROCOF inhibit value	Rate of change of frequency above this level will inhibit element operation. Used to avoid operation during motor backfeeds to isolated buses.	0.1...20 Hz/s	0.1 Hz/s	5 Hz/s

Characteristics

Table 149 - Characteristics of the *PFRC*

Characteristics		Values
Start value	Accuracy (frequency)	±10 MHz (Phase-to-neutral voltage range: 40...300 V)
	Accuracy (RoCoF)	±50 MHz/s (when measuring window is 50 ms)
	Frequency reset ratio (hysteresis)	20 MHz
	RoCoF reset ratio (hysteresis)	80 MHz/s
Operate delay	Accuracy	±2% or ±10 ms
Reset delay	Accuracy	±2% or ±30ms
Characteristic time	Start time (frequency)	< 100 ms (when the frequency change is within *BlkHzVal* ± 0.5 Hz)
	Start time (RoCoF)	< 150 ms (when the RoCoF change is within *StrVal* ± 0.5 Hz/s)
	Reset delay	< 150 ms (reset to nominal frequency)
	Disengaging time	< 120 ms
Blocked	Block time (*Blk* & *BlkV*)	< 20 ms
	Reset delay (*Blk* & *BlkV*)	< 40 ms
	Block time (*BlkRoCoF*)	< 100 ms
	Reset delay (*BlkRoCoF*)	< 150 ms

High impedance differential (*HIZPDIF*, ANSI 87/64REF)

Description

For high impedance differential protection, CTs are placed at the ends of the differential zone and paralleled. A resistor is placed in series with the PowerLogic P7 CT input to stabilize the protection for CT saturation during through fault conditions.

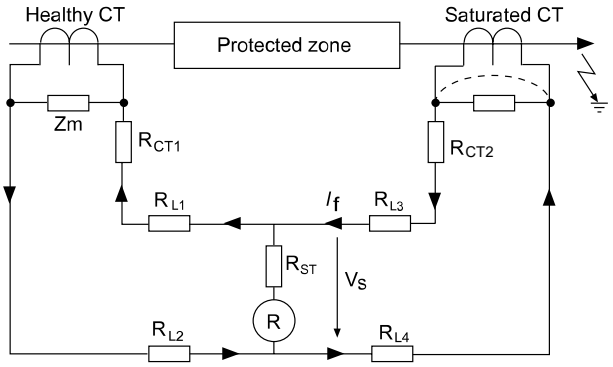
For high impedance applications, the *Measurement mode* should be set to *Peak to peak*. For core balance applications, the *Measurement mode* should be set to *FFT*.

Peak to peak can be calculated as follows:

Peak to peak = ABS(max(48 Samples in latest cycle) - min(48 Samples in latest cycle)) / (2 × *SQRT*(2))

High impedance differential protection requires all CTs to be the same ratio. The high impedance principle is best explained by considering a differential scheme where one CT is saturated for an external fault, as shown in the diagram below.

Figure 121 - Principle of high impedance differential protection



Voltage across device circuit:

$$V_s = I_f \times (R_{CT} + 2R_L)$$ E71121A

Stabilizing resistor, R_{ST}, limits spill current to setting I_S:

$$R_{ST} = \frac{V_S}{I_S} - R_R$$ E71122A

Where:

I_f = Maximum secondary through fault current

R_R = Device burden

R_L = Resistance of a single lead from the device to the current transformer

R_{CT} = Current transformer secondary winding resistance

- For an internal fault, the current feeding into the device is $I_{CT1} + I_{CT2}$
- For an external fault with no CT saturation, the current feeding into the device is $I_{CT1} - I_{CT2} = 0$
- For an external fault with one CT saturated, e.g. CT2, the secondary current produced by the CT1 will flow through CT2.

  If the magnetizing impedance of CT2 is negligible, the maximum voltage across the device circuit will be equal to the secondary fault current multiplied by the connected impedance, ($R_{L3} + R_{L4} + R_{CT2}$)

For the device to achieve stability at the maximum applied voltage, it is necessary to elevate the overall impedance of the device circuit. This adjustment helps ensure that the current passing through the device remains below the current setting (**I_S**), preventing maloperation.

As the impedance of the device input alone is relatively low, a series of connected external resistors is required. An additional non-linear resistor, Metrosil, may be required to limit the peak secondary circuit voltage during internal fault conditions.

Examples of the device connections for high impedance protection are shown below. Phase mode can be applied to any system with three phase CTs at all ends of the differential zone with no transformers within the zone.

Examples include bus, machine and reactor differential. Ground mode is used for restricted ground fault applications and only detects ground faults within the protected zone.

Examples include transformer winding and machine ground fault detection.

Figure 122 - Example of high impedance protection connections with phase mode

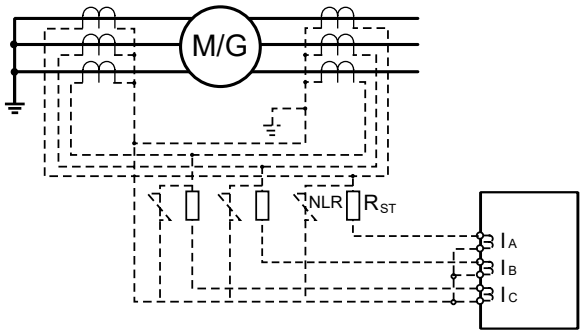
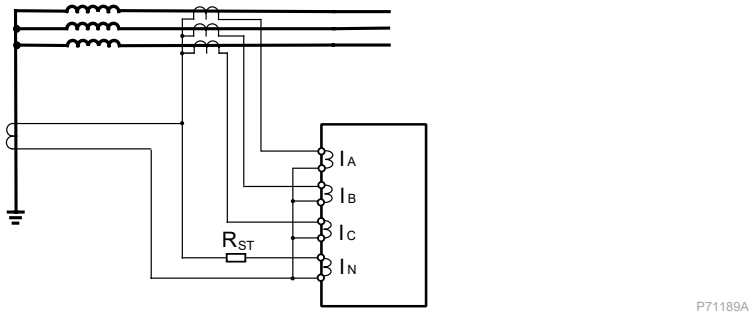


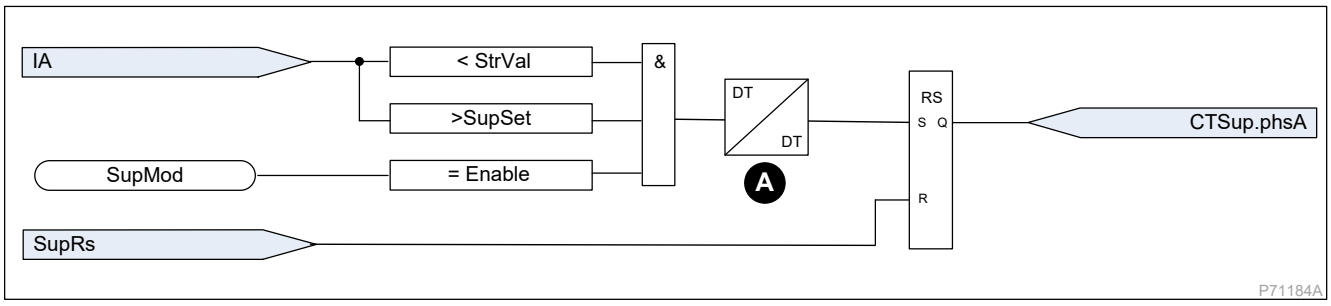
Figure 123 - Example of high impedance protection connections with ground mode



Block diagram

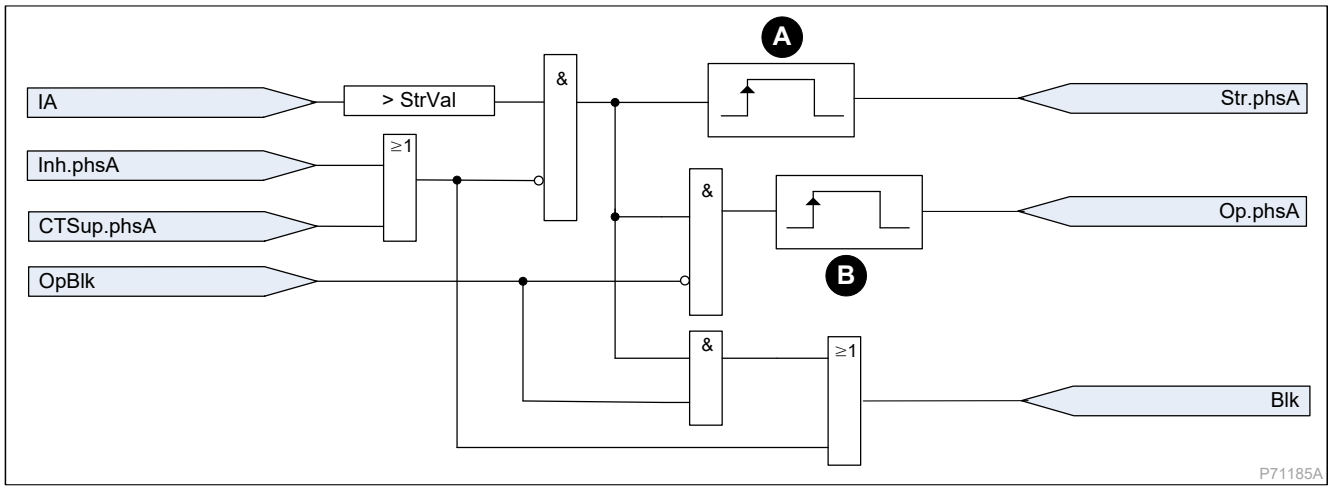
In the *Phase* mode, the high impedance differential protection is phase segregated and CT supervision is checked if necessary.

Figure 124 - Block diagram of CT supervision logic (phase A)



A *CT supervision operate delay*: *SupDITmms*
Reset delay: 0 s

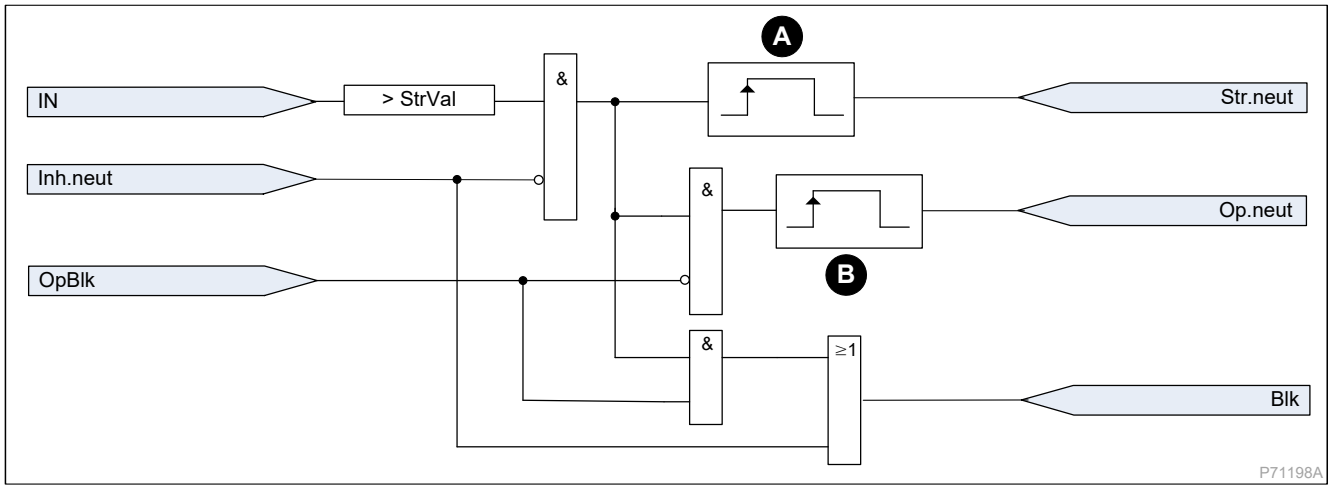
Figure 125 - Block diagram of high impedance differential (phase A)



A	Dwell time: 40 ms	B	Dwell time: 40 ms

In the ground mode, the neutral current is monitored.

Figure 126 - Block diagram of high impedance differential (IN)



A	Dwell time: 40 ms	B	Dwell time: 40 ms

Input and output signals

Table 150 - Input signals of the *HIZPDIF*

Name	Short label	Infotip
IAIBIC	Phase current	Phase current
Ineut	Neutral current	Neutral current
Inh[general;phsA;phsB;phsC;neut]	Inhibit	Inhibit function
OpBlk	Op block	Output blocked when active (timers not held)
SupRs	Reset CTS	CT supervision reset

Table 151 - Output signals of the *HIZPDIF*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
CTSup	CT supervision	CT supervision
SupRsCtrl	Reset CT supervision	Reset CT supervision
Blk	Blocked	Blocked

Setting parameters

Table 152 - Settings of the *HIZPDIF*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
MeasType	Measurement mode	Peak to peak is normally used in high impedance applications. The element can be used without external resistor as an instantaneous overcurrent where Fast Fourier Transform (FFT) or Peak to peak can be used	• FFT • Peak to peak		Peak to peak
OpMod	Operation mode	Select between phase high impedance and ground high impedance (REF)	• Phase • Ground		Phase
StrVal	Start value	Operate value. Usually set above load if possible	0.01...2 pu	0.01 pu	1 pu
SupMod	CT supervision mode	CT supervision will block operation when a CT fault is detected. Can only be used if the element is set above load	• Off • On		Off
SupSet	CT supervision start value	If this current is seen in any phase for more than the operate time then CT supervision will operate	0.005...2 pu	0.001 pu	0.1 pu
SupDlTmms	CT supervision operate delay	Set above the maximum fault time	100...10000 ms	100 ms	3000 ms

Characteristics

Table 153 - Characteristics of the *HIZPDIF*

Characteristics		Values
Start value	Accuracy	±2% or ±0.001 pu (sinusoidal input) ±5% or ±0.002 pu (fully offset input)
	Reset ratio	95% ± 5%
CT supervision operate delay	Accuracy	±2% or ±10 ms
Operate delay	Accuracy	2% or ±10 ms
Characteristic time	Start time	< 20 ms (2 Is) < 20 ms (Saturated CT)

Biased differential (*PHPDIF*, ANSI 87)

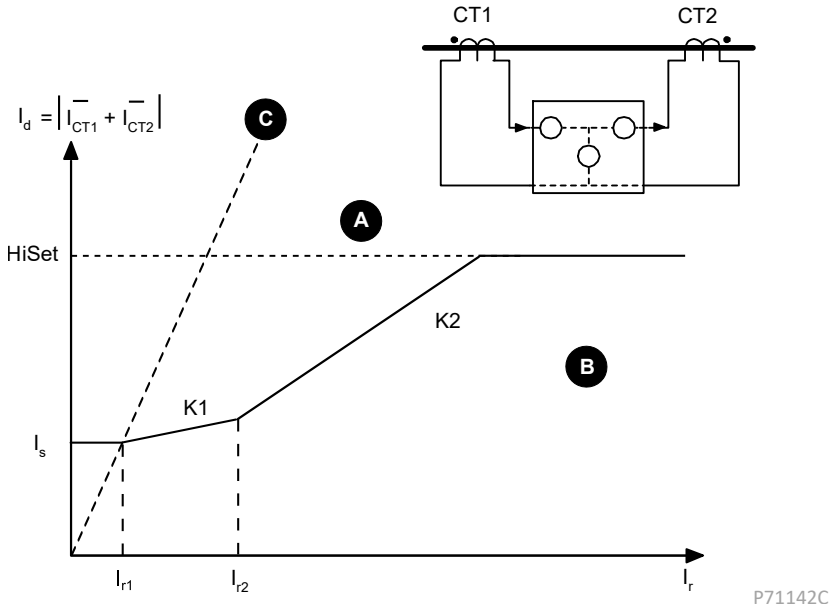
Description

The biased differential protection calculates the difference between the currents entering and leaving a protected zone. The protection operates when this difference exceeds the threshold.

Differential currents may also be generated due to CT saturation. To provide stability during saturation, the PowerLogic P7 adopts a biasing technique. This method effectively raises the setting of the device in proportion to the value of saturation to help prevent relay maloperation. The figure below shows the operating characteristics of the biased differential protection.

A three-slope biased differential protection operating characteristic is applied. The lower slope K1 provides stability for small CT mismatches, whilst ensuring good sensitivity to resistive faults under heavy load conditions. The higher slope K2 is used to improve device stability under heavy through fault conditions where CT saturation may occur.

Figure 127 - Biased differential protection operating characteristic



I_d	Differential current	I_r	Restraint current
I_s	*Start value*: Minimum differential current setting	I_{r1}	0.5 *Start value*
I_{r2}	*Slope 2 start value*: Restraint current threshold setting, above which the slope K2 is used.	K1 K2	Slope settings: *Slope 1* *Slope 2*
A	Operating area	B	Restraining area
C	Max fault		

Differential and bias currents calculation

The calculation of differential, general bias and saturation bias currents is performed on a per phase basis.

Differential current calculation (I_d)

The differential current is the vector sum of the phase currents measured at CT1 and CT2.

$$Id = |\vec{I}_{CT1} + \vec{I}_{CT2}|$$ E71101A

General bias current calculation (I_{bias})

The bias current is the average of the phase currents measured at CT1 and CT2.

$$I_{bias} = \frac{|\vec{I}_{CT1}| + |\vec{I}_{CT2}|}{2}$$ E71102A

Restraint current calculation (I_r)

The biased differential protection takes the maximum bias current from all three phases for the operating characteristic (I_r = max($I_{bias}A$, $I_{bias}B$, $I_{bias}C$)).

Saturation bias current calculation (I_{sat})

CT Saturation is very likely to occur during faults or for load currents with a DC offset such as transformer inrush. To avoid differential operation during severe saturation the device applies a saturation bias to temporarily increase the differential trip level when saturation is detected.

The device monitors the change in bias compared to the previous two cycles on per phase basis. A drop in bias can be due to load change, fault clearance or CT saturation. For CT saturation during external faults there will be a corresponding increase in differential current. For load changes, fault clearance or saturation during internal faults, there will be a reduction of differential current or no differential current.

The saturation bias is calculated on a per phase basis as three times the bias drop over the last 40 ms. This value is limited to the differential measurement.

The saturation bias is added to the trip level to stabilize the element when CT saturation occurs.

The CT saturation is due to DC components on the power system and it will come out of saturation depending upon the primary time constant. The saturation bias will decrement according to the *Saturation time constant* setting which can normally be left at the maximum setting.

The saturation bias is set to zero if the protection has started, *Saturation time constant* is zero or when the bias current is less than 0.5 *LoSet*.

Detailed saturation bias is calculated as follows:

$I_{sat}(n)$ = max[min(3 × (max($I_{bias}(n-1)$, $I_{bias}(n-2)$,...$I_{bias}(n-8)$) - $I_{bias}(n)$), $I_d(n)$), $I_{sat}(n-1)$ × (1 - 5/*SatTC*)]

- If biased differential protection starts, $I_{sat}(n)$ = 0;
- If setting *Saturation time constant* = 0, $I_{sat}(n)$ = 0;
- If $I_{bias}(n)$ < 0.5 *LoSet*, $I_{sat}(n)$ = 0.

Where:

$I_{bias}(n-x)$: bias current calculated at x execution cycles (5...40 ms) before.

$I_{bias}(n)$: bias current calculated at current execution cycle.

$I_d(n)$: differential current calculated at current execution cycle.

$I_{sat}(n-1)$: saturation bias current calculated at 1 execution cycle (5 ms) before.

Phase comparison

The phase comparison is to indicate if the fault is internal or external. It is implemented in K2 slope ($I_r > I_{r2}$).

- When $I_r > I_{r2}$, and one of the following five conditions happens, it will be treated as an internal fault and $I_{Satbias}$ will be set to *0*.
  1. ($I_1 < 0.05$) OR ($I_2 < 0.05$)
  2. [max(I_1(n),...,I_1(n-5)) < 0.05] OR [max(I_2(n),...,I_2(n-5)) < 0.05]
  3. [max(I_1(n),...,I_1(n-5)) < I_2 × 0.05] OR [max(I_2(n),...,I_2(n-5)) < I_1 × 0.05]
  4. [AND (min(I_1(n), ..., I_1(n-8)) < 0.5, | I_1(n) - I_1(n-8) | < 0.05)] OR [AND (min(I_2(n),...,I_2(n-8)) < 0.5, | I_2(n) - I_2(n-8) | < 0.05)]
  5. [($I_1 > I_{r2}$ × 0.25) OR ($I_2 > I_{r1}$ × 0.25)] AND [| Angle(I_1) - Angle(I_2) | < 50°]

     NOTE: The first four conditions are to predict internal fault in single end fed system. The last condition is to predict internal fault in double end fed system.
- When the angle between I_1 and I_2 is within [90°, 180°], also the five conditions are not achieved, it will be treated as external fault and I_{sat} will be set as I_d.
- Otherwise, I_{sat} will be set as the result derived from the equation:

  $I_{sat}(n)$ = max[min(3 × (max($I_{bias}(n-1)$, $I_{bias}(n-2)$,...$I_{bias}(n-8)$) - $I_{bias}(n)$), $I_d(n)$), $I_{sat}(n-1)$ × (1 - 5/*SatTC*)],
  which is described in Differential and bias currents calculation, page 249.

CT ratio scaling

It is recommended that CT1 and CT2 have the same ratio, but different ratios of up to 10 times are allowed. If the ratio of Primary nominal currents of CT2 and CT1 is outside 0.1 to 10, the biased protection is blocked.

The differential and bias current values for each measurement system are calculated from the current values after CT ratio matching. CT1 is used as the reference and the currents of CT2 are scaled to CT1.

$$I_d = \left| \vec{I}_{CT1} + \vec{I}_{CT2} \times \frac{CT2Prim}{CT1Prim} \right|$$

E71103A

$$I_{bias} = \frac{\left|\vec{I}_{CT1}\right| + \left| \vec{I}_{CT2} \times \frac{CT2Prim}{CT1Prim} \right|}{2}$$

E71105A

Split phase mode

If the generator stator windings are wound with two identical three-phase windings connected in parallel, and the windings are brought out separately, biased differential element can be set to *Split Phase Mode* to provide additional inter-turn protection.

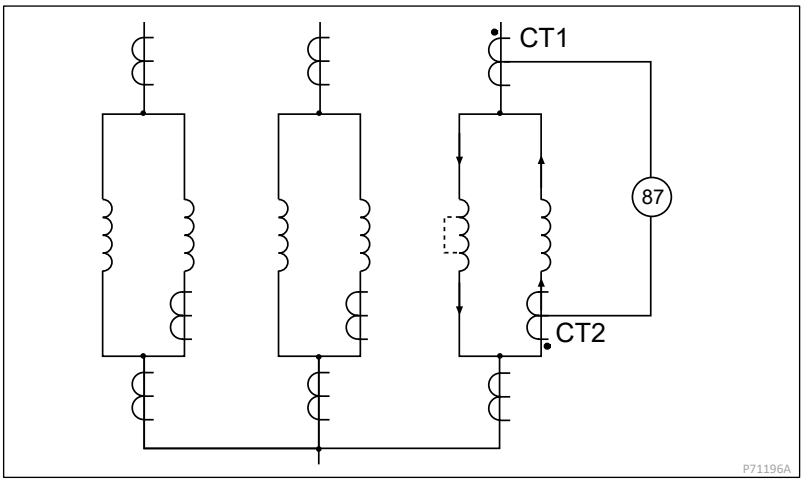
$$I_d = \left| \vec{I}_{CT1} + 2 \times \vec{I}_{CT2} \times \frac{CT2Prim}{CT1Prim} \right|$$

E71104A

$$I_{bias} = \frac{\left|\vec{I}_{CT1}\right| + \left| 2 \times \vec{I}_{CT2} \times \frac{CT2Prim}{CT1Prim} \right|}{2}$$

E71106A

Figure 128 - Split phase mode for generator differential protection



Tripping criteria

The differential current (I_d) threshold changes according to the value of restraint current (I_r) as shown in the operating characteristic.

The saturation bias current (I_{sat}) is on a per phase basis and is not affected by the K1 or K2 setting.

The operating threshold of per phase is formulated as follows:

- $0 < I_r \leq 0.5$ Is

  I_d threshold = Is
- Slope K1: 0.5 Is $< I_r \leq I_{r2}$

  I_d threshold = Is + (I_r - 0.5 × Is) × K1 + I_{sat}
- Slope K2: $I_r > I_{r2}$

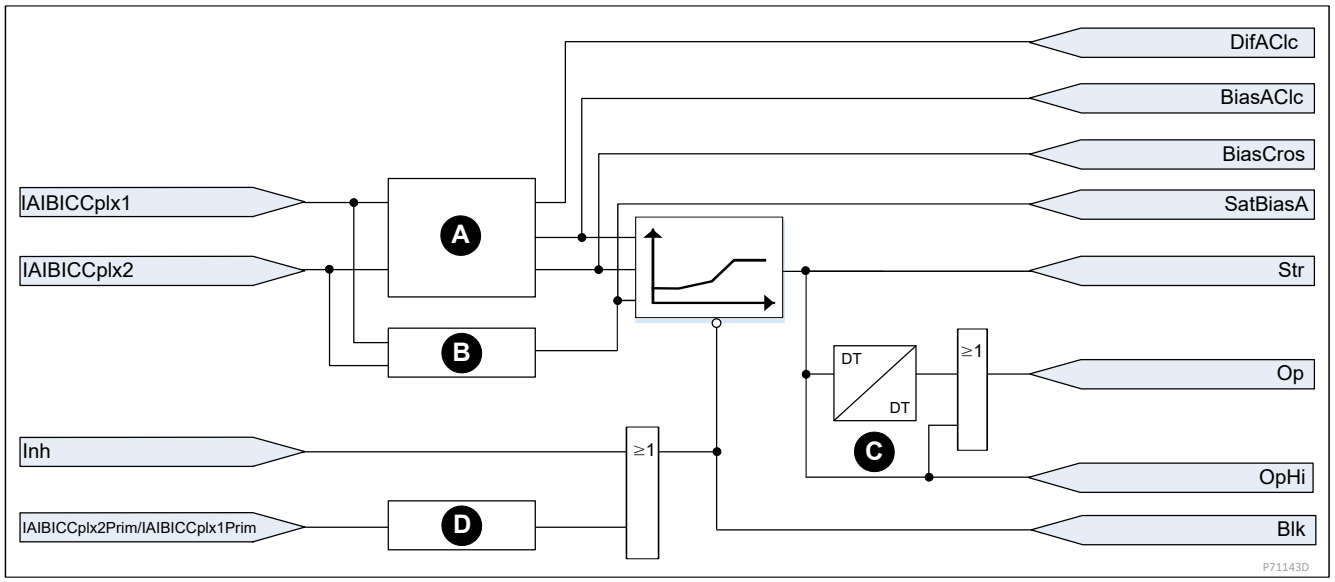
  I_d threshold = Is + (I_{r2} - 0.5 × Is) × K1 + (Ir - I_{r2}) × K2 + I_{sat}

The start signal of the biased differential protection is active when the following conditions are simultaneously present:

- No inhibit input.
- Ratio of CT2 and CT1 primary nominal currents within *0.1...10*.
- The differential current is more than I_d threshold for four consecutive measurements near the threshold or
  two consecutive measurements above 1.1 I_d threshold.

An operate signal is issued once the operate delay has elapsed. The operate signal will be reset when differential current drops down under 95% of the threshold.

Figure 129 - Block diagram of the *PHPDIF*



A	Differential and restraint currents calculation	B	Saturation bias current calculation
C	Operate delay: *OpDITmms* Reset delay: 0 ms	D	Ratio of CT2 and CT1 primary nominal currents outside *0.1...10*

Input and output signals

Table 154 - Input signals of the *PHPDIF*

Name	Short label	Infotip
IAIBICCplx1	Reference current	Reference current
IAIBICCplx2	Second current	Second current
Inh[general; phsA;phsB; phsC]	Inhibit	Inhibit function

Table 155 - Output signals of the *PHPDIF*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
OpHi	High set operate	High set operate
Blk	Blocked	Blocked
DifAClc	Diff	Diff
BiasAClc	Bias	Bias
BiasCros	Cross bias	Cross bias
SatBiasA	Saturation bias	Saturation bias

Setting parameters

Table 156 - Settings of the *PHPDIF*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
LoSet	Start value	Pickup or low set value	0.01...3 pu	0.01 pu	0.2 pu
DifSlp1	Slope 1	Lower slope for mismatch	0...2	0.01	0.3
Slp2Set	Slope 2 start value	Upper slope value normally set above load	1...10 pu	0.01 pu	1.5 pu
DifSlp2	Slope 2	Upper slope for CT saturation	0.1...2	0.01	1.5
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	0 ms
HiSet	High set op value	Instantaneous high set operate value. Normally set above maximum through fault level	0...100 pu	0.01 pu	0 pu
SPhMod	Split phase mode	Used on double wound generators to provide differential and interturn	• Off • On		Off
SatTC	Saturation time constant	Set above the system time constant. Can normally be left at maximum	0...1000	1	1000

Characteristics

Table 157 - Characteristics of the *PHPDIF*

Characteristics		Values
Start value	Accuracy	±5% or ±0.001 pu
	Reset ratio	95% ± 5%
Operate delay	Accuracy	±2% or ±10 ms
Blocked	Block time	< 20 ms
	Reset time	20...40 ms
Characteristic time	Start time	< 50 ms at 1.1 Is < 30 ms at 1.2 Is < 20 ms (single and double end fed with and without offset on slope 2 with > 2 Is)
	Start reset time	< 30 ms
	Disengaging time	< 30 ms at 0 Is

Restricted ground fault (*RGFPDIF*, ANSI 64REF)

Description

The restricted ground fault protection function is used for resistance grounded transformers where the backup ground fault time is usually too long to prevent excessive transformer damage and inadequate coverage provided by differential.

The *RGFPDIF* can also be applied to

- autotransformers to provide a differential unaffected by transformer ratio.
- grounded star windings to provide a more sensitive ground fault detection than that available from differential.

NOTE: The element applies low impedance restricted ground fault, high impedance restricted ground fault is also available in the high impedance (*HIZPDIF*) element.

Low impedance *RGFPDIF*

Each individual CT is usually considered for biasing and saturation detection. As each winding is considered independently, there is no ratio/phase correction, but all CTs must be matched to a common reference which is the primary CT.

The low impedance *RGFPDIF* uses a two-slope biased characteristic.

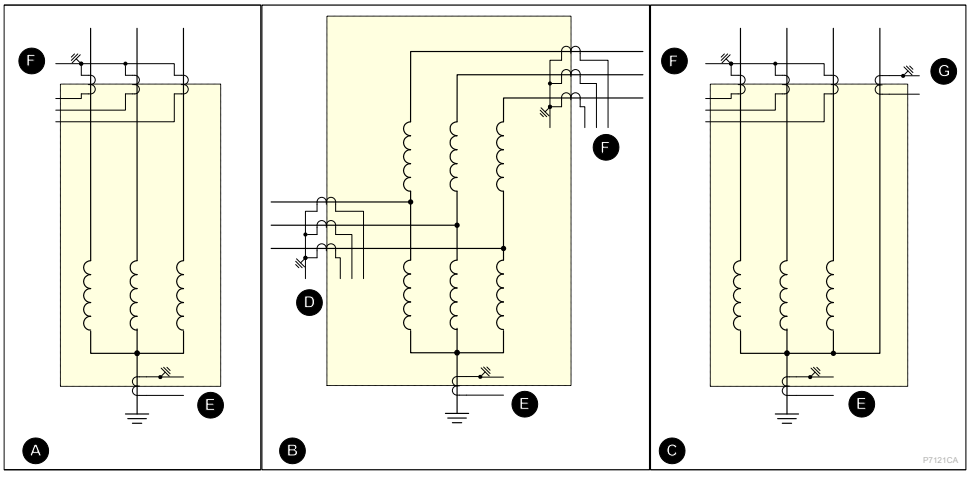
- The low impedance *RGFPDIF* compares the vector sum of the restricted ground fault protection function of the transformer winding to the neutral point current. The differential and bias currents are calculated from the current variables after scaling.

The limitation is for high resistance grounded systems where the pickup relative to the CT nominal is very low and the phase CT ankle point can cause maloperations.

- The minimum pickup range relative to the primary CT should be 5% to 200%.
- Primary ratio matching factors should be:
  - Neutral CT/Reference CT: 0.05 to 2.
  - Second CT/Reference CT: 0.05 to 1.
  - Load neutral CT/Reference CT: 0.5 to 1.
- The low impedance *RGFPDIF* compares the vector sum of the restricted ground fault protection function of the transformer winding to the neutral point current. The differential and bias currents are calculated from the current variables after scaling.

Typical applications

Figure 130 - Typical applications diagram



A	Star mode	B	Auto-transformer
C	4-wire mode	D	Phase currents (Second)
E	Starpoint current	F	Phase currents (Reference)
G	neutral wire current		

Differential and bias current calculation

- When operation mode is star mode,
  - *DifACIc* = *RefIA* + *RefIB* + *RefIC* + *INeut*
  - *BiaACIc* = Max(*RefIA*, *RefIB*, *RefIC*)
- When operation mode is Auto-transformer mode,
  - *DifACIc* = *RefIA* + *RefIB* + *RefIC* + *SndIA* + *SndIB* + *SndIC* + *INeut*
  - *BiaACIc* = Max(*RefIA*, *RefIB*, *RefIC*, *SndIA*, *SndIB*, *SndIC*)
- When operation mode is 4-wire mode,
  - *DifACIc* = *RefIA* + *RefIB* + *RefIC* + *INeut* + *ILoad*
  - *BiaACIc* = Max(*RefIA*, *RefIB*, *RefIC*, *ILoad*)

Scaling factor

The differential and bias current values for each measurement system are calculated from the current values after CT primary matching. The scaling factors are listed as follows:

- Neutral CT primary/Reference CT primary
- Second CT primary/Reference CT primary
- Load CT primary/Reference CT primary

Tripping Characteristic

The tripping characteristic of the low impedance *RGFPDIF* has one knee, which is when I_{bias} = 1 pu

The lower slope provides sensitivity for internal faults. The higher slope provides stability under through fault conditions, since transient differential currents may be present due to current transformer saturation.

Once the differential and bias currents are calculated, the following comparisons are made and an operate/restrained signal is obtained:

Flat slope:

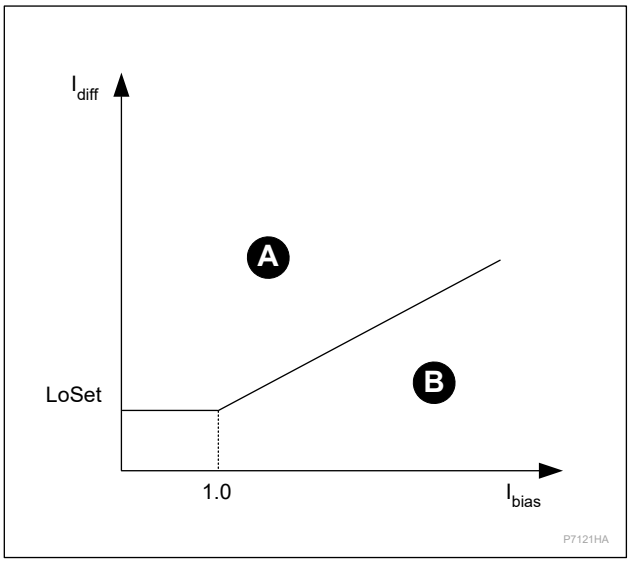
- $I_{bias} \leq 1$
- $I_{diff} \geq$ Loset

A slope:

- $I_{bias} > 1$
- $I_{diff} \geq$ Loset + (I_{bias} - 1) × 0.5

Low impedance *RGFPDIF* characteristic, page 257 shows the operating characteristic.

Figure 131 - Low impedance *RGFPDIF* characteristic



A	Operate	B	Restrain

Phase comparator

Phase A phase comparator is used to distinguish internal fault and external fault. If the phase difference between *INeut* and I_{sum} is within [-90°, 90°], it is an internal fault, otherwise it is an external fault.

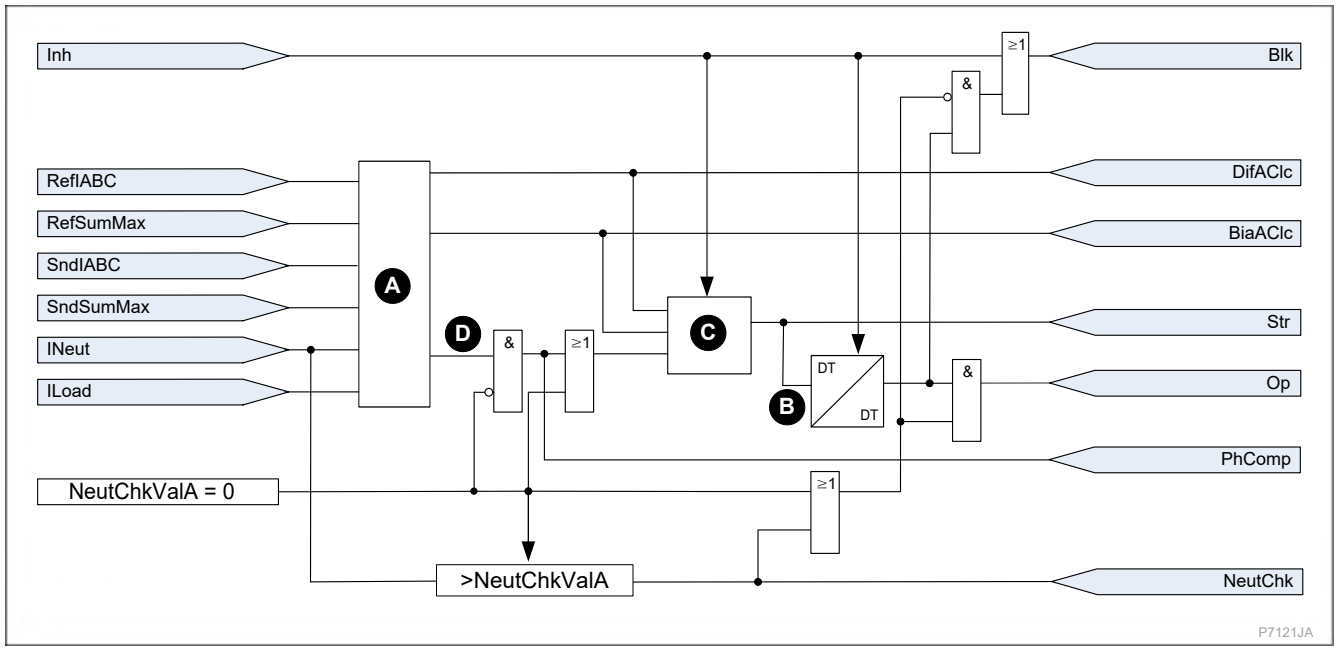
When ***NeutChkValA*** is set as *0*, ***PhComp*** is *False*. Otherwise, ***PhComp*** is *True* when any of the situations in each mode satisfies:

- When operation mode is star mode,
  - (*INeut* > *NeutChkValA*) and (sum(*RefIA*, *RefIB*, *RefIC*) < *NeutChkValA* and lasts for greater than 10 ms)
  - (*INeut* > *NeutChkValA*) and (sum(*RefIA*, *RefIB*, *RefIC*) > *NeutChkValA*) and (| *INeutang* - sum(*RefIA*, *RefIB*, *RefIC*)ang | < 90°)
- When operation mode is Auto-transformer mode,
  - (*INeut* > *NeutChkValA*) and (sum(*RefIA*, *RefIB*, *RefIC*, *SndIA*, *SndIB*, *SndIC*) < *NeutChkValA* and lasts for greater than 10 ms)
  - (*INeut* > *NeutChkValA*) and (sum(*RefIA*, *RefIB*, *RefIC*, *SndIA*, *SndIB*, *SndIC*) > *NeutChkValA*) and (| *INeutang* - sum(*RefIA*, *RefIB*, *RefIC*, *SndIA*, *SndIB*, *SndIC*)ang | < 90°)
- When operation mode is 4-wire mode,
  - (*INeut* > *NeutChkValA*) and (sum(*RefIA*, *RefIB*, *RefIC*, *ILoad*) < *NeutChkValA* and lasts for greater than 10 ms)
  - (*INeut* > *NeutChkValA*) and (sum(*RefIA*, *RefIB*, *RefIC*, *ILoad*) > *NeutChkValA*) and (| *INeutang* - sum(*RefIA*, *RefIB*, *RefIC*, *ILoad*)ang | < 90°)

  NOTE: The hysteresis of angle is 5°. 10 ms delay is for **Phase comparator** stability when the fault disappears.

Block diagram

Figure 132 - Block diagram of the *RGFPDIF*



A	Differential and bias current calculation	B	Operate delay: *OpDITmms*
C	Tripping characteristic	D	Phase comparator

Input and output signals

Table 158 - Input signals of the *RGFPDIF*

Name	Short label	Infotip
RefIABC	Reference current	Reference current
SndIABC	Second current	Second current
INeut	IN	Neutral current
ILoad	Load IN	Load neutral current
Inh[general; neut]	Inhibit	Inhibit function

Table 159 - Output signals of the *RGFPDIF*

Name	Short label	Infotip
NeutChk	Neutral check	Neutral check
PhComp	Phase comparator check	Phase comparator check
Str	Start	Start
Op	Operate	Operate
Blk	Blocked	Blocked
DifClcA	Diff	Differential current
BiasClcA	Bias	Bias current

NOTE: Second current is used in Auto mode and it should not use the same CT as reference current. Load neutral current is used in 4-wire mode and it should not use the same CT as neutral current.

Setting parameters

Table 160 - Settings of the *RGFPDIF*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
OpMod	Operation mode	Selects the type of winding to be protected	• Star • Auto • 4 wire		Star
LoSet	Start value	Start value	0.001...3 pu	0.001 pu	0.2 pu
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	0 ms
NeutChkValA	IN check value	The neutral current must exceed this value for operation. Phase comparison applied when the line current also exceeds this value	0...3 pu	0.001 pu	0.2 pu

Characteristics

Table 161 - Characteristics of the *RGFPDIF*

Characteristics		Values
Start value	Accuracy	±2% or ±0.001 pu
	Reset ratio	95% ± 5%
Operate delay	DT accuracy	2% or ±10 ms
	Reset time	< 30 ms (0 Is)
Neutral check	Accuracy	±2% or ±0.001 pu
	Reset ratio	95% ± 5%
	Start time @nomHz	< 30 ms (2 I_{trip} sinusoid)
	Start reset time	< 25 ms (0 I_{trip})
Blocked	Block time	< 20 ms
	Start reset time	< 40 ms
Characteristic time	Start time @nomHz	< 40 ms (2 I_{trip} sinusoid)
	Start reset time	< 30 ms (0 I_{trip})

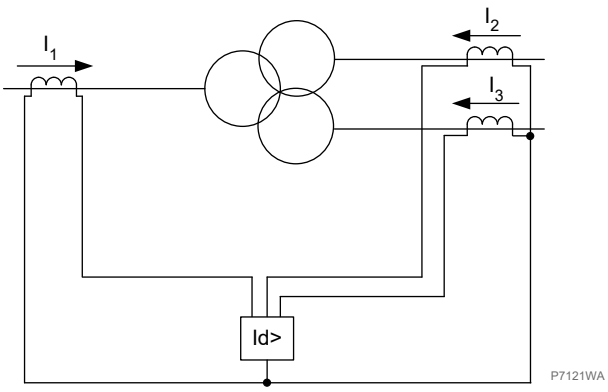
Transformer differential (*TR2PDIF* and *TR3PDIF*, ANSI 87T)

Description

The transformer differential function is used for all transformers above 1 MVA to help protect the transformer against internal faults. Most transformers have 2 windings, but 3 windings are often used for applications such as rectifiers above 20 MVA.

Principle of transformer differential, page 260 illustrates the principle of the transformer differential. Current transformers on the primary side and secondary side are summated after compensating for the vector group, transformer and CT ratios.

Figure 133 - Principle of transformer differential



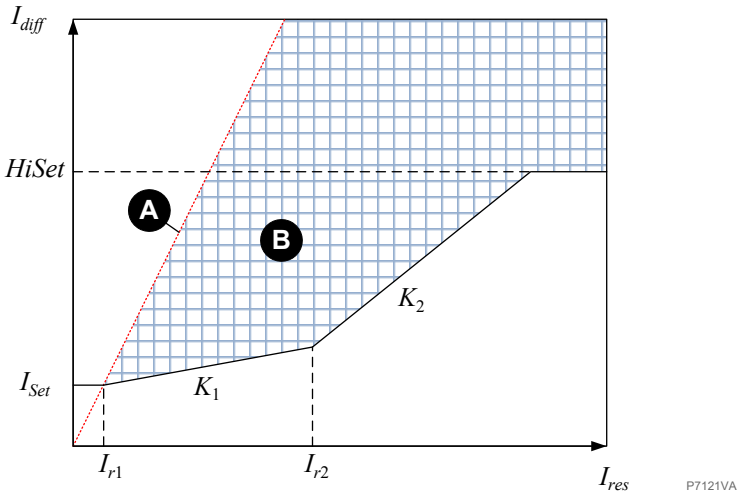
Based on the primary current values adjusted for the winding voltage and phase, currents are compared across all ends continuously. In normal operation conditions or during external faults without CT saturation, the primary current at all ends remain almost the same, so the comparison result is practically zero. However, when faults occur within the protected transformer, the comparison result is higher than the operational value, and as a result, the protection system will trip. The protection zone is determined by the location of current transformers around the transformer.

Bias is applied in the function to help ensure stability during external faults while still allowing sensitive settings to pick up internal faults. This is facilitated by a 3-slope bias differential element.

- When operation mode is 3 windings
  - For differential current: $I_{diff} = |\acute{I}_1 + \acute{I}_2 + \acute{I}_3|$
  - For restrain current: $I_{res} = (|\acute{I}_1| + |\acute{I}_2| + |\acute{I}_3|) /2$
- When operation mode is 2 windings
  - For differential current: $I_{dff} = |\acute{I}_1 + \acute{I}_2|$
  - For restrain current: $I_{res} = (|\acute{I}_1| + |\acute{I}_2|) /2$

Trip area of the transformer differential, page 260 shows the operating characteristic.

Figure 134 - Trip area of the transformer differential



A Maximum fault = 200% slope B Trip area

Tripping characteristic:

- I_{set}: *LoSet*
- I_{r1}: *LoSet*/2

- *K1*: *DiffSlp1*
- I_{r2}: *Slp2Set*
- *K2*: *DiffSlp2*

If 0.5 × *LoSet* ≤ *BiasCros* ≤ *Slp2Set*,

- I_{trip} = *LoSet* + ($I_{BiasCross}$ - *LoSet*/2) × *DifSlp1*

if *BiasCros* > *Slp2Set*,

- I_{trip} = *LoSet* + (*Slp2Set* - *LoSet*/2) × *DifSlp1* + ($I_{BiasCross}$ - *Slp2Set*) × *DifSlp2*

  NOTE:

  - $I_{BiasCross}$ is the maximum restrain current on three phases.
  - Start operation uses a counter to help ensure correct restraint.

Phase correction

To help ensure the correct operation of transformer differential protection, it is necessary that the transformer primary and secondary currents measured by the relay are in phase. In case of a delta/star transformer, the balanced three-phase current has a phase shift of 30° between the primary and secondary windings. If left uncorrected, this phase difference may lead to the relay detecting the through current as an imbalanced fault current and result in an operation.

Wndg2/***Wndg3*** sets the vector rotation of the 2/3 windings. It also corrects for CT reversal.

- For even numbered windings, the appropriate secondary current is chosen.
- For odd numbered windings, the current is determined by the current difference between the appropriate secondary currents divided by √3.

The Phase correction, page 261 shows the pattern:

- x: any phase
- a: ahead phase
- b: behind phase

  NOTE: For positive sequence with x = A, a is C and b is B.

Table 162 - Phase correction

Winding 2/3 phase shift	Secondary current	A phase secondary current (ABC rotation)
0	Secondary current x	Secondary current A
1	Secondary current x-b/√3	Secondary current (A-B)/√3
2	Secondary current - b	Secondary current - B
3	Secondary current a-b√3	Secondary current (C-B)/√3
4	Secondary current a	Secondary current C
5	Secondary current a-x√3	Secondary current (C-A)/√3
6	Secondary current - x	Secondary current - A
7	Secondary current b-x√3	Secondary current (B-A)/√3
8	Secondary current b	Secondary current B
9	Secondary current b-a√3	Secondary current (B-C)/√3
10	Secondary current - a	Secondary current - C
11	Secondary current x-a√3	Secondary current (A-C)/√3

Zero sequence current filter

When enabled zero sequence filtering is applied, the filtered current is calculated per end as:

$I_0 = (I_A + I_B + I_C)/3$

$I_A' = I_A - I_0$

Where,

- I_A: Phase A current of the respective CT input
- I_A': Phase A filtered current of the respective CT input
- I_0: Zero sequence amplitude matched current for the respective CT input

Otherwise, the filtered current is:

$I_A' = I_A$

Ratio correction

To help ensure the differential element operates correctly, the currents must be balanced under load and fault conditions. As the primary and secondary line CT ratios may not match the transformer rated winding currents exactly, a Matching Factor (MF) is used to balance to the reference winding. The user calculates the MF for each end using the transformer and CT ratings.

$MF = I_{nomx} \times \sqrt{3} \times V_{nomx}/S_{ref}$

Where,

- MF: Match Factor of CT
- I_{nomx}: Rated current for the respective CT input
- V_{nomx}: Reference voltage for winding x (usually rated or mid tap voltage)
- S_{ref}: Common reference power for all ends (usually the transformer VA)

The current used for the differential is:

$I_A'' = MF \times I_A'$

Inrush detection

Any abrupt change of magnetizing voltage may result in a magnetizing inrush. This most commonly occurs during transformer energizing (initial inrush), but can also occur upon voltage recovery after primary system failure (recovery inrush) or voltage drop during energization of a parallel transformer (sympathetic inrush).

This magnetizing inrush current usually flows into one transformer winding only. As a result, it is observed as differential current by the protection. Inrush current detection and prevention from maloperation is an inherent part of the differential protection function.

H2 blocked blocks for 2nd harmonic blocking for inrush and is normally set to cross block unless the transformer comprises three single phase units with a grounded star connection on the energizing side.

- When *H2 blocked* is set to *Off*, inrush detection is disabled.
- When *H2 blocked* is set to *Cross*, the maximum calculated *H2 ratio* is used to block all phases.
- When *H2 blocked* is set to *On*, each phase is compared individually.

The inrush condition is determined by evaluating the ratio between the 2nd harmonic and the fundamental current component, based on the phase segregated differential currents. This signal analysis occurs only if the differential is greater than the fixed minimum current of min (0.1, *LoSet*).

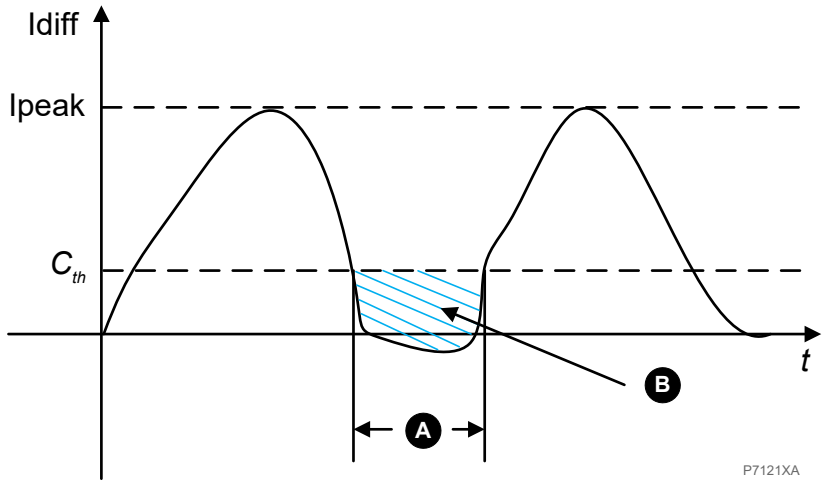
Serious internal faults may result in CT saturation, causing *H2 ratio* > *H2/H1 ratio block value*. As a consequence, differential protection may fail to trip because it is mistakenly blocked by 2nd harmonic. To resolve this problem, 3 methods are used in addition to the unrestrained high-set.

1. If the maximum sample value of differential current in one cycle exceeds *Harmonic block limit*, the inrush block logic will be ignored and the differential protection will trip based on the operation characteristic.

   NOTE: If *Harmonic block limit* is set to zero, inrush block logic works without checking it.

2. Take gap detection logic to distinguish inrush current from fault current.
   - For inrush waveform

Figure 135 - Inrush waveform



A	θ_{gap}	B	Gap region

Inrush waveform, page 264 shows an inrush waveform is split by the threshold C_{th} into two parts. The one shadowed with blue line is termed as gap and is used to identify the inrush.

In the PowerLogic P7,

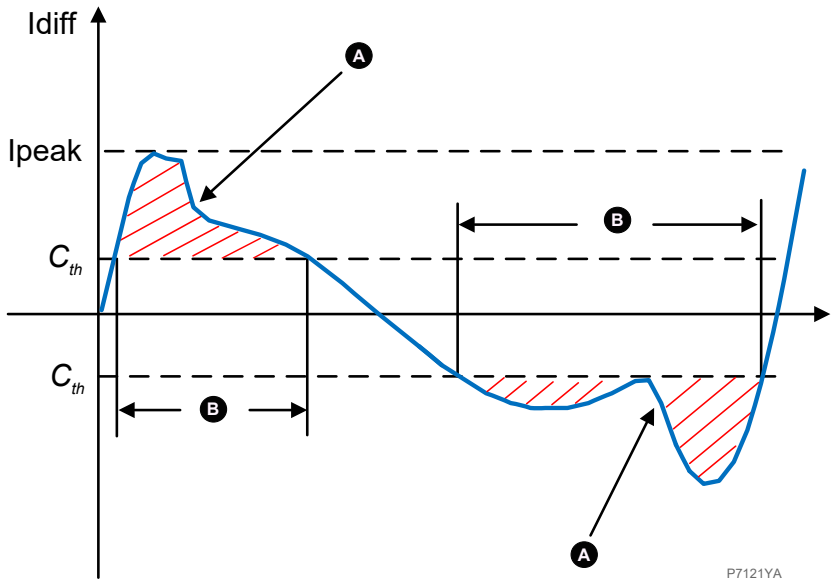
C_{th} = *Ipeak* × sin (360/48)°

θ_{gap} threshold = 10 × (360/48)° = 75°

In one cycle, if the absolute instantaneous value of 10 consecutive samples is below C_{th}, and *H2 ratio* > *H2/H1 ratio block value*, it is regarded as inrush current, differential protection will be blocked by inrush detection logic.

- For CT saturated waveform

Figure 136 - CT saturated waveform



A	Wave width region	B	θ_{width}

CT saturated waveform, page 264 shows an internal fault and CT saturated waveform.

In the PowerLogic P7,

C_{th} = *Ipeak* × sin (2×360/48)°

θ_{width} threshold = 39 × (360/48)° = 292.5°

In one cycle, if the absolute instantaneous value of 39 samples is above C_{th}, and θ_{gap} < 75°, it is regarded as fault current, differential protection will not be blocked by inrush detection logic.

3. Assuming inrush current would be on three phases, it cannot be on single phase. If *H2 ratio* is below 5% on two phases, differential protection will not be blocked by inrush detection logic.

Overfluxing detection

If the transformer is supplied with a voltage more than its rated voltage factor, saturation effects occur leading to short spikes of current at the voltage peaks. Without stabilization, these would lead to differential protection tripping. The fact that the current of the protected object under saturation conditions has a high proportion of 5th harmonic serves as the basis of stabilization.

H5 blocked enables 5th harmonic blocking for ovefluxing.

- When *H5 blocking* is set to *Off*, overflux blocking is disabled.
- When *H5 blocking* is set to *Cross*, the maximum calculated *H5 ratio* is used to block all phases.
- When *H5 blocking* is set to *On*, each phase is compared individually.

Overfluxing condition is determined by evaluating the ratio of 5th harmonic to fundamental current component based on the phase segregated differential currents. This analysis is executed only if the differential is within reasonable limits:

- The fundamental of the differential current is greater than a fixed minimum current of Min (0.1, LoSet).
- All instantaneous differential samples are smaller than *Harmonic block limit*.
- If *Harmonic block limit* is set to zero, the 5th harmonic logic works without checking it.

When overfluxing detection is enabled and an overflusing condition is determined, the differential protection will be blocked.

An alarm will be issued if a sustained overfluxing occurs for longer than *H5 alarm time*.

NOTE: The alarm operates regardless of the *H5 blocking setting* and *Harmonic block limit* setting.

CT saturation detection

During external faults, when CTs saturate, either because of very high fault currents, or because of slowly decaying DC offset of primary current.

Appropriate measures can detect such conditions to prevent false differential tripping. Also a fast reset of this blocking feature is provided for fast differential protection tripping in case of a subsequent fault inside the protection zone.

The external fault detection considers the time to saturation. Immediately after an external fault occurs, the bias current changes, but the differential current only increases after the time to saturation.

CT supervision

In the PowerLogic P7, CTS offers a fast block output with no delay, which can be linked to the inhibit input of transformer differential element to block the element when the CT fails.

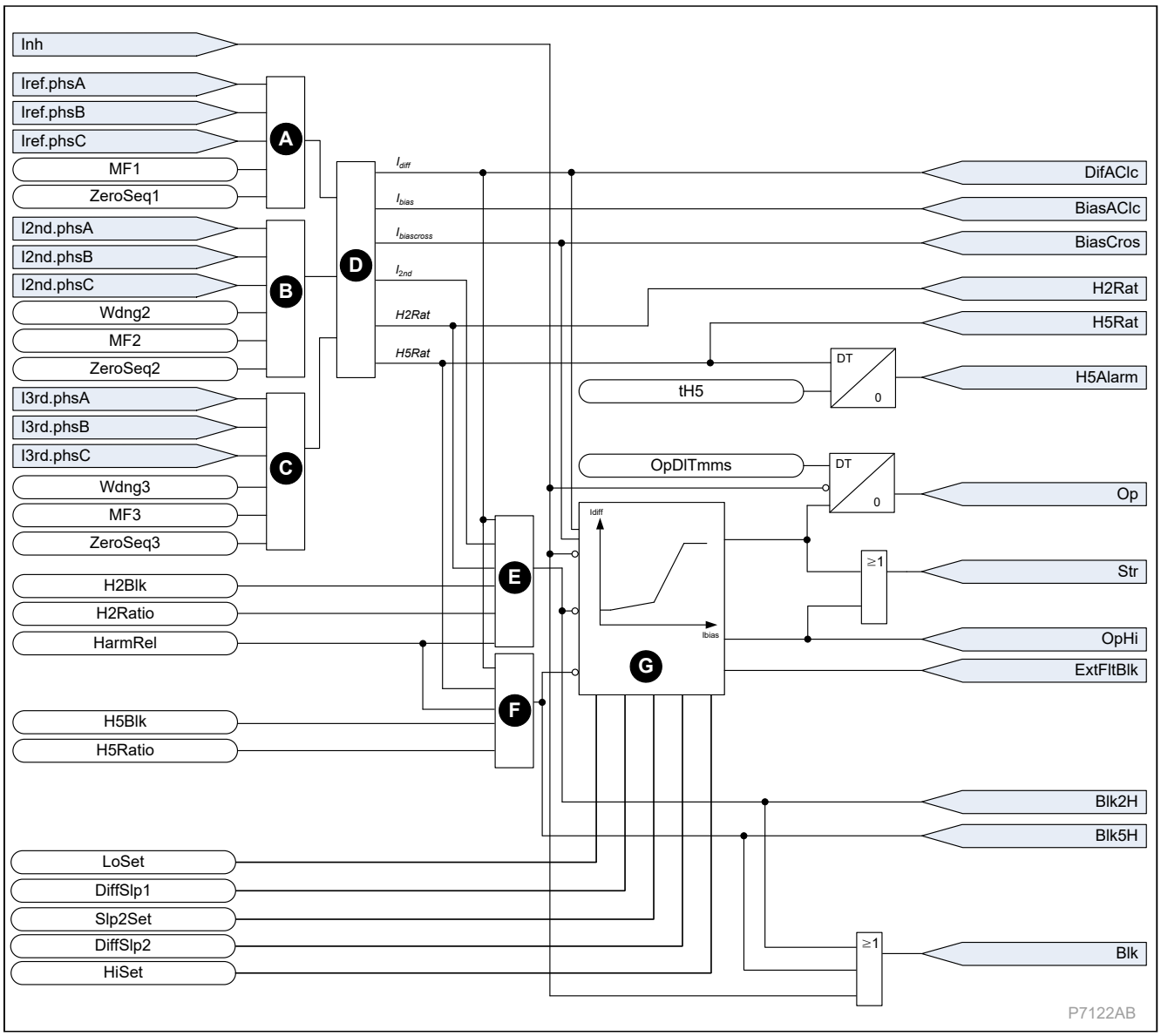
Transformer differential trip logic

The trip function of the transformer differential is impacted by the techniques of CT saturation detection and harmonic detection.

When the 2nd or 5th harmonic blocking is asserted or external fault signal is asserted, the differential protection will be blocked.

Block diagram

Figure 137 - Block diagram of the *TR2PDIF* and *TR3PDIF*



A	Reference current: • Ratio correction • Zero-sequence current filtering	B	2nd current: • Phase correction • Ratio correction • Zero-sequence current filtering	C	3rd current: • Phase correction • Ratio correction • Zero-sequence current filtering
D	Calculating: • Differential current • Biased current • 2nd harmonic current • 5th harmonic current	E	Inrush detection	F	Overfluxing detection

Input and output signals

Table 163 - Input signals of the *TR2PDIF*

Name	Short label	Infotip
Inh[general;phsA; phsB;phsC]	Inhibit	Inhibit function
Iref	Reference current	Reference current
I2nd	Second current	Second current
IrefBias		
I2ndBias		
IrefH2Rat	Reference current H2 ratio	Linked to reference current input source
I2ndH2Rat	Second current H2 ratio	Linked to second current input source

Table 164 - Input signals of the *TR3PDIF*

Name	Short label	Infotip
Inh[general;phsA; phsB;phsC]	Inhibit	Inhibit function
Iref	Reference current	Reference current
I2nd	Second current	Second current
I3rd	Third current	Third current
IrefBias	Reference bias current	Linked to reference current input source
I2ndBias	Second bias current	Linked to second current input source
I3rdBias	Third bias current	Linked to third current input source
IrefH2Rat	Reference current H2 ratio	Linked to reference current input source
I2ndH2Rat	Second current H2 ratio	Linked to second current input source
I3rdH2Rat	Third current H2 ratio	Linked to third current input source

Table 165 - Output signals of the *TR2PDIF*

Name	Short label	Infotip
H5Alarm	H5 alarm	Blocked by fifth harmonic for more than the alarm time
Str	Start	Start
OpHi	High set operate	Unrestrained instantaneous high set operation
Op	Operate	Operate
Blk2H	H2 blocked	Blocked by second harmonic
Blk5H	H5 blocked	Blocked by fifth harmonic

Table 165 - Output signals of the *TR2PDIF* (Continued)

Name	Short label	Infotip
ExtFltBlk	External fault	Blocked by external fault detection
Blk	Blocked	Blocked
BiasAClc	Bias	Bias
BiasCros	Cross bias	Cross bias
DifAClc	Diff	Diff
H2Rat	H2 ratio	H2 ratio
H5Rat	H5 ratio	H5 ratio

Table 166 - Output signals of the *TR3PDIF*

Name	Short label	Infotip
H5Alarm	H5 alarm	Blocked by fifth harmonic for more than the alarm time
Str	Start	Start
OpHi	High set operate	Unrestrained instantaneous high set operation
Op	Operate	Operate
Blk2H	H2 blocked	Blocked by second harmonic
Blk5H	H5 blocked	Blocked by fifth harmonic
ExtFltBlk	External fault	Blocked by external fault detection
Blk	Blocked	Blocked
BiasAClc	Bias	Bias
BiasCros	Cross bias	Cross bias
DifAClc	Diff	Diff
H2Rat	H2 ratio	H2 ratio
H5Rat	H5 ratio	H5 ratio

Setting parameters

Table 167 - Settings of the *TR2PDIF*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
MF1	Winding 1 matching factor	The matching factor is typically set to the nominal current for the winding	0.2...20	0.001	1
ZeroSeq1	Winding 1 I0 filter	Zero sequence filtering is applied when the winding can provide ground fault current	• Off • On		On
Wndg2	Winding 2 phase shift	The vector group relative to winding 1	0...11	1	0
MF2	Winding 2 matching factor	The matching factor is typically set to the nominal current for the winding	0.2...20	0.001	1
ZeroSeq2	Winding 2 I0 filter	Zero sequence filtering is applied when the winding can provide ground fault current	• Off • On		On
LoSet	Start value	Pickup or low set value	0.01...3 pu	0.001 pu	0.2 pu
DifSlp1	Slope 1	Lower slope for mismatch	0.01...2	0.01	0.3
Slp2Set	Slope 2 start value	Upper slope value normally set above load	1...10 pu	0.001 pu	1.5 pu

Table 167 - Settings of the *TR2PDIF* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
DifSlp2	Slope 2	Upper slope for CT saturation	0.1...2	0.01	0.7
OpDlTmms	Operate delay	Operate time delay of the low set bias differential	0...10000000 ms	1 ms	0 ms
HiSet	High set op value	The element operates instantaneously for currents above this level	0...100 pu	0.01 pu	0 pu
H2Blk	H2 blocking	Enables second harmonic blocking for inrush	• Off • On • Cross		Cross
H2Ratio	H2/H1 ratio block value	H2/H1 ratio block value	5...70 %	1 %	20 %
H5Blk	H5 blocking	Enables fifth harmonic blocking for overfluxing	• Off • On • Cross		On
H5Ratio	H5/H1 ratio block value	H5/H1 ratio block value	5...70 %	1 %	35 %
H5AlmTmms	H5 alarm delay	When fifth harmonic blocking exceeds this period an alarm is raised	0...10000000 ms	1 ms	10000 ms
HarmRel	Harmonic block limit	The second and fifth harmonic blocks are removed when the bias exceeds this level	0...100 pu	0.01 pu	10 pu

Table 168 - Settings of the *TR3PDIF*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
OpMod	Transformer type	Transformer type	• 2 winding • 3 winding		2 winding
MF1	Winding 1 matching factor	The matching factor is typically set to the nominal current for the winding	0.2...20	0.001	1
ZeroSeq1	Winding 1 I0 filter	Zero sequence filtering is applied when the winding can provide ground fault current	• Off • On		On
Wndg2	Winding 2 phase shift	The vector group relative to winding 1	0...11	1	0
MF2	Winding 2 matching factor	The matching factor is typically set to the nominal current for the winding	0.2...20	0.001	1
ZeroSeq2	Winding 2 I0 filter	Zero sequence filtering is applied when the winding can provide ground fault current	• Off • On		On
Wndg3	Winding 3 phase shift	The vector group relative to winding 1	0...11	1	0
MF3	Winding 3 matching factor	The matching factor is typically set to the nominal current for the winding	0.2...20	0.001	1
ZeroSeq3	Winding 3 I0 filter	Zero sequence filtering is applied when the winding can provide ground fault current	• Off • On		On
LoSet	Start value	Pickup or low set value	0.01...3 pu	0.001 pu	0.2 pu
DifSlp1	Slope 1	Lower slope for mismatch	0.01...2	0.01	0.3
Slp2Set	Slope 2 start value	Upper slope value normally set above load	1...10 pu	0.001 pu	1.5 pu
DifSlp2	Slope 2	Upper slope for CT saturation	0.1...2	0.01	0.7
OpDlTmms	Operate delay	Operate time delay of the low set bias differential	0...10000000 ms	1 ms	0 ms
HiSet	High set op value	The element operates instantaneously for currents above this level	0...100 pu	0.01 pu	0 pu
H2Blk	H2 blocking	Enables second harmonic blocking for inrush	• Off • On • Cross		Cross

Table 168 - Settings of the *TR3PDIF* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
H2Ratio	H2/H1 ratio block value	H2/H1 ratio block value	5...70 %	1 %	20 %
H5Blk	H5 blocking	Enables fifth harmonic blocking for overfuxing	• Off • On • Cross		On
H5Ratio	H5/H1 ratio block value	H5/H1 ratio block value	5...70 %	1 %	35 %
H5AlmTmms	H5 alarm delay	When fifth harmonic blocking exceeds this period an alarm is raised	0...10000000 ms	1 ms	10000 ms
HarmRel	Harmonic block limit	The second and fifth harmonic blocks are removed when an instantaneous differential sample exceeds this level	0...100 pu	0.01 pu	10 pu

Characteristics

Table 169 - Characteristics of the *TR2PDIF* and *TR3PDIF*

Characteristics		Values
Start value	Accuracy	±5% or ±0.001 pu
	Reset ratio	95% ± 5%
	Start time@nomHz	< 35 ms with harmonic restrain (2 Is sinusoid)
		< 30 ms without harmonic restrain (2 Is sinusoid)
		< 20 ms (2 × HiSet sinusoid)
	Reset time	< 30 ms
Operate delay	DT Accuracy	±2% or ±10 ms
	Reset time	< 30 ms
H5 alarm	DT Accuracy	±2% or ±10 ms
	Reset time	< 30 ms (0 Is)
Blocked	Accuracy (H2/H1 and H5/H1 blocking)	±5% or ± 0.01 pu (H1 > Start value)
	Block time	< 20 ms
	Reset time	20...40 ms

Motor thermal overload (*THMPTTR*, ANSI 49)

Description

The motor thermal overload protection function can be applied to help prevent damage on the stator and rotor against overloading conditions due to balanced and unbalanced currents.

- This function incorporates current based stator and rotor thermal levels, using three-phase RMS currents and sequence currents to reproduce the heating and cooling of the equipment to be protected.
- The stator thermal level considers the overheating generated by three-phase RMS currents and the negative sequence current. The average of the three-phase currents is used, and the weighting of negative sequence current is settable depending on motor characteristic.

- Flexible choices of time constants used in stator thermal level calculation are provided. The four settable constants align with the four machine statuses. In addition, a four-point curve can be defined for the overload state.
- Temperature influence is provided to compensate for the reduction in the motor thermal limits when the ambient temperature is above the rated ambient. If ambient temperature measurement is not available, the factor is ignored.
- The rotor thermal level takes heating generated from the negative and positive sequence currents and heating transfer from stator. Two calculation methods are applied for starting and non-starting motor status separately.
- The start thermal level of the stator is monitored, and the maximum start level is memorized. It can be used to automatically adapt the thermal restart inhibit based on the maximum of the last 5 starts.

Stator thermal level

In the motor thermal protection, an overall thermal model is used.

$$Hs(t) = \left(\frac{Ieq}{Is} \right)^2 \times \frac{\Delta t}{\tau + \Delta t} + Hs(t - \Delta t) \times \frac{\tau}{\tau + \Delta t}$$

E71137A

Hs(t) is the stator thermal level at time t and the output is *StaTL*;

Hs(t - Δt) is the stator thermal level at time (t - Δt);

Δt is the calculation interval;

τ is the time constant;

Ieq is the equivalent heating current;

Is is the overload current threshold.

Equivalent heating current

The equivalent heating current computes from the average value of the three-phase RMS currents and the negative sequence current multiplied by an adjustable coefficient. When the calculated *Ieq* is less than 0.05 x FLA, the equivalent heating current is ignored.

$$Ieq = \sqrt{\frac{IA^2 + IB^2 + IC^2}{3} + q \times I2^2}$$

E71138A

IA, IB, IC are the RMS phase currents;

I2 is the negative sequence phase current;

q is the settable *Neg seq factor* when *RotMod* is disabled. When *RotMod* is enabled, q is calculated with following equation.

$$q = 2 \times \frac{T_{str}}{S_{nom} \times (I_{LR} \times FLA)^2}$$

E71139A

T_{str} is the start torque from setting *StrTrq*;

S_{nom} is the nominal slip from setting *NomSlip*;

I_{LR} is locked rotor current from setting *LckRotA*.

Temperature influence factor

When ambient temperature is higher than the motor nominal working temperature, thermal level will increase faster for tripping promptly. When ambient temperature

measurement is unavailable (invalid quality, RTD errors, no temperature source and so on), Fa is set to 1.

$$Fa = \frac{Tmax - Tnom}{Tmax - Tamb}$$ E71140A

T_{max} is the maximum motor tolerance temperature from setting *TmpMax*;

T_{nom} is the nominal motor temperature from setting *TmpNom*;

T_{amb} is the ambient temperature from input *TmpAmb*;

When T_{nom} is higher than the ambient temperature, the factor is fixed to the minimum value 1.

Overload current threshold

The overload threshold is determined by the overload setting *StrVal* and the temperature factor.

$$Is = \frac{StrVal \times FLA}{\sqrt{Fa}}$$ E71141A

StrVal is the overload threshold;

FLA is the full load current.

Time constant

The time constants used in thermal level calculation depends on equivalent current and whether programmable curve function is enabled.

- When *TmACrv* = *Thermal* (programmable curve is disabled)

  Ieq ≤ 0.05 x FLA, the time constant is from setting *StpTC*;

  0.05 x FLA < Ieq < Is, the time constant is from setting *RunTC*;

  Is ≤ Ieq ≤ 2.8 x FLA, the time constant is from setting *OlTC*;

  Ieq > 2.8 x FLA, the time constant is from setting *StrTC*.

- When *TmACrv* = *Curve* (four points curve is applied)

  The time constant values (*TmACrvPt0*, *TmACrvPt1*, *TmACrvPt2* and *TmACrvPt3*) of the fixed four equivalent heating currents at 1.4 x FLA, 1.6 x FLA, 1.8 x FLA and 2.0 x FLA can be set. The time constant is the linear interpolation between the fixed points.

  This four-point curve provides a flexible tripping characteristic when *Ieq* is in the range of *Is* to 2.8 x FLA. For Ieq < Is, *RunTC* is used and when Ieq > 2.8 x FLA, *StrTC* will be applied in thermal calculation.

  When *Is* is more than 1.4 x FLA, *TmACrvPt0* is ignored. The following two time constant curves are shown as examples.

Figure 138 - Example of time constant curve when Is < 1.4 x FLA

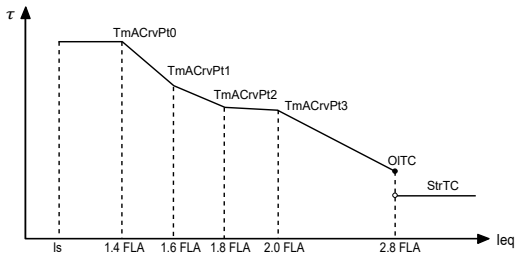
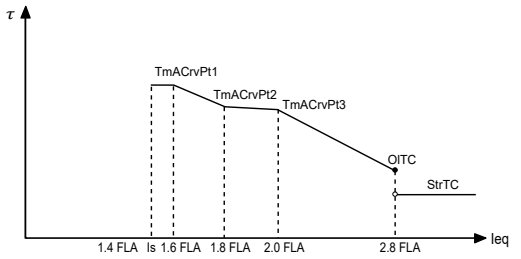


Figure 139 - Example of time constant curve when Is > 1.4 x FLA



Rotor thermal level

The rotor mode setting *RotMod* is provided to enable/disable the rotor thermal calculation. When the rotor mode is disabled, the rotor thermal is not calculated and is equal to the stator thermal. When the rotor mode is enabled, two rotor thermal levels are used according to the motor status.

Rotor thermal level when Starting

$$Hr(t) = \frac{R1 \times I1^2 + R2 \times I2^2}{(I_{LR} \times \mathrm{FLA})^2} \times \frac{1}{R_{LR}} \times \frac{\Delta t}{T_{op}} + Hr(t - \Delta t)$$

E71142A

$$R_{LR} = \frac{T_{str}}{(I_{LR} \times \mathrm{FLA})^2}$$

E71143A

$$R1 = (R_{LR} - R_N) \times s + R_N$$

E71144A

$$R2 = (R_{LR} - R_N) \times (2 - s) + R_N$$

E71145A

Hr(t) is the rotor thermal level at time t and the output is *RotTL*;

Hr(t - Δt) is the rotor thermal level at time (t - Δt);

I1, I2 is the positive and negative sequence phase currents;

T_{str} is the start torque from setting *StrTrq*;

s is the machine slip (If it is not available, the default value will be 1);

I_{LR} is locked rotor current from setting *LckRotA*;

R_N is the nominal slip from setting *NomSlip*;

T_{op} is the cold trip time from setting *Tcold*.

For short time starting, it is reasonable to consider the rotor is adiabatic (no heat transfer between iron and copper and heat dissipation).

Rotor thermal level when Running and Stopped

$$Hr\_cal(t) = \frac{\tau rotor}{\tau rotor + \Delta t} \times Hr(t - \Delta t) + k \times Hs(t) \times \frac{\Delta t}{\tau rotor + \Delta t}$$ E71146A

$$R_{LR} = \frac{T_{str}}{(I_{LR} \times \mathrm{FLA})^2}$$ E71143A

$$k = 1 - \frac{T_{hot}}{T_{cold}}$$ E71146A

$$\tau rotor = \frac{R_{LR}}{R_N} \times (I_{LR} \times FLA)^2 \times (T_{cold} - T_{hot})$$ E71148A

$$Hr(t) = \max [\min (k, Hs(t)), Hr\_cal(t)]$$ E71149A

Hr_cal(t) is the calculated rotor thermal level at time t;

Hr(t) is the rotor thermal level at time t and the output is *StaTL*;

Hr(t - Δt) is the rotor thermal level at time (t - Δt);

Hs(t) is the stator thermal level at time t;

T_{str} is the start torque from setting *StrTrq*;

I_{LR} is locked rotor current from setting *LckRotA*;

R_N is the nominal slip from setting *NomSlip*;

T_{cold} is the stall tolerance time at cold status;

T_{hot} is the stall tolerance time at hot status;

If the stator thermal level is more than *k* and the calculated rotor thermal level is less than *k*, the rotor thermal level will be set to *k*.

If the stator thermal level is less than *k* then the rotor thermal level will equal the stator thermal level.

Additional features

Although the PowerLogic P7 monitors the rotor and stator thermal levels separately, the stator thermal level always dominates for resetting due to its higher time constant. The remaining time to operate, start level calculation and blocking time use the stator thermal level for calculation.

Remaining time to operate

When the equivalent current exceeds the overload threshold, the operate delay of the thermal overload protection can be calculated with the following equation:

$$top = \tau \times \ln \frac{\left(\frac{Ieq}{Is}\right)^2 - Hs}{\left(\frac{Ieq}{Is}\right)^2 - 1}$$ E71151A

top is the remaining time to operate and the output is *RsvTmm*;

τ is the time constant;

Ieq is the equivalent heating current;

Is is the overload current threshold.

When the remaining time to operate is less than the remaining time alarm threshold *RsvVal*, a remaining time to operate alarm is issued.

Start thermal level

Start thermal level is recorded when the machine status changes from Stopped to Starting.

$$Hstr = Hsaftstr - Hsprestr$$

E71152A

Hstr is the calculated start level and the output is *StrLev*;

Hsprestr is the thermal level of the moment when the machine starts;

Hsaftstr is the thermal level of the moment when the machine stops.

The output *MaxStrLev* is the maximum start thermal level of the last five successful starts. The maximum start thermal level will be retained after a restart.

Blocking time

Starting will be inhibited when the stator thermal level is above the restart level to prevent over heating during starting.

The blocking time is calculated as follows:

- Manual mode

  $$t_{blk} = -\tau_{stp} \times \ln \frac{Hrsv}{Hs}$$

  E71153A

  Start block output *BlkThm* is issued when stator thermal level is higher than start thermal level threshold setting *RsvTL*.

- Automatic mode

  $$t_{blk} = -\tau_{stp} \times \ln \frac{1 - Hmaxstr - 5\%}{Hs}$$

  E71154A

  Start block output *BlkThm* is issued when stator thermal level is higher than (95% - *Hmaxstr*).

t_{blk} is the block time and the output is *BlkTms*;

τ_{stp} is the time constant from setting *StpTC*;

Hrsv is the start thermal level threshold setting *RsvTL*;

Hmaxstr is the maximum start level from output *MaxStrLev*.

Thermal overload logic

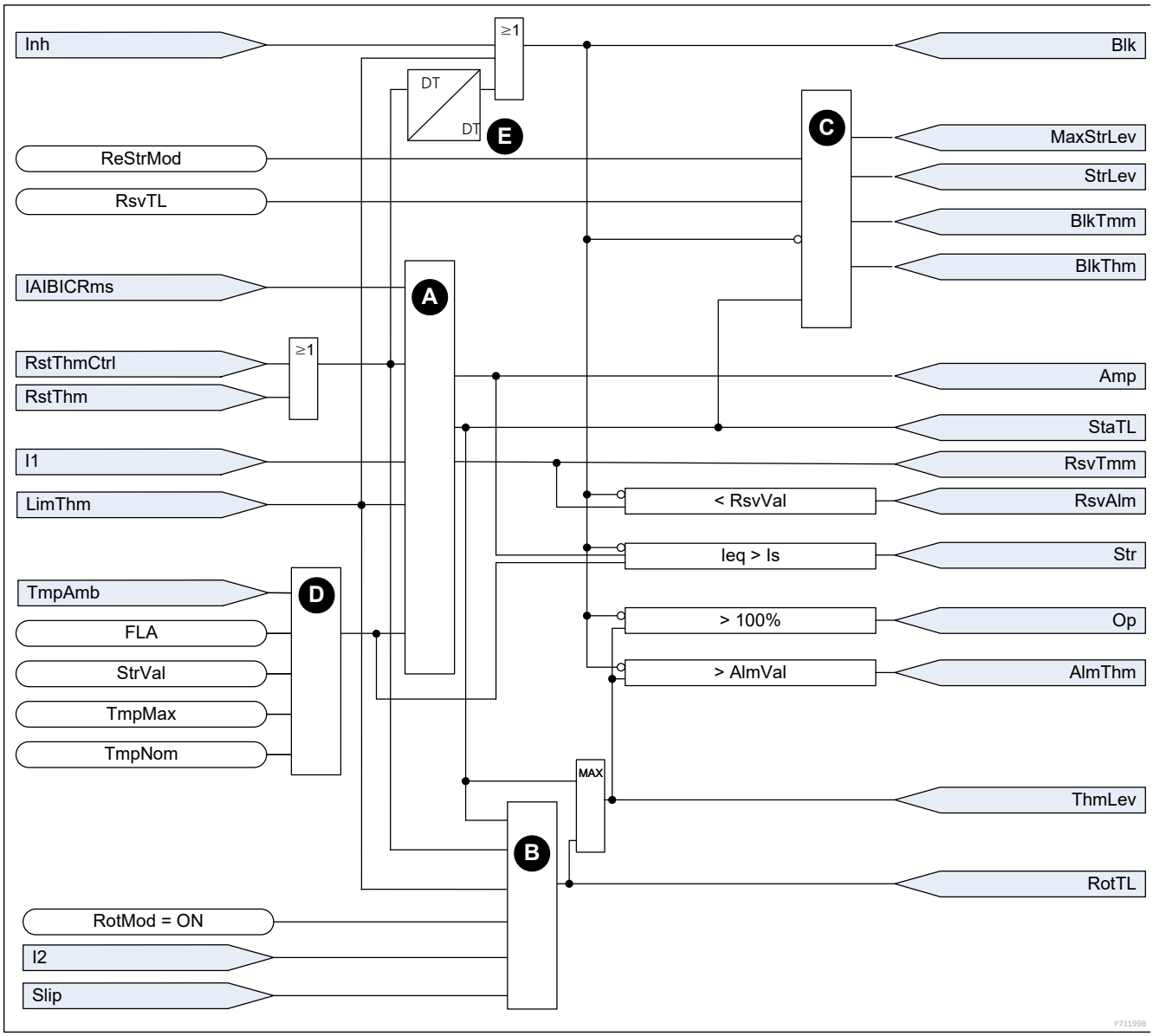
The thermal level output *ThmLev* is the maximum value of stator and rotor thermal level. The thermal overload function will be blocked if the *Inhibit* input is active.

When the thermal level exceeds the alarm setting *AlmVal*, an alarm signal is issued. If the equivalent current exceeds the overload threshold, the start signal is issued. When the thermal level reaches 100%, the operate signal issues.

The stator and rotor thermal levels can be reset to 0 via an input *RstThm* and a control input *RstThmCtrl*. If the *LimThm* input is active, the stator and rotor thermal levels will be reset to 90% if it is greater than 90% or stays as it is if less than 90% and the block output is issued.

Block diagram

Figure 140 - Block diagram of the *THMPTTR*



A	Stator thermal level calculation	B	Rotor thermal level calculation
C	Start thermal level calculation	D	Overload current threshold calculation
E	Operate delay: 1 s Reset delay: 0 s		

Input and output signals

Table 170 - Input signals of the *THMPTTR*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
IAIBICRms	Phase RMS current	Phase RMS current
I2	I2	Linked to phase RMS curent source
I1	I1	Linked to phase RMS curent source
Slip	Slip	Internal signal from TRTN1

Table 170 - Input signals of the *THMPTTR* (Continued)

Name	Short label	Infotip
TmpAmb	Ambient temp	Internal signal from RTDTTMP channel 8
LimThm	Limit	Limit thermal state to 90%
RstThm	Reset	Reset thermal state
RstThmCtrl	Reset thermal state	Reset thermal state

Table 171 - Output signals of the *THMPTTR*

Name	Short label	Infotip
AlmThm	Thermal alarm	Thermal alarm
Str	Start	Start
RsvTmm	Time to operate	Time to operate
RsvAlm	Time to operate alarm	Time to operate alarm
Op	Operate	Operate
BlkTmm	Time to restart	Time to restart
BlkThm	Block closing	Block closing
Blk	Blocked	Blocked
Amp	Thermal current	Thermal current
StaTL	Stator thermal state	Stator thermal state
RotTL	Rotor thermal state	Rotor thermal state
ThmLev	Thermal state	Thermal state
StrLev	Last start heating	Last start heating
MaxStrLev	Max start heating	Max start heating
Tmp	Ambient temperature	Ambient temperature

Setting parameters

Table 172 - Settings of the *THMPTTR*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrVal	Start value (xFLA)	The start value is a multiple of the full load current which is defined in bay configuration	1...1.5	0.01	1
NegQ	Neg seq factor	This sets the negative sequence factor in the equivalent thermal current formula. It can be calculated from nominal slip, locked rotor current and starting torque	0...20	0.1	0
StpTC	Stopped time constant	This time constant is used when the current is below 0.05pu and is taken from the motor data sheet	1...1000 min	0.1 min	30 min
RunTC	Running time constant	This time constant is used when the current is above 0.05pu and below the start value. It is taken from the motor data sheet	1...1000 min	0.1 min	30 min
OlTC	Overload time constant	This time constant is used when the current is above the start value and below 2.8 x FLA in thermal mode. It is determined from the overload curve. In 4 point mode it is the time constant at 2.8 x FLA	1...1000 min	0.1 min	30 min

Table 172 - Settings of the *THMPTTR* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
StrTC	Starting time constant	This time constant is used when current is above 2.8 x FLA. It is usually the same as the overload time constant	1...1000 min	0.1 min	30 min
AlmVal	Thermal alarm value	Thermal alarm value	50...100 %	1 %	90 %
RsvVal	Time to operate alarm value	The time to operate is calculated based on the current measurement. If the time is less than this value the alarm is raised	1...1000 min	1 min	30 min
TmpNom	Nominal temperature	The machine nominal temperature is normally 40°C	-40...300 °C	1 °C	40 °C
TmpMax	Max temperature	The maximum temperature is normally determined based on the machine insulation class	0...300 °C	1 °C	130 °C
RotMod	Rotor mode	In rotor mode the rotor has a different thermal model above 2.8 x FLA based on the stall times	• Off • On		Off
LckRotA	Locked rotor current (xFLA)	The locked rotor current is used with stall times	3...10	0.01	6
StrTrq	Start torque	Start torque	0.1...1	0.01	0.7
NomSlip	Nominal slip	Nominal slip	0.0001...0.3 pu	0.0001 pu	0.01 pu
Tcold	Cold stall time	Cold stall time	1...10000 s	0.001 s	10 s
Thot	Hot stall time	Hot stall time	0...10000 s	0.001 s	6 s
RestrMod	Restart mode	In auto mode the maximum thermal capacity used in the last 5 starts is used to determine the restart level with a 5% buffer	• Auto • Manual		Auto
RsvTL	Restart level	The stator thermal level must drop below this value to allow starting	5...100 %	1 %	30 %
TmACrv	Overload characteristic	In thermal mode the overload time constant is used between the start value and 2.8 x FLA. In 4 point mode the time constant is interpolated between the 4 points and the overload time constant	• Thermal • 4 point curve		
TmACrvPt0	1.4 x FLA time constant	1.4 x FLA time constant	1...1000 min	0.1 min	30 min
TmACrvPt1	1.6 x FLA time constant	1.6 x FLA time constant	1...1000 min	0.1 min	30 min
TmACrvPt2	1.8 x FLA time constant	1.8 x FLA time constant	1...1000 min	0.1 min	30 min
TmACrvPt3	2.0 x FLA time constant	2.0 x FLA time constant	1...1000 min	0.1 min	30 min

Characteristics

Table 173 - Characteristics of the *THMPTTR*

Characteristics		Values
Alarm thermal level	Accuracy	Setting value ±2%
Operate thermal level	Accuracy	100% ± 2%
Alarm delay	Accuracy	±2% or ±500 ms (alarm time delay < 400 minutes)
Operate delay	Accuracy	±2% or ±500 ms (trip time delay < 400 minutes)
Characteristic time	Start time	< 35 ms at 2 Is
	Disengaging time	< 100 ms (fixed 50 ms drop-off delay to avoid chatter)

Thermal overload (*THFPTTR*, ANSI 49F)

Description

The thermal overload protection can be applied to help prevent the plant damage caused by operating at temperatures exceeding design limits. Such damage includes excessive sagging of overhead lines, destruction of the conductor material, insulation deterioration in cables, overloads in transformers and so on.

A thermal model is used to calculate the thermal level of the plant, which can be feeder, transformer and so on. The thermal model uses the maximum of the three-phase RMS currents, configurable time constants, and optionally the ambient temperature, as the main inputs to calculate the thermal level.

When the calculated thermal level reaches the configured *Thermal alarm value* such as 90%, an alarm is triggered to prompt operator intervention. If operators do not intervene and the calculated thermal level continues rising to 100%, a trip signal is issued.

Plant thermal level

Equivalent heating current

The equivalent heating current is calculated from the maximum value of the three-phase RMS currents. When the calculated $I_{eq}(t)$ is less than 0.05 x FLA, the equivalent heating current is ignored.

$$I_{eq} = max(IA_{RMS}, IB_{RMS}, IC_{RMS})$$ E71187

Thermal Level Calculation

When I_{eq} is above 0.05 x FLA, the thermal level H is calculated with the following equation:

$$H(t) = H(t - \Delta t) + Fa \times \left(\frac{I_{eq}(t)}{StrVal \times FLA}\right)^2 \times \frac{\Delta t}{\tau + \Delta t} - H(t - \Delta t) \times \frac{\Delta t}{\tau + \Delta t}$$ E71188

When I_{eq} is below 0.05 x FLA, the thermal level H will decay exponentially to zero and is calculated with the following equation:

$$H(t) = H(t - \Delta t) - H(t - \Delta t) \times \frac{\Delta t}{\tau + \Delta t}$$ E71190

H(t) is the thermal level at time t;

H(t-Δt) is the thermal level at time t-Δt;

Δt is the calculation interval;

Ƭ is the thermal time constant at I_{eq}, as detailed in Time constant, page 280;

Fa is the temperature influence factor.

Temperature influence factor

The temperature influence factor is introduced because the thermal withstand is reduced when the ambient temperature is higher than the plant nominal working temperature. The factor is calculated with the following equation:

$$Fa = \frac{T_{max} - T_{nom}}{T_{max} - T_a}$$ E71189

T_{max} is the maximum working temperature of the plant from the *Max temperature* setting;

T_{nom} is the nominal ambient temperature of the plant from the *Nominal temperature* setting;

T_a is the ambient temperature of the plant from input *Ambient temp*.

The minimum value of Fa is 1. When T_a is unavailable, invalid, lower than T_{nom}, or higher than T_{max}, the value of Fa is fixed to 1.

Overload current threshold

The overload current threshold is determined by the start value and the temperature influence factor. When I_{eq} is above the overload current threshold, the function activates and will trip when the thermal level reaches 100%.

NOTE: When the thermal level reaches the configured *Thermal alarm value*, which is usually less than 100%, an alarm is triggered to prompt operator intervention.

The overload current threshold is calculated with the following equation:

$$Is = \frac{StrVal \times FLA}{\sqrt{Fa}}$$ E71141A

Time constant

The time constant used in the thermal model depends on the equivalent heating current and the *Overload characteristic* setting.

NOTE: The thermal overload characteristic is usually applied to plant with single thermal mass such as an overhead line. The four-point curve overload characteristic can be applied to items with multiple masses such as the oil, insulation and windings in a transformer.

- When *Overload characteristic* = *Thermal* (programmable curve is disabled):
  - If $I_{eq} \leq 0.05 \times FLA$, the time constant is from setting *Cooling time constant*;
  - If $0.05 \times FLA < I_{eq} < I_s$, the time constant is from setting *Running time constant*;
  - If $I_{eq} \geq I_s$, the time constant is from setting *Overload time constant*.

- When setting *Overload characteristic = 4 point curve* (programmable curve is enabled), users can set the time constant values (*TmACrvPt0*, *TmACrvPt1*, *TmACrvPt2* and *TmACrvPt3*) of the fixed four equivalent heating currents at 1.4 x FLA, 1.6 x FLA, 1.8 x FLA and 2.0 x FLA. The time constant is the linear interpolation between the fixed points.

  This four-point curve provides a flexible tripping characteristic when I_{eq} is in the range of I_s to 2.8 x FLA:

  - If $I_{eq} \leq 0.05$ x FLA, the time constant is from setting *Cooling time constant*;
  - If 0.05 x FLA < I_{eq} < I_s, the time constant is from setting *Running time constant*;
  - If $I_s \leq I_{eq} < 2.8$ x FLA, the time constant is determined by the programmable curve;
  - If $I_{eq} \geq 2.8$ x FLA, the time constant is from setting *Overload time constant*.

  The following two time constant curves are shown as examples:

  NOTE: If I_s is more than 1.4 x FLA, *TmACrvPt0* is ignored.

Figure 141 - Example of time constant curve when $I_s \leq 1.4$ x FLA

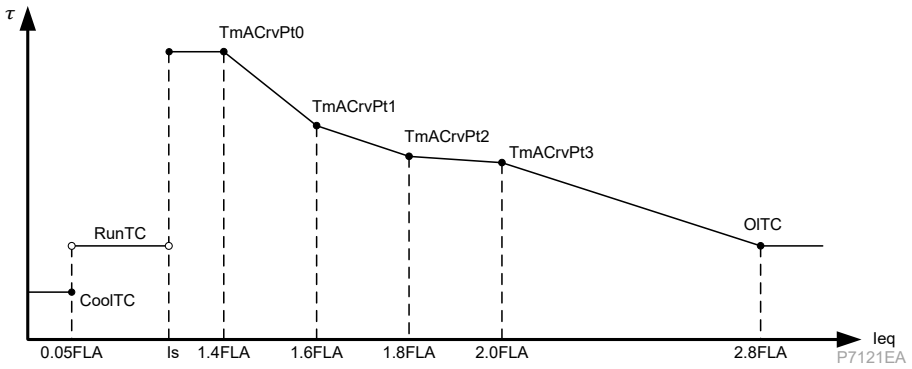
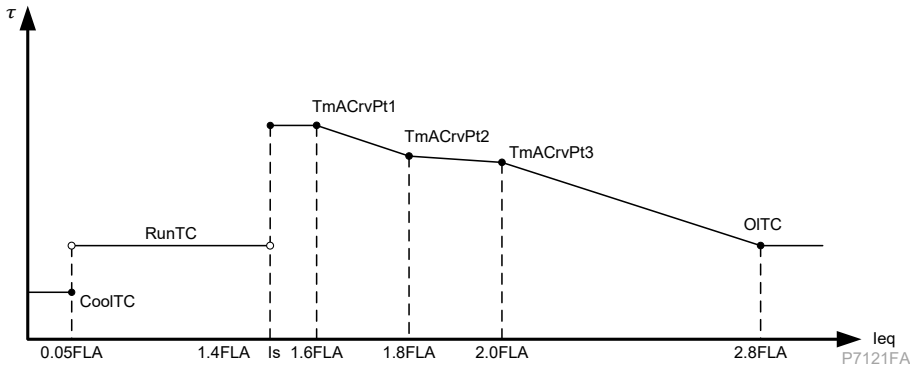


Figure 142 - Example of time constant curve when $I_s > 1.4$ x FLA



Additional features

Remaining time to trip

If the function starts, the remaining time to trip can be calculated with the following equation on the condition that the load current present stays constant:

$$t_{op} = \tau \times \ln\left[\frac{\left(\frac{I_{eq}}{I_s}\right)^2 - H(t)}{\left(\frac{I_{eq}}{I_s}\right)^2 - 100\%}\right]$$

E71192

t_{op} is the *Time to operate*;

τ is the time constant;

I_{eq} is the equivalent heating current;

I_s is the overload current threshold.

When the *Time to operate* is less than the *Time to operate alarm value* setting, an alarm is raised.

Blocking time to restart

After a trip, if the thermal level is above the *Restart level* setting, restarting will be blocked for a calculated amount of time to prevent re-tripping.

The blocking time is calculated with the following equation:

NOTE: The following equation is only valid for zero current. When $I_{eq}(t) > 0.05$ x FLA or the three phase RMS currents are all invalid, the blocking time will be zero.

$$t_{blk} = -\tau \times \ln\left(\frac{RsvTL}{H}\right)$$

E71191

t_{blk} is the blocking time and the output is *BlkTmm*;

RsvTL is the *Restart level* setting;

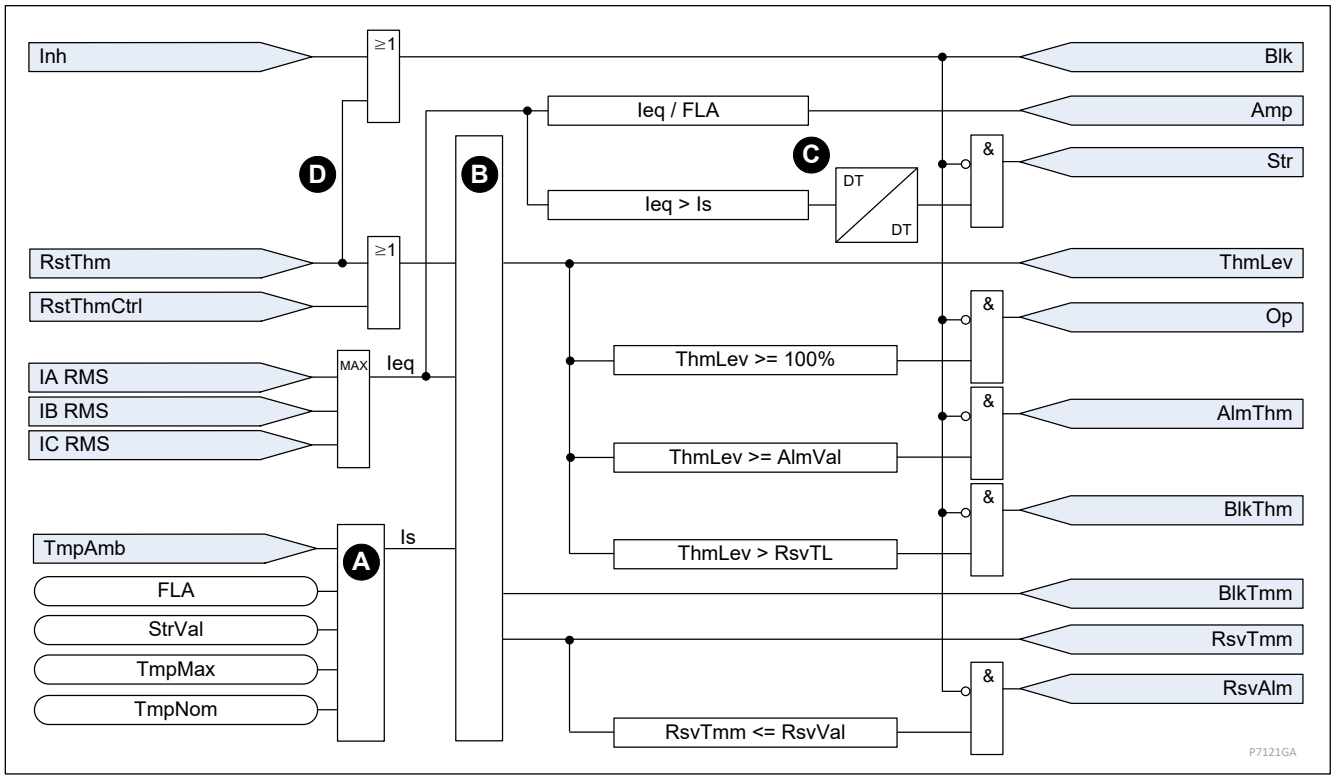
τ is the time constant from setting *Running time constant*;

When H > RsvTL, a blocking signal is issued after a trip.

When H ≤ RsvTL, the blocking time will be zero and no blocking signal is issued after a trip.

Block diagram

Figure 143 - Block diagram of the *THFPTTR*



A	Overload current threshold calculation	B	Thermal level calculation
C	Drop-off delay: 50 ms	D	TRUE for more than 1s

Input and output signals

Table 174 - Input signals of the *THFPTTR*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
IAIBICRms	Phase RMS current	Phase RMS current
TmpAmb	Ambient temp	Ambient temp
RstThm	Reset	Reset thermal state
RstThmCtrl	Reset thermal state	Reset thermal state

Table 175 - Output signals of the *THFPTTR*

Name	Short label	Infotip
AlmThm	Thermal alarm	Thermal alarm
Str	Start	Start
RsvTmm	Time to operate	Time to operate
RsvAlm	Time to operate alarm	Time to operate alarm value.
Op	Operate	Operate
BlkThm	Block closing	Block closing
BlkTmm	Time to restart	Time to restart
Blk	Blocked	Blocked

Table 175 - Output signals of the *THFPTTR* (Continued)

Name	Short label	Infotip
Amp	Thermal current	Thermal current
ThmLev	Thermal state	Thermal state
Tmp	Ambient temperature	Ambient temperature

Setting parameters

Table 176 - Settings of the *THFPTTR*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrVal	Start value (xFLA)	The start value is a multiple of the full load current which is defined in bay configuration	1...1.5	0.01	1
CoolTC	Cooling time constant	This time constant is used when the current is below 0.05pu.	1...1000 min	0.1 min	30 min
RunTC	Running time constant	This time constant is used when the current is above 0.05pu and below the start value	1...1000 min	0.1 min	30 min
OlTC	Overload time constant	This time constant is used when the current is above the start value in thermal mode. In 4 point mode it is the time constant above 2.8 x FLA	1...1000 min	0.1 min	30 min
AlmVal	Thermal alarm value	Thermal alarm value	50...100 %	1 %	90 %
RsvVal	Time to operate alarm value	The time to operate is calculated based on the current measurement. If the time is less than this value the alarm is raised	1...1000 min	1 min	30 min
TmpNom	Nominal temperature	The plant nominal temperature is normally 40°C	-40...300 °C	1 °C	40 °C
TmpMax	Max temperature	The maximum temperature is normally determined based on the plant insulation withstand or line sag	0...300 °C	1 °C	130 °C
RsvTL	Restart level	The thermal level must drop below this value to allow closing	5...100 %	1 %	90 %
TmACrv	Overload characteristic	In thermal mode the overload time constant is above the start value. In 4 point mode the time constant is interpolated between the 4 points and the overload time constant	• Thermal • 4 point curve		
TmACrvPt0	1.4 x FLA time constant	1.4 x FLA time constant	1...1000 min	0.1 min	30 min
TmACrvPt1	1.6 x FLA time constant	1.6 x FLA time constant	1...1000 min	0.1 min	30 min
TmACrvPt2	1.8 x FLA time constant	1.8 x FLA time constant	1...1000 min	0.1 min	30 min
TmACrvPt3	2.0 x FLA time constant	2.0 x FLA time constant	1...1000 min	0.1 min	30 min

Characteristics

Table 177 - Characteristics of the *THFPTTR*

Characteristics		Values
Alarm thermal level	Accuracy	Setting value ± 2%
Operate thermal level	Accuracy	100% ± 2%
Alarm delay	Accuracy	± 2% or ± 500 ms (alarm time delay < 400 minutes)

Table 177 - Characteristics of the *THFPTTR* (Continued)

Characteristics		Values
Operate delay	Accuracy	± 2% or ± 500 ms (trip time delay < 400 minutes)
Characteristic time	Start time	< 35 ms at 2 Is
	Disengaging time	< 100 ms (fixed 50 ms drop-off delay to avoid chatter)

Overtemperature (*STMP*, ANSI 38/49T)

Description

The temperature is monitored by Resistance Temperature Detector (RTD), it is installed in different locations (bearing/winding/ambient etc.)

The function has two independent set points:

- Alarm set point.

  NOTE: Once temperature reaches this threshold, an alarm signal will be issued.

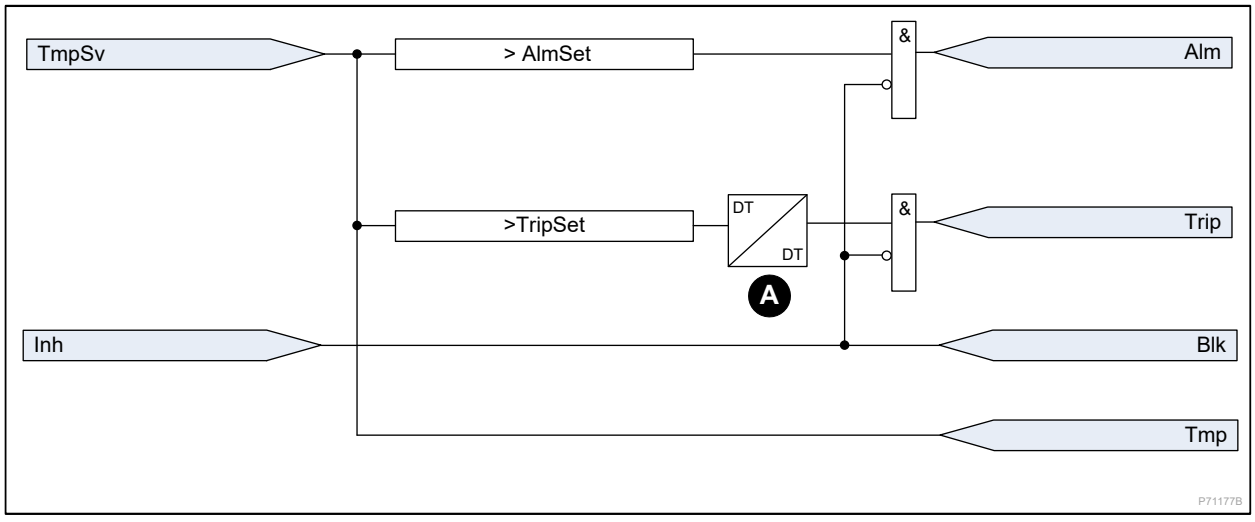
- Tripping set point.

  NOTE: If temperature keeps rising and exceeds the operate temperature, an operate signal will be issued to trip the circuit.

The measurement is valid from -31°C to 201°C. Outside of this range the measurement is marked as invalid and the *Blocked* output is active.

Block diagram

Figure 144 - Block diagram of the *STMP*



A Operate delay: 200 s
Reset delay: 0 ms

Input and output signals

Table 178 - Input signals of the *STMP*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
TmpSv	Temperature	From corresponding channel on RTD module

Table 179 - Output signals of the *STMP*

Name	Short label	Infotip
Alm	Alarm	Alarm
Trip	Trip	Trip
Blk	Blocked	Blocked
Tmp	Temperature	Temperature

Setting parameters

Table 180 - Settings of the *STMP*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
TmpLab	Name	Name or Location of RTD			label
TmpFun	Function	Function of RTD	• Other • Winding • Bearing • Ambient		Ambient
AlmSet	Alarm value	Alarm value	-30...200 °C	1 °C	80 °C
TripSet	Trip value	Trip value	-30...200 °C	1 °C	100 °C

NOTE: The default setting for *FunctionSetting* varies by stage.

Characteristics

Table 181 - Characteristics of the *STMP*

Characteristics		Values
Alarm/Trip value	Accuracy	±1°C
	Reset ratio	-2°C ± 1°C
Alarm/Trip outputs	Update interval	< 10 s

Machine unbalance (*NPSPTTR*, ANSI 46)

Description

The machine unbalance protection function is applied to help protect motors or generator rotors from overheating caused by negative sequence currents, which are generated from unbalanced supply such as single phasing. When the negative sequence current exceeds the start value, this function uses either an I^2t curve or a thermal curve to calculate the operate delay, after which the element trips. When the negative sequence current drops below the start value, this function will reset based on the reset characteristic.

NOTE:

- To avoid operation during switching or other transient error currents, a minimum operate delay is introduced for both curves.
- To ensure the thermal level does not exceed the machine's I^2t withstanding rating, a maximum operate delay is introduced for both curves.

Time Constant

The time constant τ is calculated with the following equation:

$$\tau = \frac{MaxThm}{(StrVal \times FLA)^2}$$ E71198

MaxThm is the *Nominal op delay* setting.

FLA is Bay full load amps set in the Bay configuration.

I^2t curve

When *Operating curve* is set to *I^2t*, the motor thermal level and operate delay are calculated as below.

Thermal level

- When the negative sequence current exceeds the start value, the motor thermal level is calculated with the following equation:

$$H(t) = H(t-\Delta t) + \frac{\Delta t}{\left(\frac{MaxThm}{\left(\frac{I_2}{FLA \times StrVal}\right)^2}\right)}$$

E71193

H(t) is the motor thermal level at time t and the output is *Thermal state*;

H(t-Δt) is the motor thermal level at time t-Δt;

Δt is the calculation interval;

MaxThm is the *Nominal op delay* setting;

FLA is Bay full load amps;

I_2 is the negative phase sequence current.

NOTE:

- When $I_2 > I_2max$, I_2max is based on the maximum operate delay.
- When StrVal x FLA < I_2 < I_2min, I_2min is based on the minimum operate delay.

- When the negative phase sequence current is lower than the start value, the motor thermal level is calculated with the following equation:

$$H(t) = H(t-\Delta t) - \frac{\Delta t}{\tau \times RstMul}$$

E71194

RstMul is the *Reset multiplier* setting.

Operate delay

The operate delay is calculated with the following equation:

$$t_{op} = \frac{MaxThm}{\left(\frac{I_2}{FLA \times StrVal}\right)^2} \times (1 - H(t-\Delta t))$$

E71195

t_{op} is the operate delay and the output is *Time to operate*.

Thermal curve

When the *Operating curve* is set to *Thermal*, the motor thermal level and operate delay are calculated as below:

Thermal level

- When the negative sequence current exceeds the start value, the motor thermal level is calculated with the following equation:

$$H(t) = \left(\frac{I_2}{StrVal \times FLA}\right)^2 \times \frac{\Delta t}{\tau + \Delta t} + H(t-\Delta t) \times \frac{\tau}{\tau + \Delta t}$$

E71196

NOTE:

  - When $I_2 > I_2max$, I_2max is based on the maximum operate delay.
  - When StrVal x FLA < I_2 < I_2min, I_2min is based on the minimum operate delay.

- When the negative sequence current is lower than the start value, the motor thermal level is calculated with the following equation:

$$H(t) = \left(\frac{I_2}{StrVal \times FLA}\right)^2 \times \frac{\Delta t}{\tau \times RstMul + \Delta t} + H(t-\Delta t) \times \frac{\tau \times RstMul}{\tau \times RstMul + \Delta t}$$

E71199

Operate delay

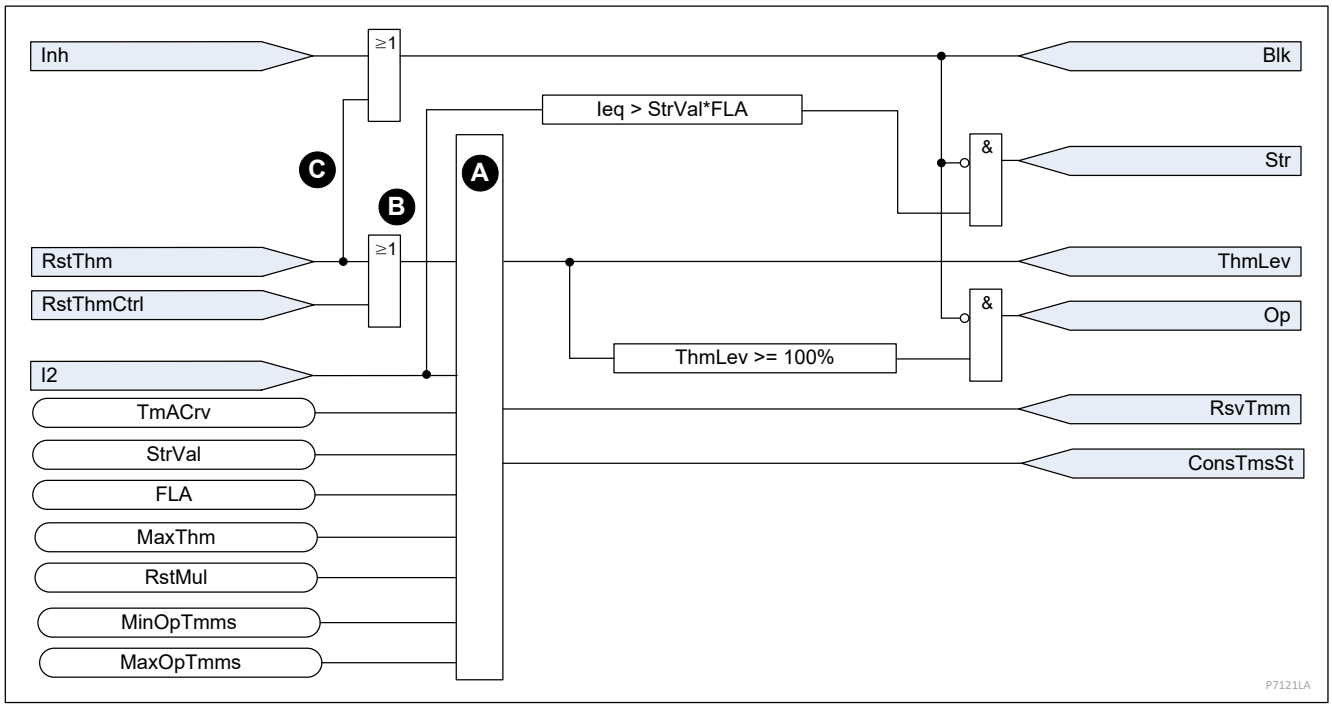
The operate delay is calculated with the following equation:

$$t_{op} = \tau \times \ln\left[\frac{\left(\frac{I_2}{StrVal \times FLA}\right)^2 - H(t-\Delta t)}{\left(\frac{I_2}{StrVal \times FLA}\right)^2 - 1}\right]$$

E71197

Block diagram

Figure 145 - Block diagram of the *NPSPTTR*



A	*Thermal state* calculation	B	Reset thermal state	C	True for more than 1s

Input and output signals

Table 182 - Input signals of the *NPSPTTR*

Name	Short label	Infotip
I2	I2	I2
Inh[general]	Inhibit	Inhibit function
RstThm	Reset	Reset thermal state
RstThmCtrl	Reset thermal state	Reset thermal state

Table 183 - Output signals of the *NPSPTTR*

Name	Short label	Infotip
Str	Start	Start
RsvTmm	Time to operate	Time to operate
Op	Operate	Operate
Blk	Blocked	Blocked
ThmLev	Thermal state	Thermal state
ConsTmsSt	Time constant	Time Constant(s)

Setting parameters

Table 184 - Settings of the *NPSPTTR*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrVal	Start value (xFLA)	The start value is a multiple of the full load current which is defined in bay configuration	0.01...0.5	0.01	0.1
MaxThm	Nominal op delay	This is the operating time delay with I2 FLA. It is used to determine the time constant for thermal mode as Nominal op time/Start value²	1...100 s	0.1 s	15 s
TmACrv	Operating curve	Machine unbalance characteristic. Thermal is asymptotic as it approaches the start value where I²t isn't	• I²t • Thermal		
RstMul	Reset multiplier	Nominal op time/Start value² is multiplied by this value to give the reset time in I²t mode or the reset time constant in Thermal mode	0...10	0.1	1
MinOpTmms	Min op delay	Minimum operating time delay	0...100000 ms	1 ms	250 ms
MaxOpTms	Max op delay	Maximum operating time delay when I2 exceeds the start value	100...10000 s	1 s	1000 s

Characteristics

Table 185 - Characteristics of the *NPSPTTR*

Characteristics		Values
Start value	Accuracy	±2% or ±0.001 pu
	Reset ratio	95% ± 5%
Thermal state	Accuracy	±2%
Operate delay	Accuracy	< 50 ms or ± 2%
Blocked	Block time	<20 ms
	Reset time	<40 ms
Characteristic time	Start time	< 25 ms at 1.2 Is
	Start reset time	< 30 ms at 0.9Is
	Overshoot time	<30 ms for the range between 10 Is and 0.9 Is
	Thermal reset time	<100 ms at 0 Is

Motor monitoring (*ZMOT*)

Description

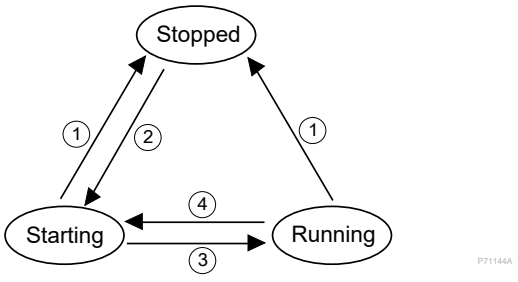
The motor monitoring function is available in the PowerLogic P7.

Motor state

There are three states for a motor: *Stopped*, *Starting* or *Running*.

The PowerLogic P7 motor state is based on the *Bay dead* signal and the phase currents.

Figure 146 - Motor state



Criterion for motor in Stopped state

Motor is in *Stopped* state when the *Bay dead* signal is detected. ①

Criterion for motor in Starting state

- Motor will change to the *Starting* state when motor is in *Stopped* state and the *Bay dead* input changes from active to inactive. ②

  NOTE: The maximum current during *Starting* is recorded as *Start current*. The recording omits the first second of the *Starting* process to avoid inrush.

  If any of the three phase currents exceed the start current setting, motor remains in the Starting state.

- Motor will change to the *Starting* and *Reacceleration* state, when motor is in *Running* state and the following conditions are met sequentially: ④
  1. Reacceleration detection function is enabled.
  2. Any of the phase-to-phase voltages drop below *ReAccVVal* for over 100 ms and then rise above *ReStoVVal*.
  3. Any of the three phase currents exceed the start current setting within 5 s.

  or,

  1. Reacceleration detection function is enabled.
  2. *ReacAuth* input is asserted.
  3. Any of the three phase currents exceed the start current setting.

Criterion for motor in Running state

When motor is in *Starting* state, motor will change to the *Running* state if the following conditions are met simultaneously: ③

- *Bay dead* input is inactive.
- All three phase currents are less than 95% of the start current setting for more than 1 s.

  NOTE: The time elapsed when changing from *Starting* to *Running* is recorded as *Start time*.

Counters and alarms

Each start and reacceleration is counted. The counters can be reset individually. If the number of starts counter value reaches the set threshold, an alarm is issued.

When motor is in *Running* or *Starting* state, the running hours is accumulated. The running hours can be reset. Two running hours alarms will be asserted when corresponding alarm is enabled and time exceeds its threshold setting.

Block diagram

Figure 147 - Block diagram of the *ZMOT Stopped* state

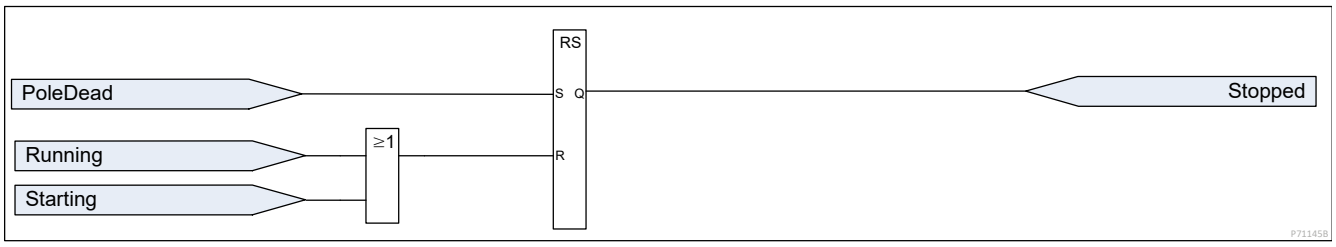


Figure 148 - Block diagram of the *ZMOT Starting* state

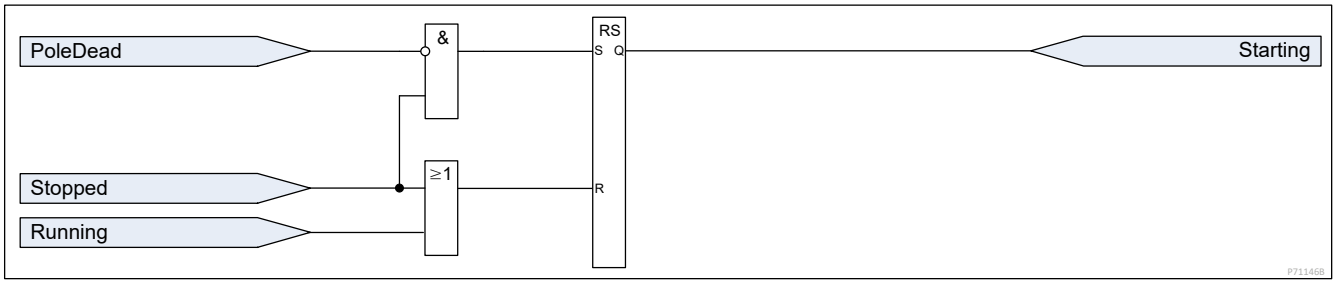


Figure 149 - Block diagram of the *ZMOT Reacceleration* state

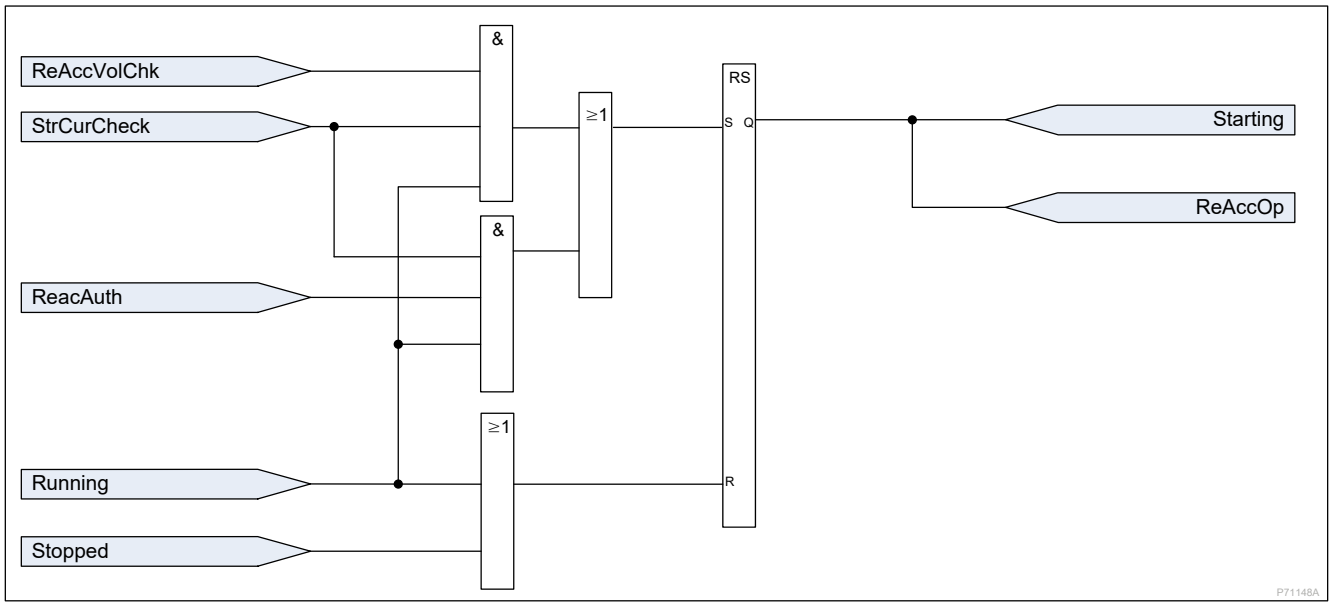
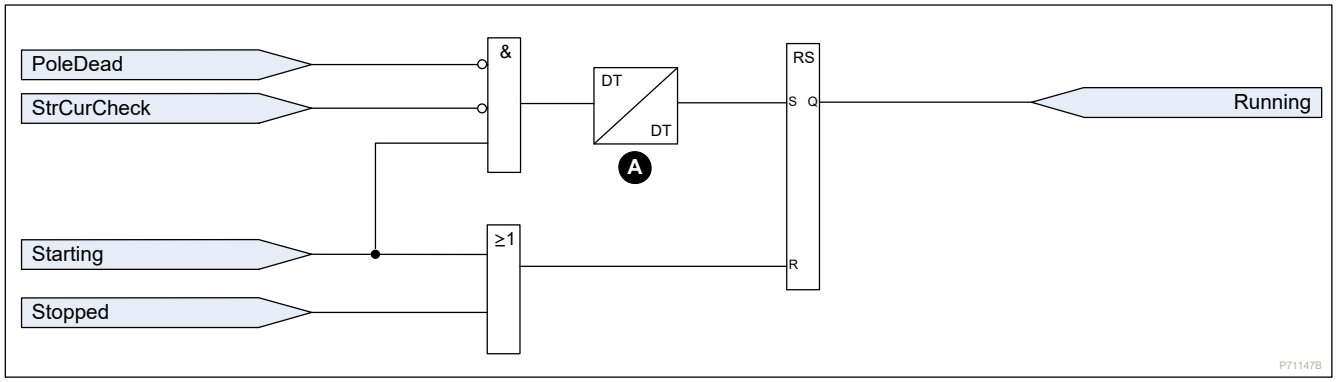


Figure 150 - Block diagram of the *ZMOT Running* state



A Operate delay: 1 s
Reset delay: 0 ms

Input and output signals

Table 186 - Input signals of the *ZMOT*

Name	Short label	Infotip
IAIBIC	Phase current	Phase current
UABUBCUCA	Line voltage	Line voltage
PoleDead	Bay dead	Internal signal from PDGAPC1
ReacAuth	Restart	Restart (reacceleration) initiation

Table 187 - Output signals of the *ZMOT*

Name	Short label	Infotip
MotSt	Motor Status	Motor Status
HrRunCntRs	Hours running	Hours running
HrRunAlm1	Hour run alarm 1	Hour run alarm 1
HrRunAlm2	Hour run alarm 2	Hour run alarm 2

Table 187 - Output signals of the *ZMOT* (Continued)

Name	Short label	Infotip
OpCntStrRs	Start count	Start count
NbStrAlm	Start number alarm	Start number alarm
ReAccOp	Reacceleration active	Reacceleration active
ReAccOpCntRs	Reacceleration count	Reacceleration count
StrCurrent	Start current	Start current
StrTime	Start time	Start time

Setting parameters

Table 188 - Settings of the *ZMOT*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		On
StrCurVal	Start value (xFLA)	Current used to determine motor status. It is a multiple of the full load current which is defined in bay configuration	0.01...40	0.001	3
HrRAlm1Val	Hours run alarm 1 value	Hours run alarm 1 value	0...9999 hr	1 hr	0 hr
HrRAlm2Val	Hours run alarm 2 value	Hours run alarm 2 value	0...9999 hr	1 hr	0 hr
NbStrAlmVal	Start number alarm value	Start number alarm value	0...999	1	0
ReAccTmSt	Reacceleration status	Reacceleration will allow the motor to go from running state to starting state during voltage dips. This avoids locked rotor operation	• Off • On		Off
ReAccVVal	Reacceleration voltage	This is the voltage level to initiate reacceleration. The voltage must be below this level for 100ms	0.01...1	0.01	0.7
ReStoVVal	Restoration voltage	If reacceleration voltage is detected the motor status will go to starting if this voltage is exceeded and current above the start level occurs in the next 5 seconds	0.01...1	0.01	0.9

Characteristics

Table 189 - Characteristics of the *ZMOT*

Characteristics		Values
Start value (xFLA)	Accuracy	±2%
	Reset ratio	95% ± 2%
Voltage settings	Accuracy	±2%
Operate delay	Accuracy	±2% or ±20 ms

Motor start supervision (*PMSS*, ANSI 48)

Description

The motor start supervision protection function includes two parts:

1. Excessive starting time

   After a motor start is detected, before starting supervision time expires, if current successfully falls below the starting current threshold[12], it means the motor start successfully, otherwise the *operate* signal will be issued after starting time delay.

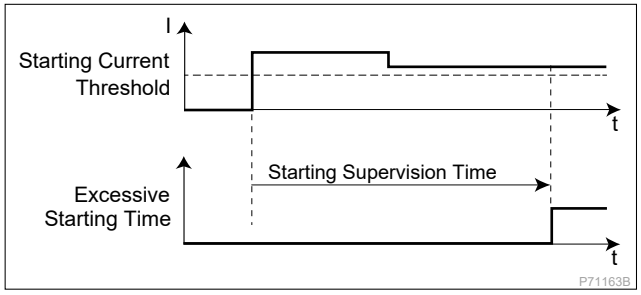
   The excessive starting time delay uses DT or IDMT timer based on the prolonged start mode setting. The IDMT operation curve is as follows:

$$t = \frac{SetTms}{\left(\frac{G}{SetA}\right)^2}$$

E71118A

   G is the fundamental current amplitude.

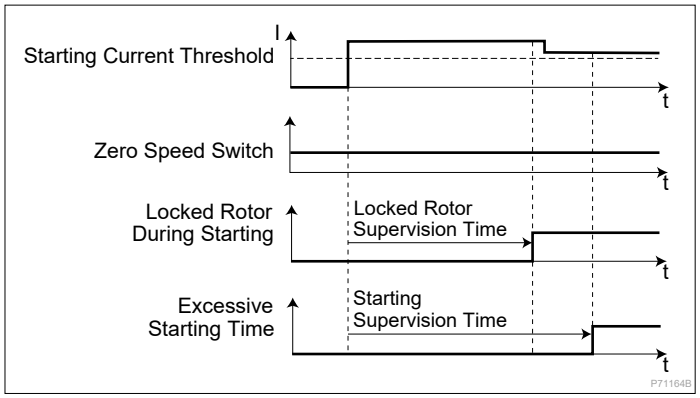
Figure 151 - Excessive starting time



2. Locked rotor during starting

   For certain applications, the stall withstand time is less than the starting time. A *Zero speed* input is used to indicate the machine is starting and not stalled. If the current exceeds the starting current threshold[12] and the speed of the motor is equal to zero (zero speed switch input is active), the *Operate* signal will be issued after the stall time.

Figure 152 - Locked rotor during starting

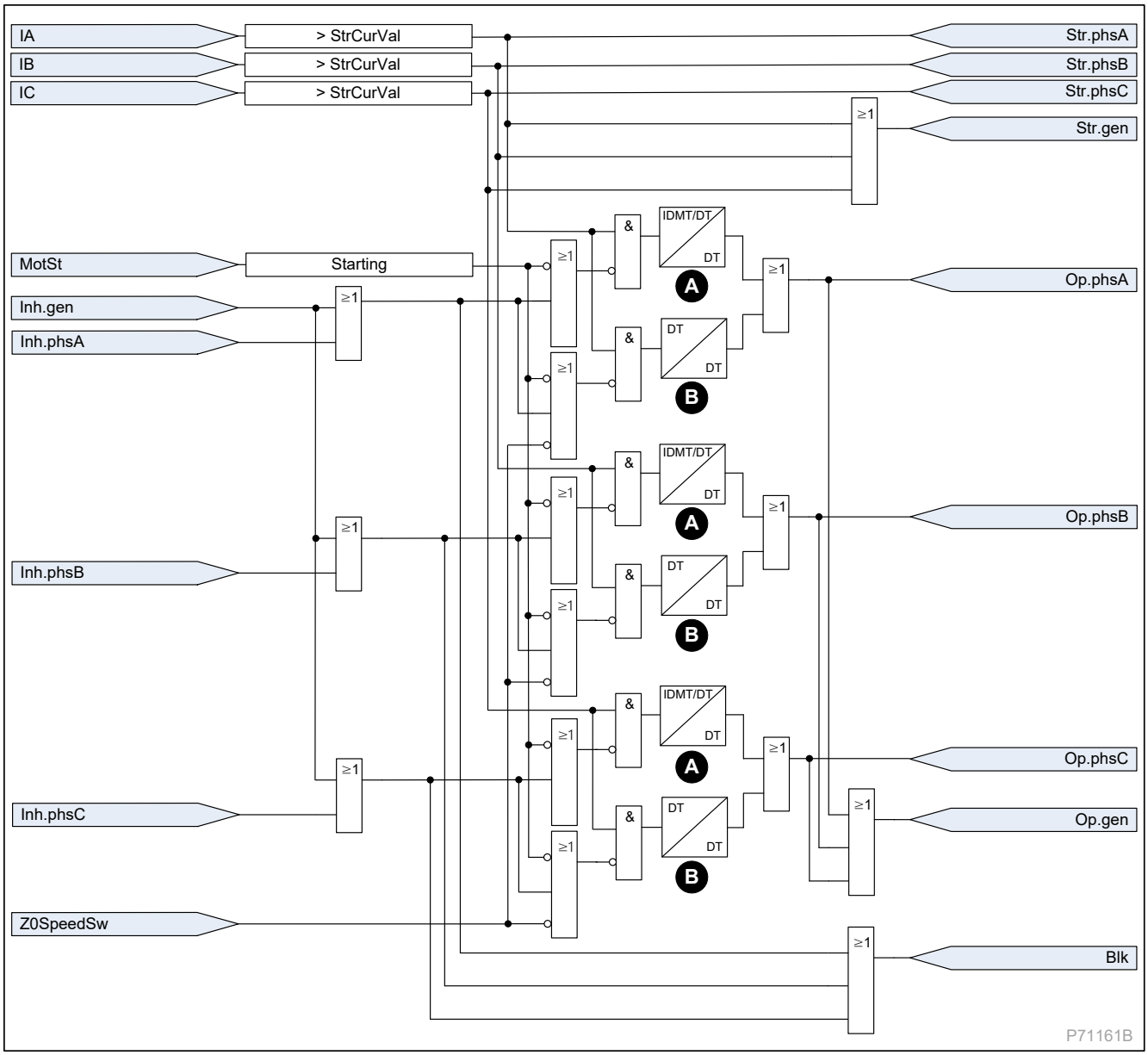


The *Start* output signal will be issued if one of the three-phase current exceeds the starting current threshold[12] and no inhibit signal is generated.

12. The starting current threshold is the same as the starting current detection threshold from the *ZMOT*.

Block diagram

Figure 153 - Block diagram of the *PMSS*



A	DT Operate delay: *LokRotTms* IDMT Operate delay: *SetA*, *SetTms* Reset delay: 0 ms	B	Operate delay: *LokRotTms* Reset delay: 0 ms

Input and output signals

Table 190 - Input signals of the *PMSS*

Name	Short label	Infotip
Inh[general;phsA;phsB;phsC]	Inhibit	Inhibit function
Z0SpeedSw	Zero speed	When active locked rotor time applies
IAIBIC	Phase current	Phase current
MotSt	Motor status	Internal signal from ZMOT1

Zero speed switch input comes from the matrix and it will be asserted by either one of the following signals:

- The output signal of zero speed function.
- The Binary Input (BI) from the external switch.

NOTE: If neither of the signals are mapped to Zero speed switch input, the default value of *Z0SpeedSw* will be inactive.

Table 191 - Output signals of the *PMSS*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
Blk	Blocked	Blocked

Setting parameters

Table 192 - Setting parameters of the *PMSS*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	The element will only operate when the motor status is starting	• On • Off		Off
PSMod	Operating curve	An inverse curve can be used to provide longer start times at reduced voltage	• Definite Time • Inverse		
SetA	Nom voltage start current (xFLA)	In inverse mode the operate time equals the Nominal voltage start time at this multiple of full load current which is defined in bay configuration	0.005...40 pu	0.001 pu	6 pu
SetTms	Nom voltage start time	In inverse mode this is the operating time at start current. In definite time mode this is the operating time for all currents	0...10000000 ms	1 ms	5000 ms
LokRotTms	Locked rotor delay	This is the operating time delay when zero speed input is active	0...10000000 ms	1 ms	2000 ms

Characteristics

Table 193 - Characteristics of the *PMSS*

Characteristics		Values
Operate delay	DT accuracy	±2% or ±10 ms
	IDMT accuracy	±5% or ±20 ms
Characteristic time	Start time	< 25 ms at 2 Is
	Disengaging time	< 30 ms
	Overshoot time	< 30 ms (10...0.9 Is)

Locked rotor (*JAMPTOC*, ANSI 51LR)

Description

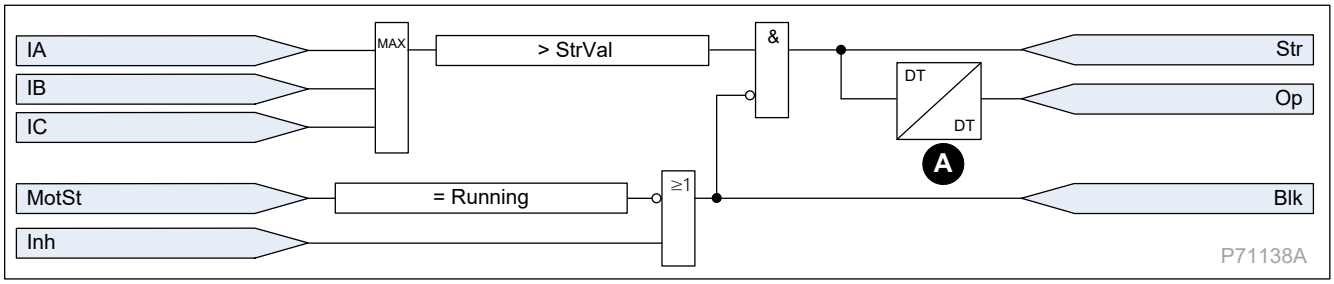
Locked rotor protection function is used for motors. If a machine load becomes jammed when running, it will cause start-up current to flow. As the machine is not

spinning, there is reduced windage, so the rotor rapidly overheats. The protection will operate more quickly than the thermal element which allows a shorter time to restart once the jam is cleared.

Following a successful start, if the current exceeds the stalling current threshold and fails to fall below the threshold before the stall time delay elapsed, then the operate signal is issued. The element will not operate when the motor is starting and is protected by separate start protection. Reacceleration can be applied in the motor monitor function to help prevent operation on voltage drops.

Block diagram

Figure 154 - Block diagram of the *JAMPTOC*



A Operate delay: *OpDITmms*
Reset delay: 0 ms

Input and output signals

Table 194 - Input signals of the *JAMPTOC*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
MotSt	Motor status	Internal signal from ZMOT1
IAIBIC	Phase current	Phase current

NOTE: For the three-phase inputs, two-phase mode indicates only IA and IC are active.

Table 195 - Output signals of the *JAMPTOC*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
Blk	Blocked	Blocked

Setting parameters

Table 196 - Settings of the *JAMPTOC*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrVal	Start value	Element will start if current is above this level when the motor is running	0.005...40 pu	0.001 pu	3 pu
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	2000 ms

Characteristics

Table 197 - Characteristics of the *JAMPTOC*

Characteristics		Values
Start value	Accuracy	±2% or ±0.001 pu
	Reset ratio	95% ± 5%
Operate delay	DT accuracy	±2% or ±10 ms
Reset time	DT accuracy	< 30 ms
Characteristic time	Start time	< 25 ms at 2 Is
	Overshoot time	< 30 ms

Motor restart inhibition and emergency restart (*PMRI*, ANSI 66)

The motor restart inhibition includes three functions: starts inhibition, time between starts and anti-backspin.

The emergency restart effectively removes restart inhibition from thermal overload, starts inhibition and time between starts inhibition.

Number of starts limitation

Starts inhibition

Any motor has a restriction on the number of starts within a defined period to avoid overheating of the motor, mainly inside the rotor.

The maximum allowable number of starts per period is an auto-reset inhibit function which monitors the number of motor starts in the set period *MaxStrTmm*. At the end of the supervising period the number of starts is reset.

When the maximum number of starts *MaxNumStr* within the defined period has been reached, therefore, the starts number inhibition signal *StrNumInh* is initiated. The starts number inhibition signal will be present until the end of the *InhTmm* or as long as the counter of the number of starts is above the maximum allowed starts.

Figure 155 - Example of remaining supervising time < *InhTmm*

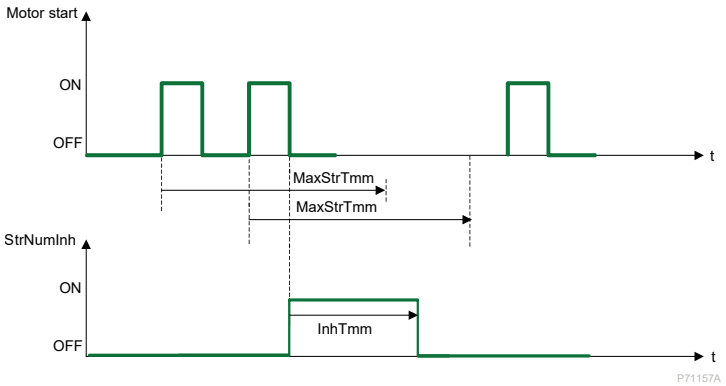
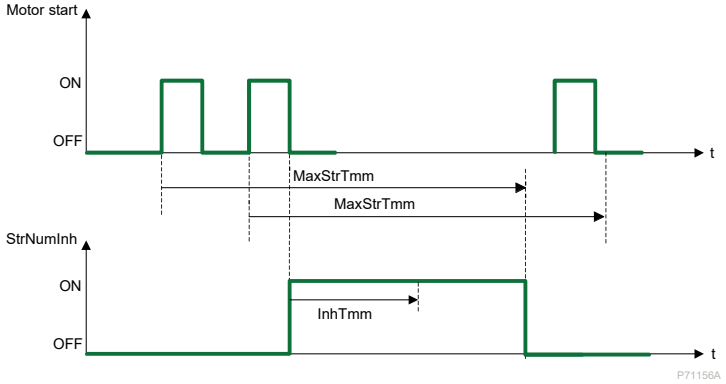


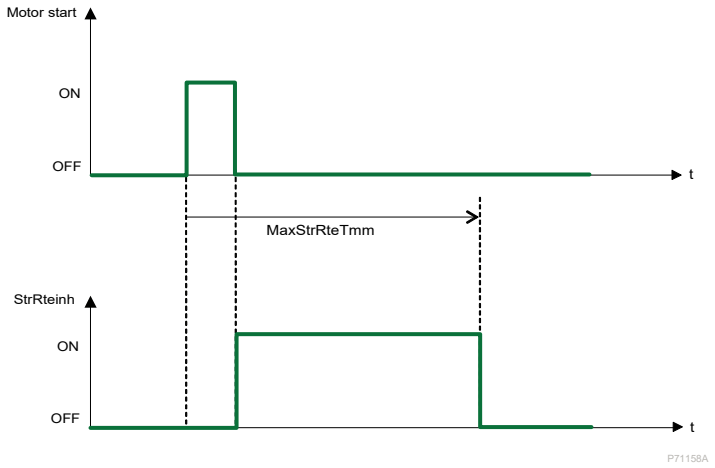
Figure 156 - Example of remaining supervising time > *InhTmm*



Time between starts

Once a motor start is detected, the PowerLogic P7 initiates the minimum time between starts setting *MaxStrRteTmm*. When the motor is stopped and the monitor timer of the last motor start has not expired, the start rate inhibition signal *StrRteInh* will be present until end of the *MaxStrRteTmm*.

Figure 157 - Time between starts

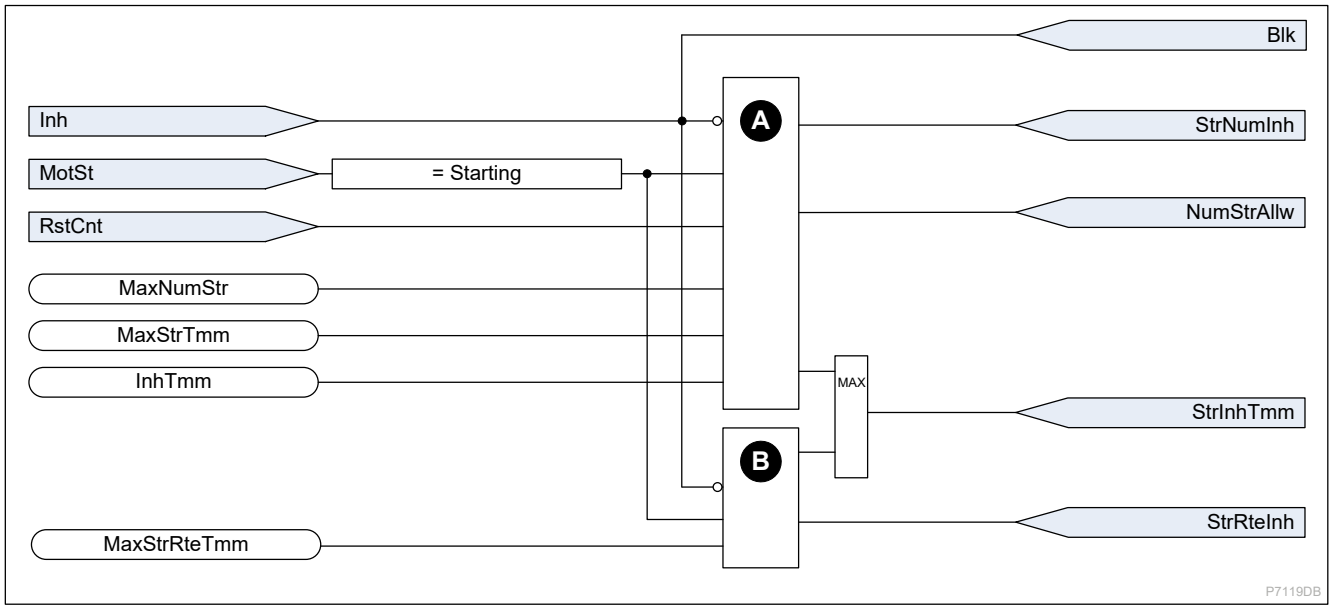


Block diagram of number of starts limitation

The block diagram of the number of starts limitation function is shown as follows. The allowed start number is recorded and the start number can be reset.

The inhibition time *StrInhTmm* is the maximum value of starts number inhibition time and start rate inhibition time.

Figure 158 - Block diagram of the number of starts limitation



A	Starts inhibition logic	B	Time between starts logic

NOTE: When *MaxNumStr* is *0*, the starts inhibition logic is disabled; when *MaxStrRteTmm* is *0*, the time between starts logic is disabled.

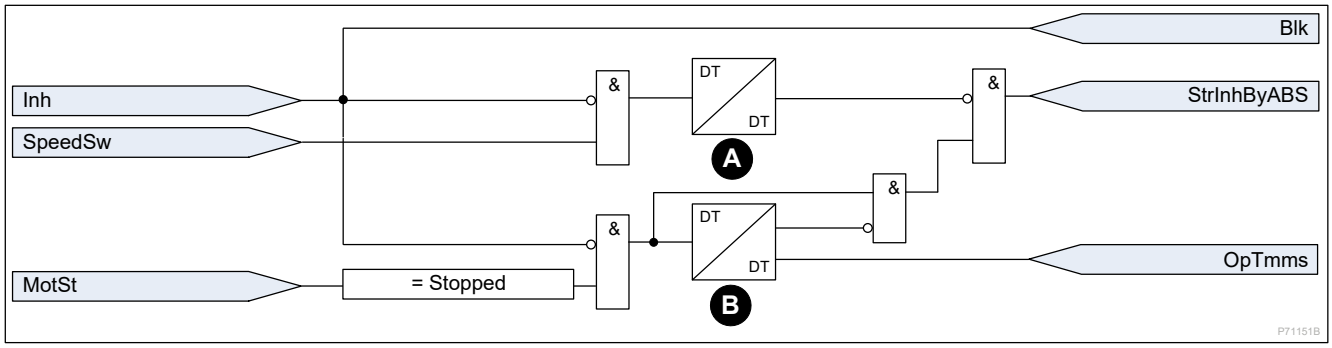
Anti-backspin

The anti-backspin function is used in applications where the motor may spin backwards after stopping due to the load such as inclined conveyors. If a start is attempted the motor will draw excess current for an extended time which will likely lead to an unsuccessful start. The function is used to detect when the rotor has completely stopped, in order to allow restarting of the motor.

The anti-backspin protection is initiated by motor *Stopped* status from motor monitor function. The restart inhibit signal is issued when the motor is stopped and is present until the anti-backspin timer *AbsTmms* expires. Zero speed switch input is used to reset restart inhibit signal after the time delay *ZerSpdTmms*.

The remaining time is based on the anti-backspin timer to indicate the left time before the motor restart is allowed.

Figure 159 - Block diagram of the anti-backspin



A	Operate delay: *ZerSpdTmms* Reset delay: 0 ms	B	Operate delay: *AbsTmms* Reset delay: 0 ms

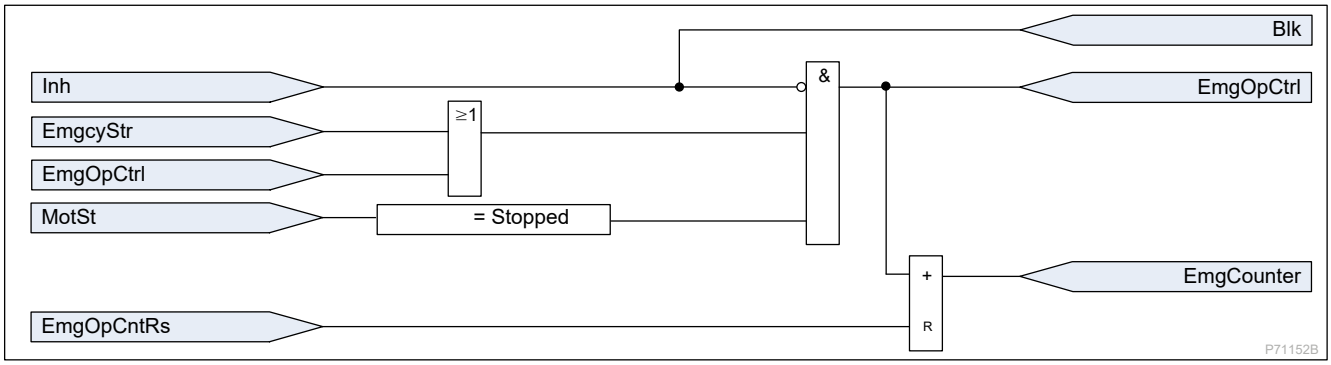
Emergency restart

Where a motor forms part of an essential process, it is sometimes desirable for it to continue operation, even under severe overload conditions. This usually means the motor being subjected to temperatures in excess of its design limits. Even though this may decrease the life of the motor or burn the motor out, such conditions may be justified in an emergency.

The emergency restart signal is issued when the motor is in Stopped status and an emergency restart input is active. The emergency restart input can be enabled through a binary input, HMI or via the remote communications.

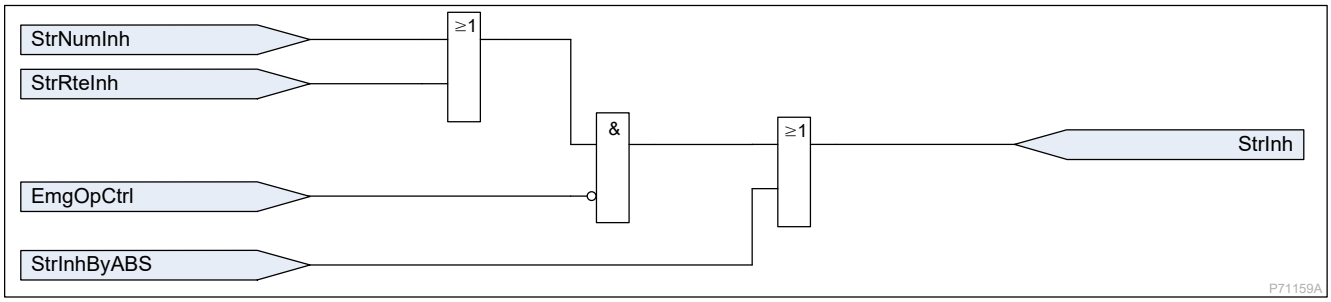
An operation counter is provided to record the number of emergency restarts.

Figure 160 - Block diagram of the emergency restart



The emergency restart effectively removes the start inhibits from thermal overload, starts inhibition and time between starts functions. The emergency restart limits the thermal level under 90% to enable the user to start the motor immediately. The anti-backspin inhibition cannot be reset by emergency restart. The general restart inhibition signal is issued.

Figure 161 - Block diagram of the motor restart inhibition and emergency restart logic



Input and output signals

Table 198 - Input signals of the *PMRI*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
MotSt	Motor status	Motor status
RstStrNum	Reset	Reset allowed start number
SpeedSw	Zero speed	If this input is high for Zero speed time the ABS is released
EmgcyStr	Em restart	Emergency restart - resets number of starts and time between starts. It also sets the emergency restart output which can be used to limit thermal. The output resets when the motor is running

Table 198 - Input signals of the *PMRI* (Continued)

Name	Short label	Infotip
StrNumCtrl	Reset	Reset allowed start number
EmgOpCtrl	Emergency restart	Emergency restart
EmgOpCntRs	Emergency restarts count	Emergency restarts count

Table 199 - Output signals of the *PMRI*

Name	Short label	Infotip
NumStrAllw	Allowed starts remaining	Allowed starts remaining
StrNumInh	Number of starts inhibit	Number of starts inhibit
StrRteInh	Time between starts inhibit	Time between starts inhibit
StrInhbyABS	Anti backspin inhibit	Anti backspin inhibit
StrInh	Start inhibited	Start inhibited
StrInhTmm	Inhibition time (mins)	Inhibition time (mins)
OpTmms	ABS time remaining	ABS time remaining
EmgOpCtrl	Emergency restart	Emergency restart
EmgOpCntRs	Emergency restarts count	Emergency restarts count
Blk	Blocked	Blocked

Setting parameters

Table 200 - Settings of the *PMRI*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
MaxStrTmm	Start number period	The number of starts is normally given in starts per hour	0...120 min	1 min	60 min
MaxNumStr	Start number in period	The number of starts allowed in the start period. Typically 2 or 3 starts per hour	1...10	1	1
InhTmm	Start number min inhibition time	If the number of starts is exceeded, starting is blocked for the minimum of this setting and the remaining time in the start period	0...120 min	1 min	10 min
MaxStrRteTmm	Time between starts	Time between starts	0...120 min	1 min	2 min
AbsTmms	Anti backspin time	This is the time to wait to ensure the motor is not being run backwards by the load	1...10000000 ms	1 ms	300 ms
ZerSpdTmms	Zero speed time	Zero speed needs to be active for this time to allow a restart	1...10000000 ms	1 ms	300 ms

Characteristics

Table 201 - Characteristics of the *PMRI*

Characteristics		Values
Operate delay	Accuracy	±5% or ±50 ms
Characteristic time	Start inhibition	< 20 ms

Voltage check (*VCPTUV*, ANSI 47)

Description

The voltage check function is normally used in motor applications to help ensure the machine has the correct voltage before attempting to start. The voltage should come from a busbar VT for this function to operate. The PowerLogic P7 monitors the input voltage rotation and magnitude to determine both correct phase rotation and sufficient supply voltage, prior to permitting motor starting.

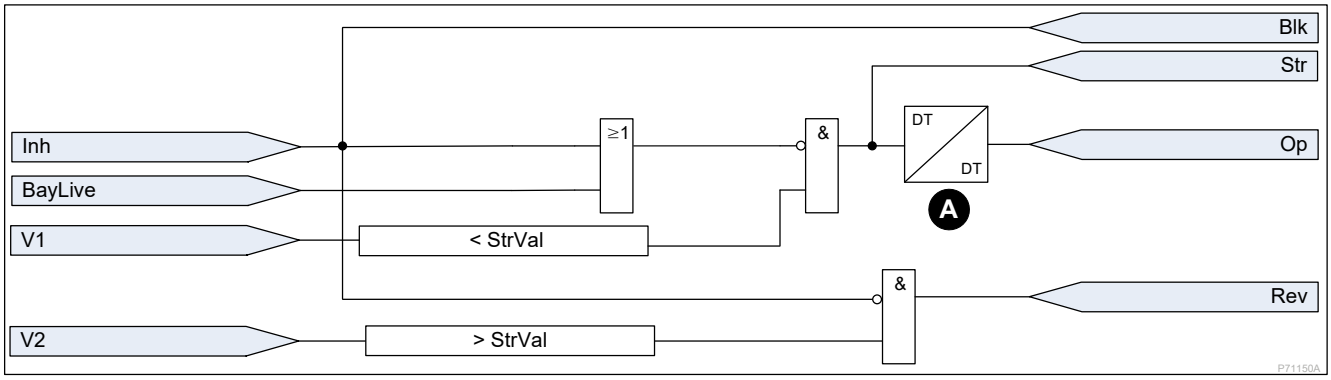
For a good starting condition, the positive sequence voltage (V1) should be more than the set threshold. If V1 drops under the threshold, start and operate signals are generated and can be linked to *CBCILO* or *CBCSWI* via Matrix to inhibit CB closing and block motor start.

If the negative sequence voltage (V2) is more than the threshold, the voltage is considered to be reverse phase. A reverse indication signal is generated and can be used to block motor start via matrix if reverse rotation is not allowed.

This function is normally linked to the CB control to inhibit closing and can be inhibited when the bay is live.

Block diagram

Figure 162 - Block diagram of the *VCPTUV*



A Operate delay: *OpDITmms*
Reset delay: 0 ms

Input and output signals

Table 202 - Input signals of the *VCPTUV*

Name	Short label	Infotip
V1	V1	V1
V2	V2	Linked to V1 input source
Inh[general]	Inhibit	Inhibit function
BayLive[general]	Bay live	Signal to indicate the bay is live. This will inhibit operation

Table 203 - Output signals of the *VCPTUV*

Name	Short label	Infotip
Str	Start	Start
Rv	Reverse rotation	Reverse rotation

Table 203 - Output signals of the *VCPTUV* (Continued)

Name	Short label	Infotip
Op	Operate	Operate
Blk	Blocked	Blocked

Setting parameters

Table 204 - Settings of the *VCPTUV*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Checks V1 is adequate for starting. A reverse indication is given if V2 is above the start value	• On • Off		Off
StrVal	Start value	Minimum positive sequence voltage for starting	0.1...2 pu	0.01 pu	0.8 pu
OpDlTmms	Operate delay	Operate time delay	0...100000 ms	1 ms	0 ms

Characteristics

Table 205 - Characteristics of the *VCPTUV*

Characteristics		Values
Start value	Accuracy	±2% or ±0.001 pu
	Reset ratio	±102% (with accuracy ±2%)
Operate delay	DT timer – Accuracy	±2% or ±10 ms
Characteristic time	Start time	< 25 ms

Table 206 - Characteristics of the reverse phase rotation

Characteristics		Values
Start value	Accuracy	±5% or ±0.01 pu
	Reset ratio	90% (with accuracy ±10%)
Characteristic time	Start time	< 50 ms

Third harmonic undervoltage (*STPTUV*, ANSI 27TN)

Description

Neutral displacement protection measures the fundamental frequency voltage component at the generator star point, and it operates when the fundamental frequency voltage exceeds the preset value. By applying this principle, approximately 95% of the stator winding can be protected. In order to help protect the last 5% of the stator winding, close to the neutral end, third harmonic voltage measurement can be performed. In *STPTUV* protection, either the neutral point third harmonic undervoltage principle, or differential principle based on the magnitude ratio of the neutral point third harmonic voltage to the third harmonic differential voltage can be applied. However, differential principle is strongly recommended. Combined with neutral displacement it provides coverage for entire stator winding against ground faults.

If the terminal VT is wye-grounded, a third-harmonic measurement at the terminal (*V3T*) is available. In this case, both *V3T* and the neutral third harmonic (*V3N*) measured across a neutral grounding transformer are used.

If the terminal VT is wye ungrounded (*V3T* unavailable), the third harmonic neutral undervoltage element which uses *V3N* is applied.

Operation equation of protection

The third harmonic undervoltage differential protection compares geometrically the third harmonic voltages measured at both neutral (N) and terminal (T) side of the generator. The algorithm of the third harmonic voltage differential protection is as follows. The operating equation of the protection is:

Equation 1: Differential mode	*V3N* / *V3HDiff* < *V3HRatio*
Equation 2: Undervoltage mode	*V3N* < *V3NStrVal*

Where:

V3HDiff = |*V3T* - *V3N*| = |*V3G*| is the magnitude of total third harmonic voltage generated by stator.

V3N and *V3T* are third harmonic phasors with real and imaginary parts.

Equation 1 defines the operate regions of the protection. The third harmonic differential undervoltage protection operates, and after delay *OpDlTmms* trips the faulty generator.

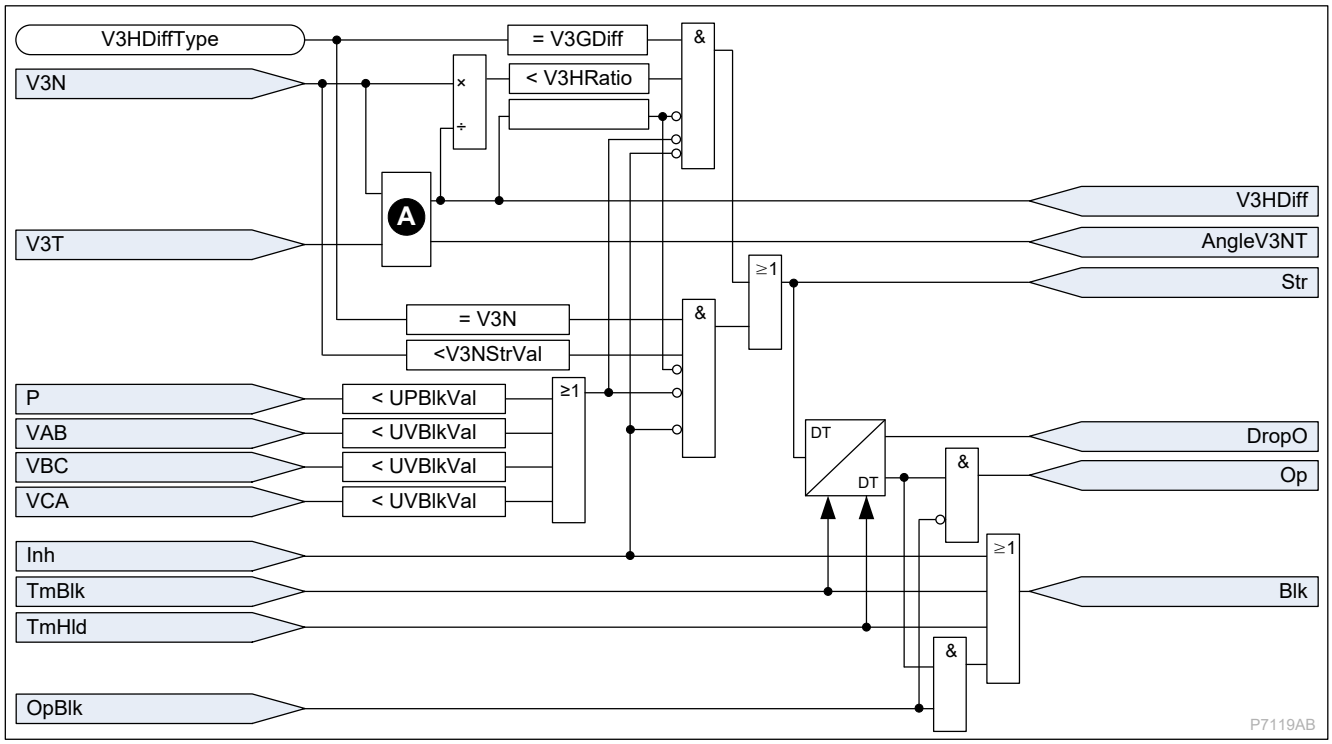
When the fault position is closer to neutral point, |*V3N*| will decrease, when fault position is closer to terminal point, |*V3N*| will increase. As both the differential and undervoltage elements look for reduced voltage at the neutral end they only work for faults near the neutral point. This complements neutral displacement protection which can detect faults in the remainder of the winding.

The advantage of the third harmonic undervoltage differential protection is that this algorithm offers a protection which is independent of the changing load on the protected generator.

Whenever the generator is running, there will be a certain amount of third harmonics present. *V3HBlkVal* should be set below this value to ensure the element is only operational when the machine is running.

Block diagram

Figure 163 - Block diagram of the *STPTUV*



A Calculating V3HDiff by |V3N – V3T| and angle of V3N to V3T.

Input and output signals

Table 207 - Input signals of the *STPTUV*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
TmBlk	Block	Block (reset) timers
TmHld	Hold	Hold timers
OpBlk	Op block	Output blocked when active (timers not held)
VABVBCVCA	Line voltage	Line voltage
V3T	Terminal VN	Linked to line voltage input source
V3TCplx	Terminal complex VN	Linked to line voltage input source
V3N	Star point VN	Star point VN
V3NCplx	Neutral complex VN	Linked to star point VN input source
P	Total power	Internal signal from PWRGAPC1

Table 208 - Output signals of the *STPTUV*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO	Drop off	Drop off
Blk	Blocked	Blocked

Table 208 - Output signals of the *STPTUV* (Continued)

Name	Short label	Infotip
V3HDiff	H3 diff voltage	H3 diff voltage
AngleV3NT	Term-neut H3 angle	Term-neut H3 angle

Setting parameters

Table 209 - Settings of the *STPTUV*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
V3HDiffType	Operation mode	Choose differential or neutral undervoltage mode	• Diff under ratio • Neutral undervoltage		Neutral under-voltage
V3HRatio	Diff ratio start value	Operation when V3N is less than this setting multiplied by the total third harmonic voltage (V3T-V3N)	0.001...1	0.001	0.1
V3NStrVal	Neutral UV start value	Operation when V3N is less than this setting	0.001...1.25 pu	0.001 pu	0.01 pu
V3HBlkVal	H3 diff block value	Operation blocked if the total third harmonic voltage (V3T-V3N) is less than this value. Set to zero to disable this check	0...1.25 pu	0.001 pu	0.01 pu
UVBlkVal	Undervoltage block value	Operation blocked when V3T is below this value. Set to zero to disable this check	0...1.25 pu	0.001 pu	0.8 pu
UPBlkVal	Underpower block value	Operation blocked when bay power is below this value. Set to zero to disable this check	0...1.25 pu	0.001 pu	0.03 pu
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	0 ms
RsDlTmms	Reset delay	Reset time delay	0...10000000 ms	1 ms	0 ms

Characteristics

Table 210 - Characteristics of the *STPTUV*

Characteristics		Values
Neutral UV start value	Accuracy	±2% or ± 0.001 pu
	Reset ratio	102% ± 2%
H3 diff block value	Accuracy	±2% or ± 0.001 pu
	Reset ratio	102% ± 2%
H3 diff voltage	Accuracy	±2% or ± 0.001 pu
Operate delay	DT accuracy	±2% or ±10 ms

Inter-turn protection based on split phase (*ITPDIF*, ANSI 87G)

Description

Introduction of generator inter-turn protection of split phase

For generators with multi-turn stator windings, there is the possibility of a winding inter-turn fault occurring. Unless such a fault evolves to become a stator ground fault, it will not otherwise be detected with conventional protection arrangements. Hydro generators usually involve multi-stator windings with parallel windings.

Generator differential inter-turn protection

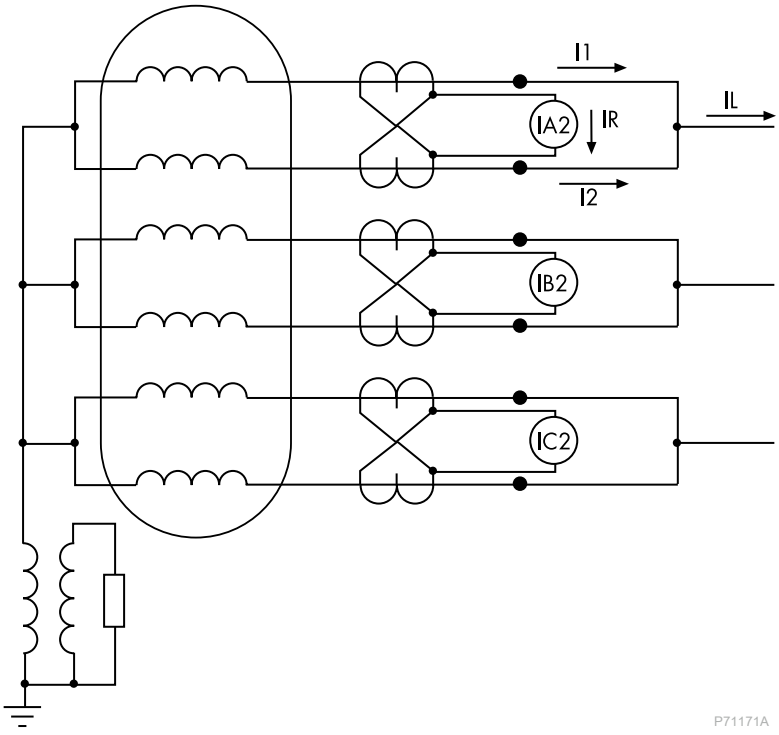
One differential scheme using bushing type CTs that is commonly used for inter-turn protection is shown in Generator inter-turn protection using separate CTs, page 309. In this scheme the circuits in each phase of the stator winding are split into two equal groups and the current of each group are compared. A difference in these currents indicates an unbalance caused by an inter-turn fault. Since there is normally some current unbalance between windings, the protection is set so that it will not respond to this normal unbalance but will pick-up for the unbalance caused by a single turn fault.

In some cases, the generator may run with a faulted turn until it is repaired and therefore the current pick-up level should be increased to allow operation but still be able to detect a second fault. The second group current inputs IA2/IB2/IC2 can be used for this type of application and has independent settings per phase.

Therefore the current setting can be increased on the faulted phase only without affecting the sensitivity of the protection on the other unfaulted phases. A time delay is used to prevent operation on CT transient error currents that may occur during external faults.

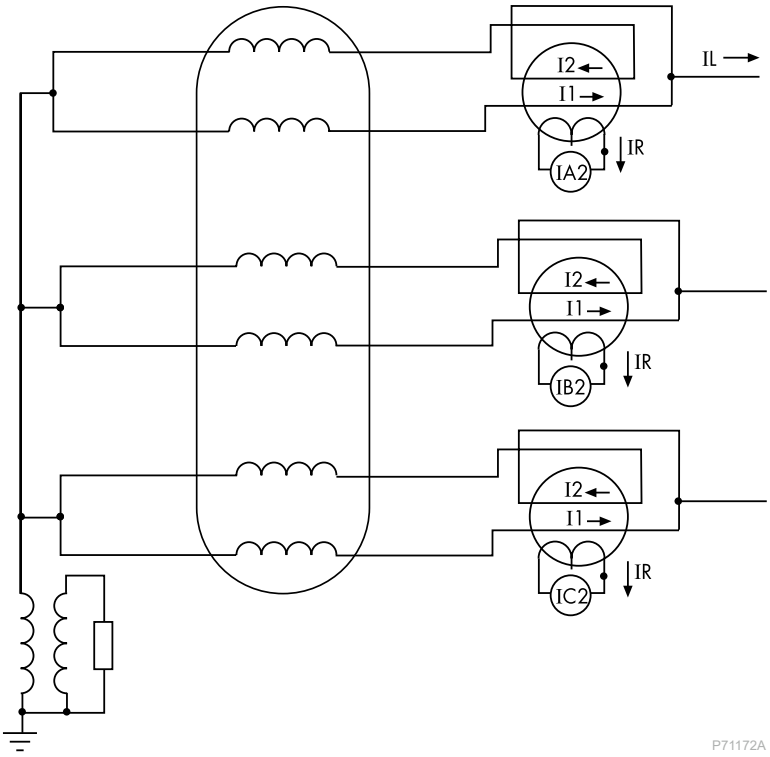
The current inputs IA2/IB2/IC2 could not be used for other protections anymore.

Figure 164 - Generator inter-turn protection using separate CTs



The problem of CT transient error currents can be eliminated by using core balance (window) type CTs as below in Generator inter-turn protection using separate CTs, page 310.

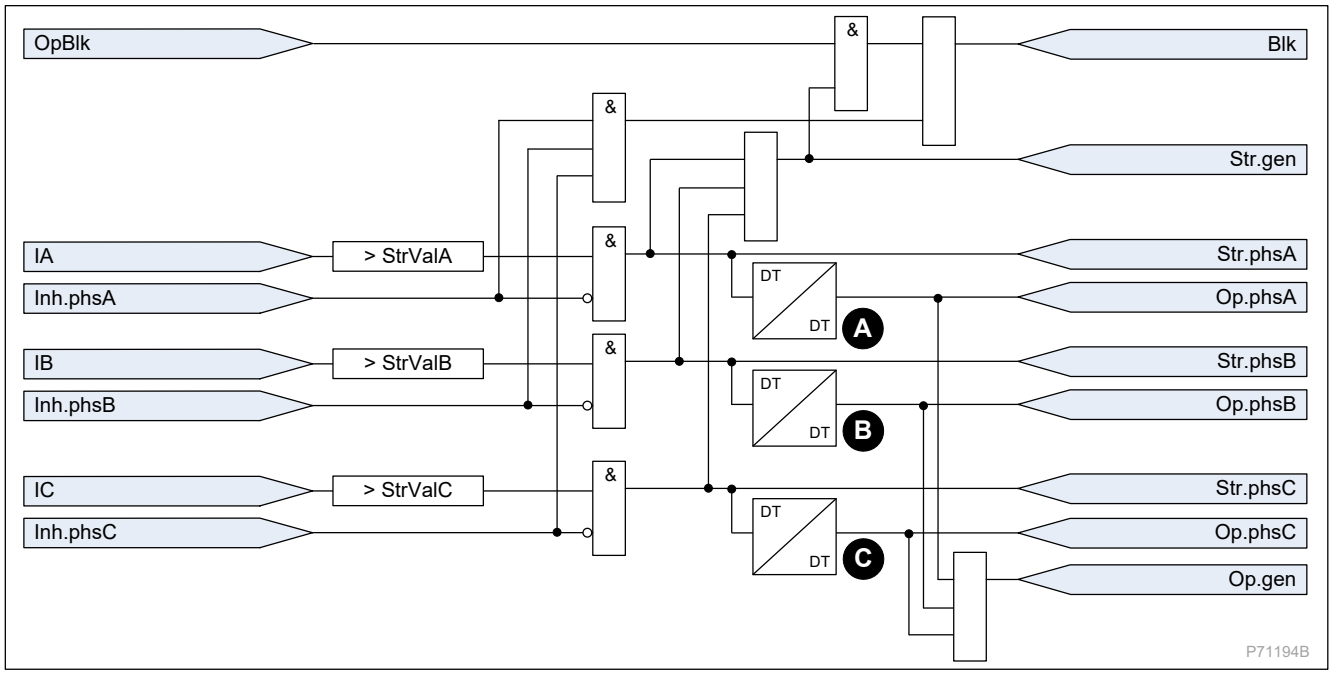
Figure 165 - Generator inter-turn protection using separate CTs



This method of inter-turn protection will detect phase and some ground faults in the stator winding. However, because of the slow operating time of this protection, it is common practice to provide standard high speed differential protection for each phase and separate ground fault protection. If there are main 1 and main 2 protection devices, the IA2/IB2/IC2 inputs could be used for inter-turn protection on the one device and used for standard differential protection across the generator in the other device. The *HIZPDIF* element can be used for this application without a series resistor.

Block diagram

Figure 166 - Block diagram of the *ITPDIF*



A, B, C Operate delay: *OpDITmms*
Reset delay: 0 ms

Input and output signals

Table 211 - Input signals of the *ITPDIF*

Name	Short label	Infotip
Inh[general;phsA;phsB;phsC]	Inhibit	Inhibit function
OpBlk	Op block	Output blocked when active (timers not held)
IAIBIC	Phase current	Phase current

Table 212 - Output signals of the *ITPDIF*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
Blk	Blocked	Blocked

Setting parameters

Table 213 - Settings of the *ITPDIF*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrValA	Aph start value	All start values are usually the same unless a winding is intentionally shorted	0.005...40 pu	0.001 pu	1 pu

Table 213 - Settings of the *ITPDIF* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
StrValB	Bph start value	All start values are usually the same unless a winding is intentionally shorted	0.005...40 pu	0.001 pu	1 pu
StrValC	Cph start value	All start values are usually the same unless a winding is intentionally shorted	0.005...40 pu	0.001 pu	1 pu
OpDITmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	0 ms

Characteristics

Table 214 - Characteristics of the *ITPDIF*

Characteristics		Values
Start value	Accuracy	±2% or ±0.001 pu
	Reset ratio	95% ± 5%
Operate delay	Accuracy	±2% or ±10 ms
Reset time	Accuracy	< 30 ms
Characteristic time	Start time	< 25 ms at 2 Is
	Overshoot time	< 30 ms

Inadvertent energization (*IEPIOC*, ANSI 50/27)

Description

Accidental energization of a generator can cause severe damage to the machine. When the machine is at standstill, if the Circuit Breaker (CB) is closed, then the generator begins to act as an induction motor with the surface of the rotor core, and the rotor winding slot wedges acting as the rotor current conductors. This abnormal current in the rotor can cause overheating and damage.

The protection is capable of differentiating between a normal generator shutdown/starting sequence, and a generator shutdown/inadvertent energization sequence. They are shown in the Generator shutdown and normal starting and inadvertent starting, page 313.

- Generator shutdown

  There is no current and the voltage collapses to zero over a short period of time, corresponding to the generator running down.

- Normal generator starting

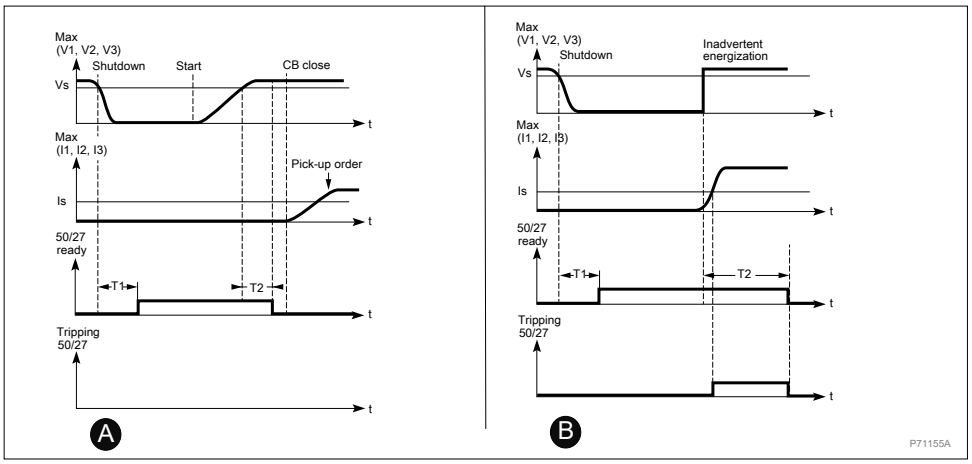
  The generator is started, and the output voltage increases to the correct value. The coupling CB is closed when the voltages are high, and synchronization is achieved between the generator and the remote system. When the CB is closed, the generator load current ramps up from zero to the target level.

- Inadvertent energization

  When the CB is closed, the machine voltage takes the value of the applied system and the current increases when the voltage is applied.

The function detects when the machine is not running by monitoring the voltage output from the machine side Voltage Transformer (VT). The busbar VT is not used. The element is only active once the current and voltage are below set levels for the activation time. It will then deactivate when voltage is above setting for the release delay. If current appears above setting when the element is active it will operate.

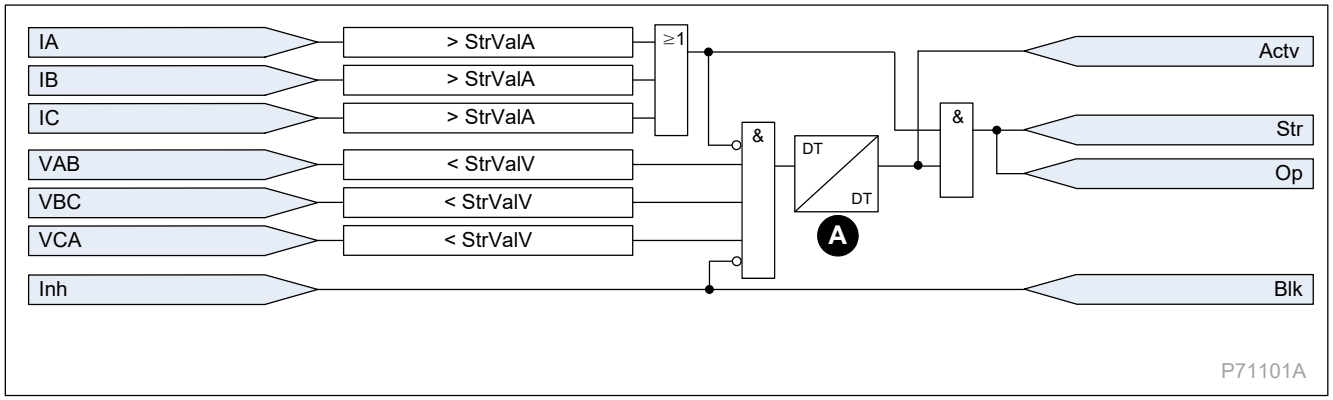
Figure 167 - Generator shutdown and normal starting and inadvertent starting



A	Example: Generator shutdown and normal starting.	B	Example: Generator shutdown and inadvertent starting.

Block diagram

Figure 168 - Block diagram of the *IEPIOC*



A	Operate delay: *ActDITmms* Reset delay: *DITmms*

- The function includes an instantaneous three-phase undervoltage detector, based on phase-to-phase voltage quantities, which operates only if all three phases are below the undervoltage threshold, and a three-phase overcurrent detector which operates if one of the currents is above the threshold.
- The function is primed by a condition when three-phase undervoltage and undercurrent conditions are present for a duration greater than operate delay. This indicates that the CB is open and the generator has been de-energized. In the event of a VT Miniature Circuit Breaker (MCB) open condition, blocking with the overcurrent ensures correct operation of the element. The operate delay makes the function insensitive to voltage sags. Under normal conditions the generator runs up whilst the coupling CB is open, so the generator voltage output will ramp above the undervoltage reset threshold, which causes the element to reset and initiate reset time. Usually the coupling CB is closed after reset time, ideally with minimal impact on the power system. However, if an overcurrent condition occurs during the delay of reset time, this results in an operation.

The active output, which indicates the element will operate if current appears, picks up after operate delay following the three-phase undervoltage and undercurrent condition being met and resets after reset time following reset of the undervoltage and undercurrent elements.

Input and output signals

Table 215 - Input signals of the *IEPIOC*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
UABUBCUCA	Line voltage	Line voltage
IAIBIC	Phase current	Phase current

Table 216 - Output signals of the *IEPIOC*

Name	Short label	Infotip
Actv	Active	Active
Str	Start	Start
Op	Operate	Operate
Blk	Blocked	Blocked

Setting parameters

Table 217 - Settings of the *IEPIOC*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrValA	Overcurrent start value	Overcurrent start value	0.1...2 pu	0.01 pu	0.1 pu
StrValV	Undervoltage start value	Undervoltage start value	0.1...1 pu	0.01 pu	0.8 pu
ActDITmms	Activation delay	The element is active if the current and voltage are below start values for this period	0...10000 ms	1 ms	5000 ms
DITmms	Release delay	If voltage above start is present for this time the element will deactivate. During this release period operation will occur if current exceeds the start value	0...10000 ms	1 ms	500 ms

Characteristics

Table 218 - Characteristics of the *IEPIOC*

Characteristics		Values
Overcurrent start value	Accuracy	±5%
	Reset ratio	95% ± 5%
Undervoltage start value	Accuracy	±5%
	Reset ratio	102% ± 5%
Operate delay	Accuracy	±1% or < 40 ms
Reset time	Accuracy	±1% or < 40 ms

Overspeed (*POVS*, ANSI 12)

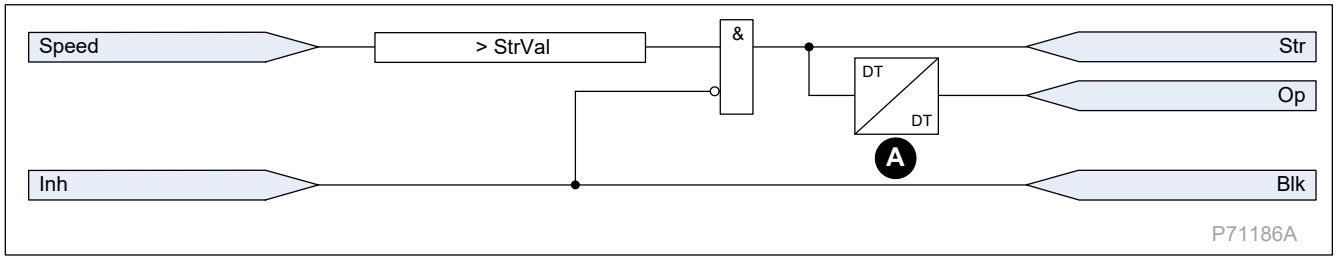
Description

The overspeed protection function is applied to motor or generator applications. The rotation speed of the applications is measured using cams mounted on the rotor, with the detection by means of a proximity sensor.

Overspeed protection is only available when speed detection function is enabled. Whenever the motor speed reaches the threshold, this function starts and an instantaneous start signal is issued. If the fault remains active longer than the operate delay setting, a trip signal is issued.

Block diagram

Figure 169 - Block diagram of the *POVS*



A Operate delay: *OpDITmms*
Reset delay: 0 ms

Input and output signals

Table 219 - Input signals of the *POVS*

Name	Short label	Infotip
Speed	Speed	Internal signal from TRTN1
Inh[general]	Inhibit	Inhibit function

Table 220 - Output signals of the *POVS*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
Blk	Blocked	Blocked

Setting parameters

Table 221 - Settings of the *POVS*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrVal	Start value	Start value	1...1.6 pu	0.01 pu	1 pu
OpDITmms	Operate delay	Operate time delay	0...300000 ms	1000 ms	0 ms

Characteristics

Table 222 - Characteristics of the *POVS*

Characteristics		Values
Start value	Accuracy	< ±2%
	Reset ratio	95% ± 2%
Operate delay	Accuracy	< 600 ms
Characteristic time	Start time	< 600 ms
	Disengaging time	< 600 ms

Underspeed (*PZSU*, ANSI 14)

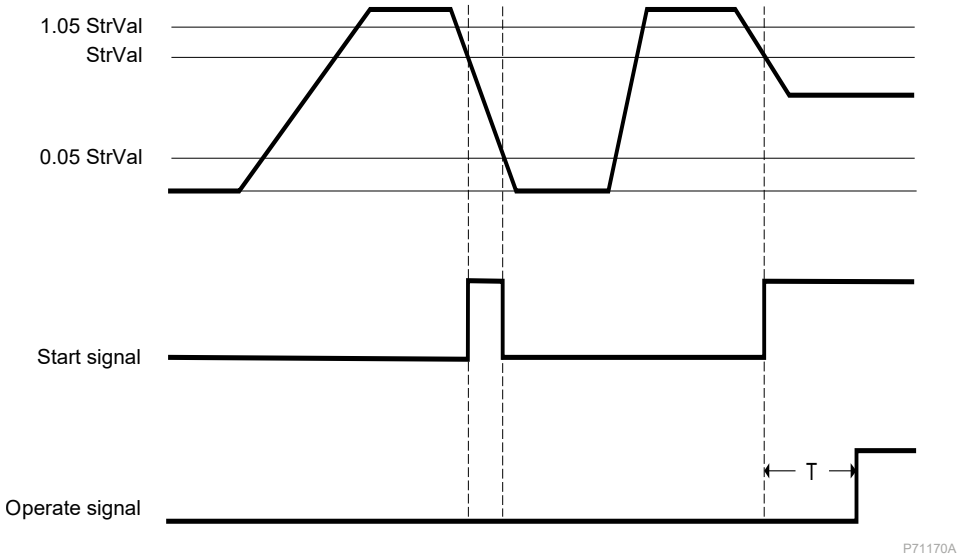
Description

Based on the measurement using cams mounted on the rotor, with detection by means of a proximity sensor, the underspeed protection function is applied to motor or generator applications to detect the slow-down of rotational speed after starting, resulting from the mechanical overloads or locked rotor.

The underspeed protection is only available when speed detection function is enabled.

The logic is shown in figure Starting and operating logic of the *PZSU*, page 317.

Figure 170 - Starting and operating logic of the *PZSU*

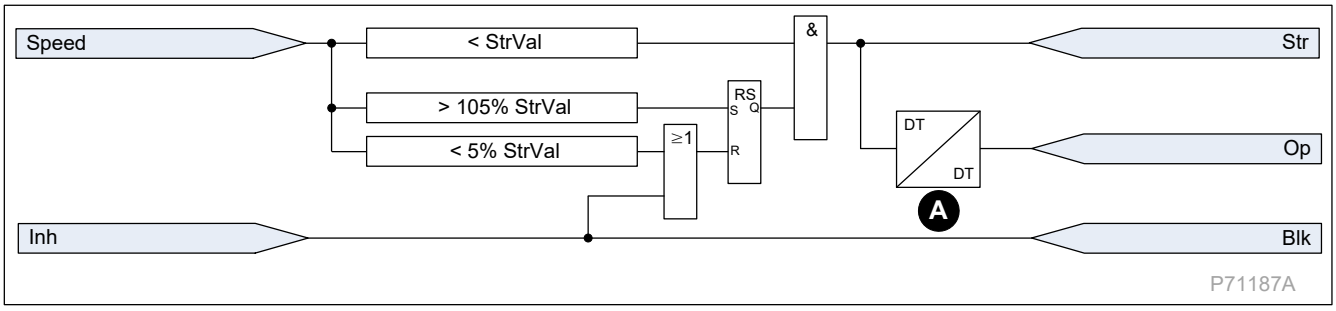


The function provides the start signal if the speed measured drops below the speed threshold after the speed exceeds the set point by 5%, which avoids tripping when the machine stopped. The underspeed protection is blocked when the motor speed drops below 5% of threshold, to avoid unwanted tripping when the motor is switched off.

If the start time of the underspeed protection function exceeds the operate delay time setting, a trip signal is issued.

Block diagram

Figure 171 - Block diagram of the *PZSU*



A Operate delay: *OpDITmms*
Reset delay: 0 ms

Input and output signals

Table 223 - Input signals of the *PZSU*

Name	Short label	Infotip
Speed	Speed	Internal signal from TRTN1
Inh[general]	Inhibit	Inhibit function

Table 224 - Output signals of the *PZSU*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
Blk	Blocked	Blocked

Setting parameters

Table 225 - Settings of the *PZSU*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrVal	Start value	Start value	0.01...1 pu	0.01 pu	0.4 pu
OpDITmms	Operate delay	Operate time delay	0...300000 ms	1000 ms	0 ms

Characteristics

Table 226 - Characteristic of the *PZSU*

Characteristics		Values
Start value	Accuracy	< ±2%
	Reset ratio	105% ± 2%
Operate delay	DT accuracy	< 600 ms
Characteristic time	Start time	< 600 ms
	Disengaging time	< 600 ms

Zerospeed (*ZEROPZSU*, ANSI 14)

Description

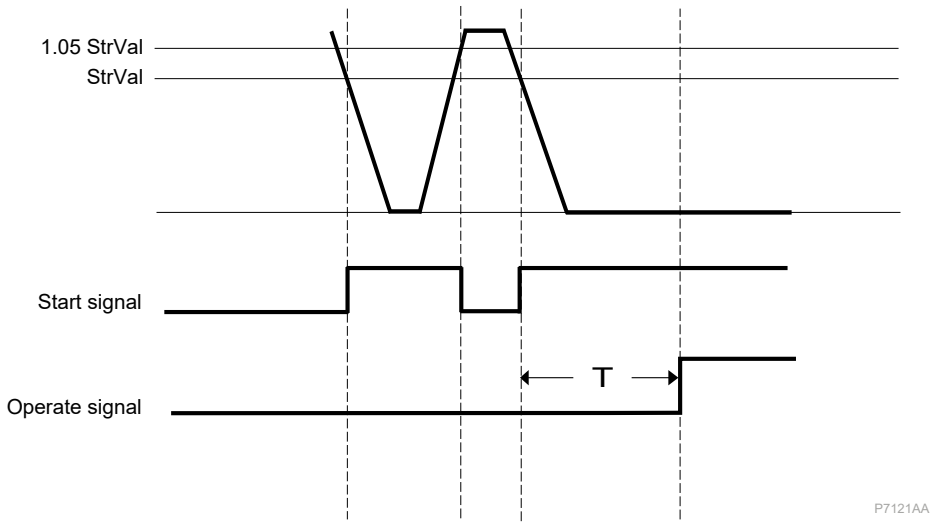
The zerospeed protection is only available when speed detection function is enabled.

This function is active when the motor speed is less than the threshold, which means the start signal will be asserted if the speed measured drops below the speed threshold. This function is inactive when the speed exceeds 105% of the threshold, which means the start signal will be deasserted.

If the start time of the zerospeed protection function exceeds the operate delay time setting, an operate signal is issued. This is usually used with other functions such as *PMSS* or *PMRI*.

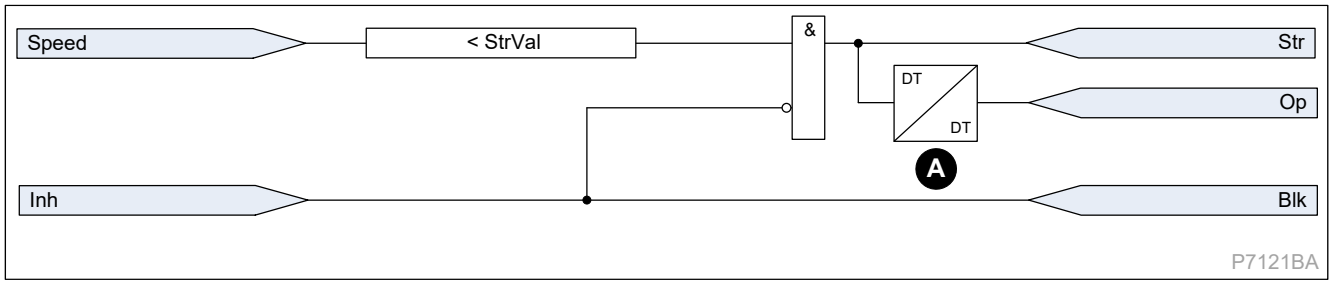
The logic is shown in figure Starting and operating logic of the *ZEROPZSU*, page 319.

Figure 172 - Starting and operating logic of the *ZEROPZSU*



Block diagram

Figure 173 - Block diagram of the *ZEROPZSU*



A Operate delay: *OpDITmms*
Reset delay: 0 ms

Input and output signals

Table 227 - Input signals of the *ZEROPZSU*

Name	Short label	Infotip
Speed	Speed	Internal signal from TRTN1
Inh[general]	Inhibit	Inhibit function

Table 228 - Output signals of the *ZEROPZSU*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
Blk	Blocked	Blocked

Setting parameters

Table 229 - Settings of the *ZEROPZSU*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
StrVal	Start value	Per unit speed below this value will start the operation timer	0.01...1 pu	0.01 pu	0.05 pu
OpDITmms	Operate delay	Operate time delay	0...300000 ms	1000 ms	0 ms

Characteristics

Table 230 - Characteristic of the *ZEROPZSU*

Characteristics		Values
Start value	Accuracy	< ±2%
	Reset ratio	105% ± 2%
Operate delay	DT accuracy	< 600 ms
Characteristic time	Start time	< 600 ms
	Disengaging time	< 600 ms

Speed detection (*TRTN*)

Description

The speed detection function is applied to motor or generator applications where the rotation speed is measured using cams mounted on the rotor, with detection by means of proximity detectors. The output from the proximity sensor is a train of electrical pulses, each pulse corresponds to the detection of an individual cam.

If a given application has R number of cams mounted 360º/R apart on a rotor, the number of cams R is equal to the number of pulses per rotation of the rotor shaft. The time interval ΔT (in seconds) between consecutive pulses is used to calculate the revolutions per minutes (rpm).

The rpm is calculated as follows based on the time interval of the two pulses ΔT from Binary Input (BI) and the setting of pulse per rotation (R).

$$\omega = \frac{60}{\Delta T(s) \times R} = \frac{60000}{\Delta T(ms) \times R}$$

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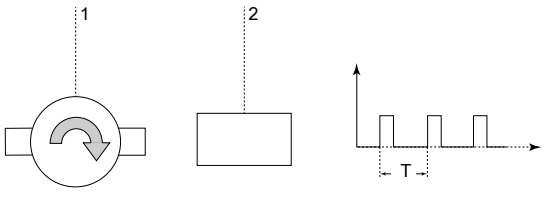
Motor speed slip rate is calculated as follows:

$$S = \frac{\omega_1 - \omega}{\omega_1} \times 100\%$$

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ω_1 is nominal speed and it is a setting parameter, ω is motor speed (rpm).

Figure 174 - Proximity sensor



1	Rotor with 2 cams	2	Proximity sensor

Table 231 - Characteristics of proximity sensor

Characteristics	Values
Pass-band (in Hz)	> 2 ω_n x R / 60 **NOTE:** ω_n is the nominal speed.
Output	24 to 250 V DC, 3 mA minimum
Leakage current in open status	< 0.5 mA
Voltage dip in closed status	< 4 V (with 24 V power supply)
Pulse duration	0 status > 120µs 1 status > 200µs

NOTE: The proximity sensor output pulses are at a voltage level, and the voltage level is compatible with the logic inputs (24...250 V DC). A logic input is mapped to a given proximity sensor to perform the speed measurement.

The Mixed Input/Output (MIO) module and Trip Circuit Supervision Input/Output (TIO) module contain two specific binary input (BI7 and BI8) to detect the rotational speed. It recognizes the high voltage signal as status 1 with pulse width greater than 200 µs, and the low voltage signal as status 0 with pulse width greater than 120 µs.

NOTICE

IMPROPER EQUIPMENT OPERATION

If the counting input BI7 or BI8 on MIO or TIO is selected for speed detection, both BI7 and BI8 cannot be used by any other protection functions.

Failure to follow instructions can result in equipment damage.

Input and output signals

Table 232 - Analog input signals of the *TRTN*

Name	Short label	Infotip
IntTCnt	Pulse interval	Internal signal from T1LPDI1
PluseMarker	Pulse number	Internal signal from T1LPDI1

Table 233 - Analog output signals of the *TRTN*

Name	Short label	Infotip
MotSpd	Machine speed	Machine speed
Slip	Slip rate	Slip rate

Table 234 - Binary output signals of the *TRTN*

Name	Short label	Infotip
ZeroSpd	Zero speed	Zero speed

Setting parameters

Table 235 - Settings of the *TRTN*

Name	Short label	Infotip	Setting Range	Step Size	Default Setting
PPR	Pulses per rotation	Pulses per rotation	1...24	1	1
NomSpd	Nominal speed	Nominal speed	15...10000 rpm	1 rpm	3000 rpm
ZeroTmms	Zero operate time	When a pulse is not received for this time the zero speed output will be set	0...300000 ms	1000 ms	60000 ms

NOTE: The limitation for the pulse per rotation (PPR) is: $(\omega_n \times R)/60 \leq 1000$

- ω_n = nominal speed
- R = pulses per rotation

Characteristics

Table 236 - Characteristics of the *TRTN*

Characteristics	Values
Motor speed calculating rate	200 ms
Motor speed measurement range	0...10000 rpm
Motor speed measurement accuracy	±2%
Sample refresh period	100 ms

Field failure (*FFPDIS*, ANSI 40)

Description

Complete loss of excitation may arise as a result of accidental tripping of the excitation system, an open circuit or short circuit occurring in the excitation DC circuit, flashover of any slip rings or failure of the excitation power source.

When the excitation of a synchronous motor fails, not enough synchronizing torque is provided to keep the rotor locked in step with the stator rotating magnetic field. The machine would then be excited from the power system and hence be operating as an induction motor.

In generator applications, if the field is lost the generator can slightly overspeed. Without a field the stator windings will appear as an inductive load fed from the power system.

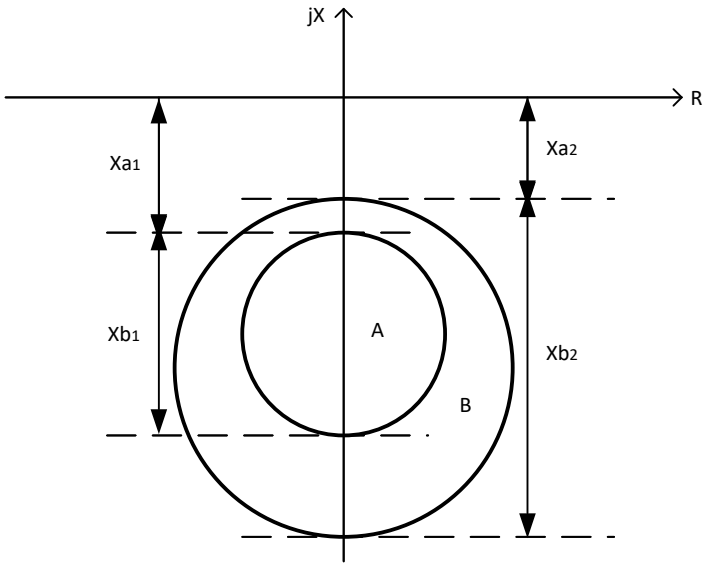
These conditions will result in an increasing level of reactive power being drawn from the power system. If the system cannot supply enough reactive power the system voltage will drop and the system may become unstable. In order to ensure fast tripping under these conditions, one of the impedance elements is used with a short time delay. This can trip the machine quickly to preserve system stability. This element has a small diameter to prevent tripping under power swinging conditions. The second impedance element, set with a larger diameter and time

delay, can provide detection of field failure when permanent magnetism partially maintains the field.

Field failure characteristic

The field failure protection function is based on an offset mho characteristic in the negative reactance plane. It has two stages. Stage 1 is enabled by default and stage 2 can be enabled or disabled by a setting *Mho2Mod*. Stage 1 will normally detect any field failure but is delayed to avoid operation on power swings. If required, stage 2 can be enabled to operate faster for a reduced impedance not affected by power swings. The PowerLogic P7 uses positive sequence impedance. The mho characteristic in the negative reactance region of the R-X plane is shown in the following figure.

Figure 175 - Field failure characteristic



Xa1	***Ofs***, offset from origin of stage1	Xb1	***PoRch***, diameter of mho of stage1
Xa2	***SndOfs***, offset from origin of stage2	Xb2	***SndPoRch***, diameter of mho of stage2
A	Operating area of stage1	B	Operating area of stage2

Start logic

The function asserts the start output when the following conditions are simultaneously present:

- No inhibit input
- The positive sequence impedance (with valid quality) falls within the offset mho circle characteristic
- The positive sequence current exceeds 10% In
- The positive sequence voltage exceeds 10% Vn

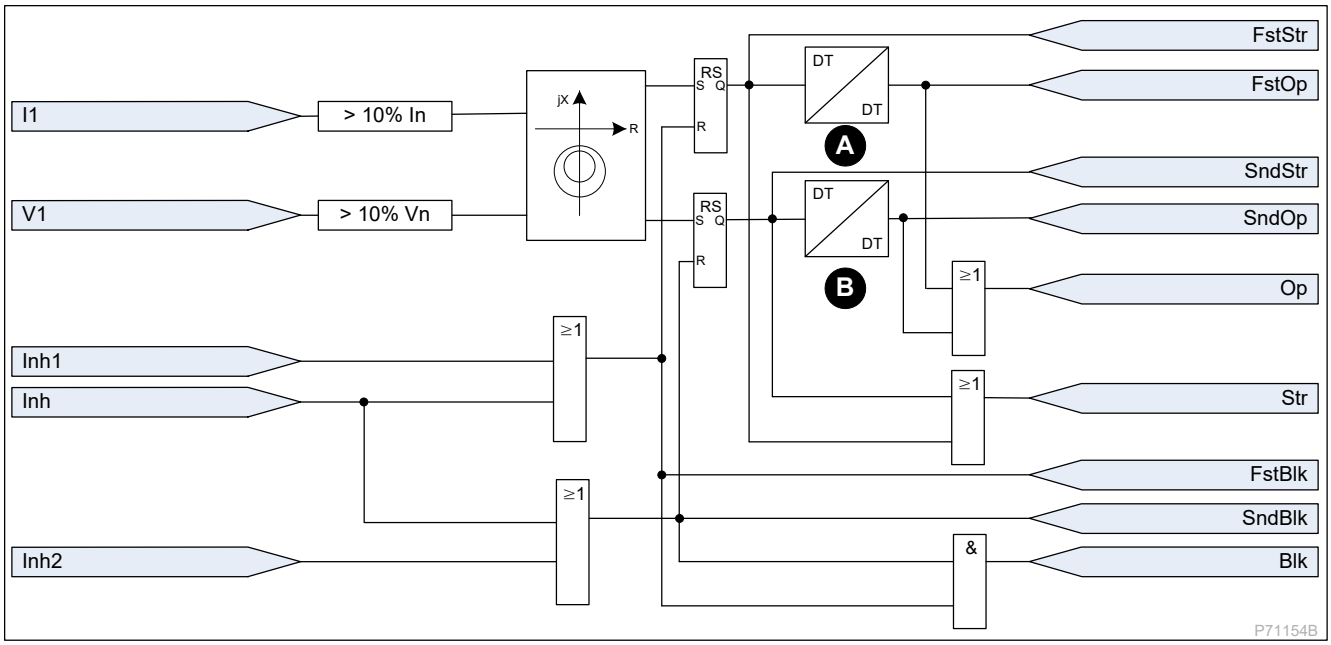
The function resets the start output providing the positive sequence impedance falls outside of an expanded offset mho circle, with diameter 105% of the set threshold.

Operate logic

The function asserts the operate output providing the start output remains for a duration of operate delay and the inhibit input is not presents.

Block diagram

Figure 176 - Block diagram of the *FFPDIS*



A	Operate delay: *OpDITmms* Reset delay: 0 ms	B	Operate delay: *SndOpDITmms* Reset delay: 0 ms

Input and output signals

Table 237 - Input signals of the *FFPDIS*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
Inh1[general]	Inhibit Z1	Inhibit stage 1
Inh2[general]	Inhibit Z2	Inhibit stage 2
V1Cplx	Line voltage	Line voltage
I1Cplx	Phase current	Phase current

Table 238 - Output signals of the *FFPDIS*

Name	Short label	Infotip
FstStr	Stage 1 start	Stage 1 start
SndStr	Stage 2 start	Stage 2 start
Str	Start	Start
FstOp	Stage 1 operate	Stage 1 operate
SndOp	Stage 2 operate	Stage 2 operate
Op	Operate	Operate
FstBlk	Stage 1 blocked	Stage 1 blocked
SndBlk	Stage 2 blocked	Stage 2 blocked
Blk	Blocked	Blocked

Setting parameters

Table 239 - Settings of the *FFPDIS*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
Ofs	Stage 1 offset	Stage 1 offset	0.0005...5 pu	0.0001 pu	0.2 pu
PoRch	Stage 1 diameter	Stage 1 diameter	0.0005...5 pu	0.0001 pu	2 pu
OpDlTmms	Stage 1 operate delay	Stage 1 operate time delay	0...10000000 ms	1 ms	5000 ms
Mho2Mod	Stage 2 status	If required, stage 2 is usually set with the same offset as stage 1 with a smaller diameter and faster operating time. It should be set to avoid operation on power swings	• Off • On		Off
SndOfs	Stage 2 offset	Stage 2 offset	0.0005...5 pu	0.0001 pu	0.2 pu
SndPoRch	Stage 2 diameter	Stage 2 diameter	0.0005...5 pu	0.0001 pu	1 pu
SndOpDlTmms	Stage 2 operate delay	Stage 2 operate time delay	0...10000000 ms	1 ms	0 ms

Characteristics

Table 240 - Characteristics of the *FFPDIS*

Characteristics		Values
Operating area	Accuracy	±5% or ±0.0001 pu (50%...120% Vn)
	Accuracy (min op thresholds)	±5%
	Reset ratio	105% ± 5%
Operate delay	Accuracy	±2% or ±10 ms
Characteristic time	Start time	< 45 ms at 0.9 Zs
	Disengaging time	< 30 ms at 1.1 Zs

Underimpedance (*UZPDIS*, ANSI 21)

Description

The underimpedance protection function is used to detect faults on either side of the step-up transformer. The transformer is typically star-delta producing a 2-1-1 fault distribution on the generator (delta) side for a phase-phase fault on the grid (star) side. The impedance is calculated using phase-phase voltage divided by phase currents to detect this condition.

ZA=VAB/IA
ZB=VBC/IB
ZC=VCA/IC

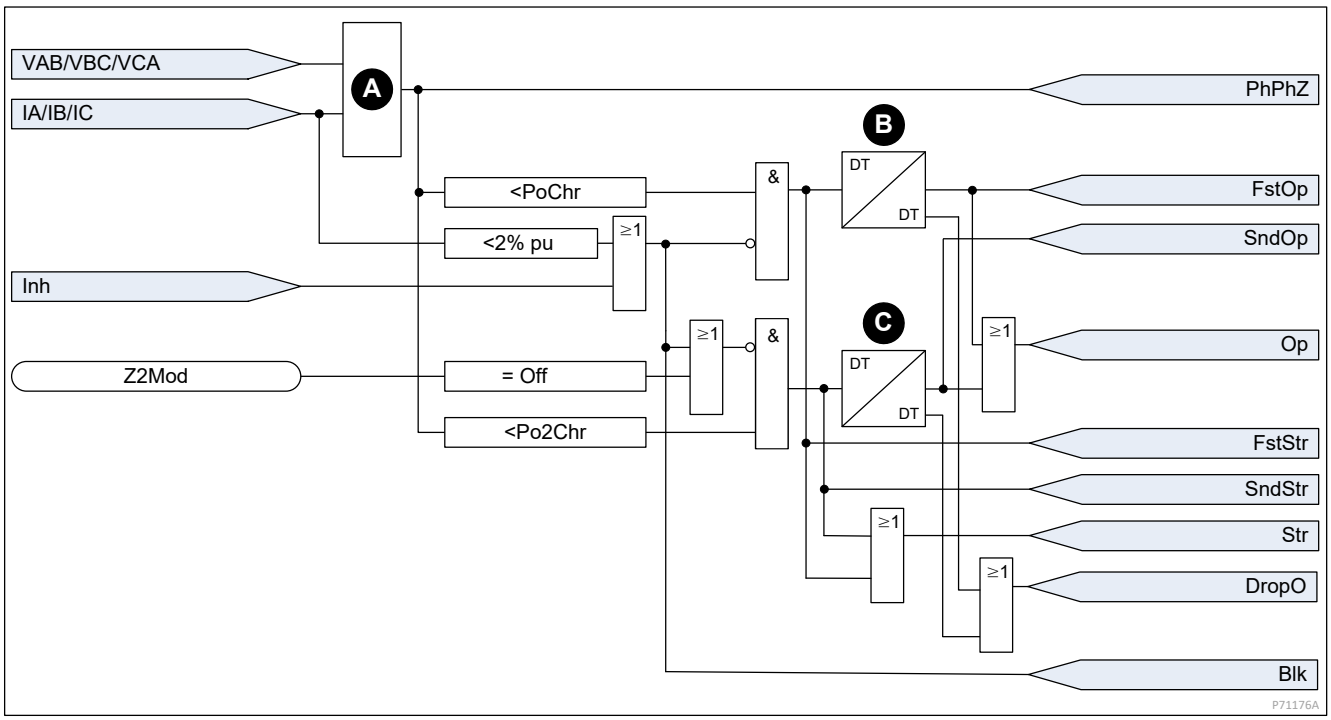
The start signal is issued when any of the magnitude of the calculated impedances is under the setting threshold. After the operate delay has elapsed, the operate signal is issued.

If the phase current is under 2% pu, the related impedances will be set to 0 and will not trigger start and operate signals.

Two zones are available for the underimpedance protection function. Zone 2 can be enabled or disabled separately. Stage 1 is normally set to see faults on either side of the step-up transformer and must grade with the outgoing protection. Stage 2 can be enabled to provide faster tripping for faults up to the transformer.

Block diagram

Figure 177 - Block diagram of the *UZPDIS*



A	Impedance calculation	B	Operate delay: *OpDITmms* Reset delay: *RsDITmms*	C	Operate delay: *Op2DITmms* Reset delay: *Rs2DITmms*

Input and output signals

Table 241 - Input signals of the *UZPDIS*

Name	Short label	Infotip
Inh[general;phsA;phsB;phsC]	Inhibit	Inhibit function
IAIBIC	Phase current	Phase current
UABUBCUCA	Line voltage	Line voltage

Table 242 - Output signals of the *UZPDIS*

Name	Short label	Infotip
FstStr	Stage 1 start	Stage 1 start
SndStr	Stage 2 start	Stage 2 start
Str	Start	Start
FstOp	Stage 1 operate	Stage 1 operate
SndOp	Stage 2 operate	Stage 2 operate
Op	Operate	Operate

Table 242 - Output signals of the *UZPDIS* (Continued)

Name	Short label	Infotip
Blk	Blocked	Blocked
DropO	Drop out	Drop out

Setting parameters

Table 243 - Settings of the *UZPDIS*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Normally applied as a backup protection for generators	• On • Off		Off
PoChr	Stage 1 start value	Usually set to see faults through the step up transformer	0.0005...5 pu	0.0001 pu	0.7 pu
OpDlTmms	Stage 1 operate delay	Usually set to grade with outgoing protection on the HV of the step up transformer	0...10000000 ms	1 ms	2000 ms
RsDlTmms	Stage 1 reset delay	Stage 1 reset time delay	0...10000000 ms	1 ms	0 ms
Z2Mod	Zone 2 status	A second stage can be applied for faster backups of faults within the generator or step up transformer	• Off • On		Off
Po2Chr	Stage 2 start value	Usually set to cover the generator and partially into the step up transformer	0.0005...5 pu	0.0001 pu	0.25 pu
Op2DlTmms	Stage 2 operate delay	Usually set with a small time delay to backup other protection	0...10000000 ms	1 ms	500 ms
Rs2DlTmms	Stage 2 reset delay	Stage 2 reset time delay	0...10000000 ms	1 ms	0 ms

Characteristics

Table 244 - Characteristics of the *UZPDIS*

Characteristics		Values
Start value	Accuracy	±5% or ±0.005 pu
	Reset ratio	105% ± 5%
Operate delay	Accuracy	±2% or ±10 ms
Characteristic time	Start time	< 25 ms at 0.8 Zs
	Disengaging time	< 30 ms at 1.2 Zs
	Overshoot time	< 30 ms at 0...1.2 Zs

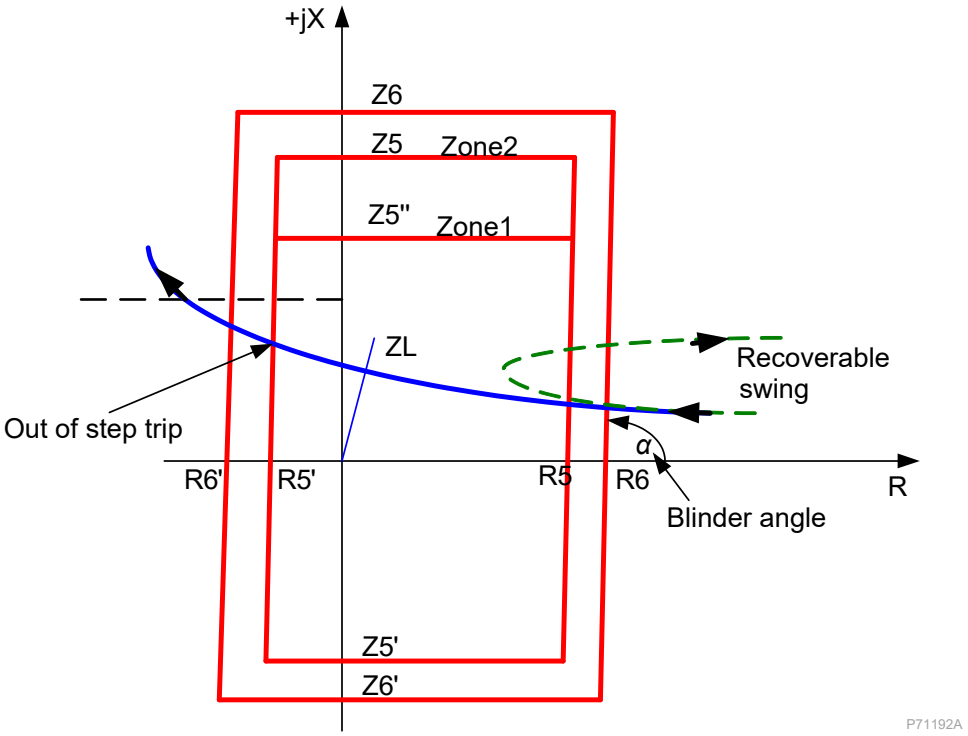
Out of step (*OOSPPAM*, ANSI 78)

Description

Out of step is detected by looking at the impedance loci travelling during an out of step seen at the device measuring point.

- In the case of a generator, the locus will travel from right to left.
- In the case of a synchronous machine, the locus will travel from left to right.

Figure 178 - Out of step characteristic



Z5	*PoRch*	Z5'	*PoRchRev*
Z5"	*PoRch* × *PctRchZ1*	Z6	*PoRch* × *PctRch*
Z6'	*PoRchRev* × *PctRchRev*	R5	*RisPhRch*
R5'	*RisPhRchRev*	R6	*RisPhRch* × *PctRisRch*
R6'	*RisPhRchRev* × *PctRisRchRev*		

All polygon characteristics are independent. Independent settings are available for the respective reactance and resistive reaches.

A Z5" reach is used to distinguish between generator and system slips.

- **Zone 1** is Z5', R5', Z5" and R5.
- **Zone 2** is Z5', R5', Z5 and R5.
- **Outer zone** is Z6', R6', Z6 and R6.

All four resistive blinders are parallel, using the common angle setting *BldAng*.

The measured positive sequence impedance is calculated as:

Z1 = V1/I1

Where,

V1 and *I1* are positive sequence voltage and current derived from the measured phase quantities.

Operating principle

The *OOSPPAM* detection algorithm is based on measuring the speed of positive sequence impedance passing through zones.

When the positive sequence impedance is in **outer zone**, the *Outer start* is asserted. When the positive sequence impedance is in **zone 2**, the *Inner start* is asserted.

When measured positive sequence impedance touches the **outer zone**, a timer is started.

- If it takes less than 25 ms from entering **outer zone** to entering **zone 2**, the device will consider this to be a power system fault and not an out of step trip condition.

  NOTE: The timer of 25 ms is a fixed timer in the logic and not accessible.
- If it takes more than 25 ms from entering **outer zone** to entering **zone 2**, *Start* will be asserted.

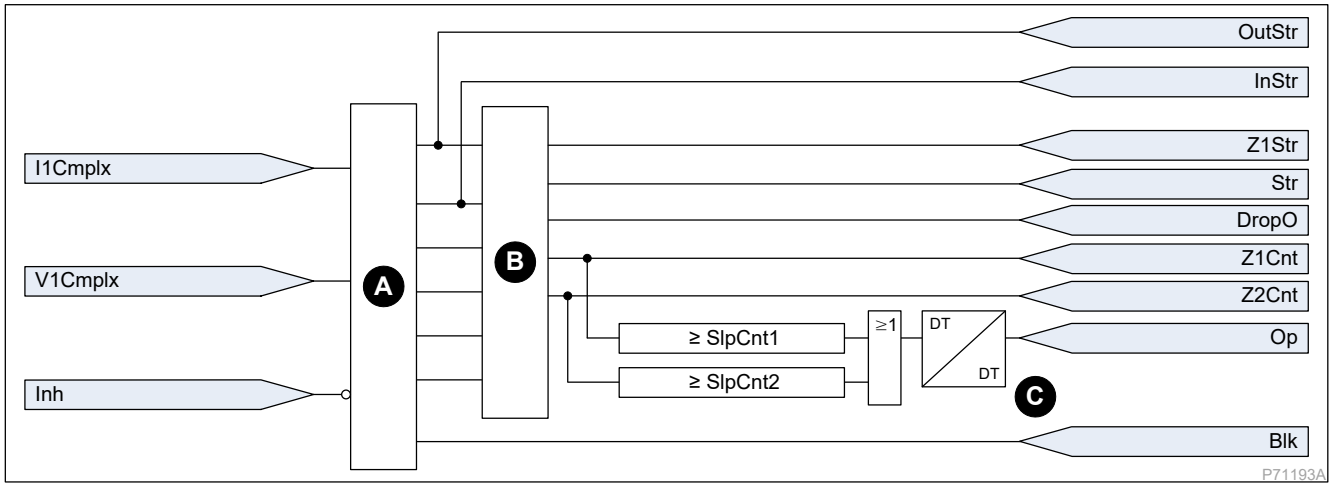
  Since **zone 1** is in **zone 2**, so if it takes more than 25 ms from entering **outer zone** to entering **zone 1**, both *Start* and *Zone 1 start* will be asserted.
- If the resistive part of the positive sequence impedance leaves **zone 2** with the same polarity of entry, it is deemed a recoverable swing. No tripping will be issued.
- If the resistive part of the positive sequence impedance leaves **zone 2** with the opposite polarity of entering **zone 2**, an out of step condition is recognized, counter for **zone 2** is started.
- If the positive sequence impedance leaves **zone 2** and resistive part leaves **zone 1** with the opposite polarity of entering **zone 1**, counter for **zone 1** is started.

When the counter for **zone 2** changes from *0* to *1*, the reset timer will be started, the impedance loci travelling occurring before the reset timer exceeds *RsDlTmms* will increase the counter. When the reset timer expires, the counter resets.

The *Operate* will be asserted after *OpDlTmms* when any of the out of step counters exceeds the setting for zones.

Block diagram

Figure 179 - Block diagram of the *OOSPPAM*



A Out of step characteristic B Out of step logic C Operate delay: *OpDlTmms*

Reset delay: 0 ms

Input and output signals

Table 245 - Input signals of the *OOSPPAM*

Name	Short label	Infotip
V1Cmplx	Line voltage	Linked to line voltage input source
I1Cmplx	Phase current	Linked to phase current input source
Inh[general]	Inhibit	Inhibit function

Table 246 - Output signals of the *OOSPPAM*

Name	Short label	Infotip
OutStr	Outer start	Outer start
InStr	Inner start	Inner start
Z1Str	Zone 1 start	Zone 1 start
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked
Z1Cnt	Slip count zone 1	Slip count zone 1
Z2Cnt	Slip count zone 2	Slip count zone 2

Setting parameters

Table 247 - Settings of the *OOSPPAM*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
PoRch	Inner forward reach	The inner zone is used for operation when the fault locus exits with the opposite sign resistance to entry. This is the inner zone forward reach on the blinder angle determined by the maximum generation voltage to system voltage ratio	0.0005...5 pu	0.0001 pu	1 pu
PoRchRev	Inner reverse reach	This is the inner zone reverse reach on the blinder angle determined by the minimum generation voltage to system	0.0005...5 pu	0.0001 pu	1 pu
RisPhRch	Inner res forward reach	This is the inner zone resistive forward reach determined by the maximum pole slip rate time to travel from the outer zone for generator applications	0.0005...5 pu	0.0001 pu	1 pu
RisPhRchRev	Inner res reverse reach	This is the inner zone resistive reverse reach determined by the maximum pole slip rate time to travel from the outer zone for motoring applications	0.0005...5 pu	0.0001 pu	1 pu
PctRch	Outer/inner forward reach	This is the ratio of the outer zone reach to the inner zone forward reach. The impedance must be in the outer zone for greater than 25ms to avoid operation during faults. Load impedance must be outside the outer zone	110...1000 %	10 %	110 %
PctRchRev	Outer/inner reverse reach	Outer/inner reverse reach ratio	110...1000 %	10 %	110 %
PctRisRch	Outer/inner res forward reach	Outer/inner resistive forward reach ratio	110...1000 %	10 %	110 %
PctRisRchRev	Outer/inner res reverse reach	Outer/inner resistive reverse reach ratio	110...1000 %	10 %	110 %
BldAng	Blinder angle	This is the tilt of the inner and outer characteristics	20...90 deg	1 deg	80 deg
PctRchZ1	Z1/inner forward reach	This is the forward reach of Z1 along the blinder angle relative to the inner zone forward reach. This sets the lower portion of then inner zone for generator slips when different slip counts are required for generator and power system slips	0.01...1	0.01	1
SlpCnt1	Slip count zone 1	Slip counts for zone 1 (generator)	1...20	1	1

Table 247 - Settings of the *OOSPPAM* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
SlpCnt2	Slip count zone 2	Slip counts for zone 2 (transformer/system)	1...20	1	1
OpDlTmms	Operate delay	Operation is instant when the fault locus leaves the inner zone. This delays the operate signal to avoid operation during high current levels	0...10000000 ms	1 ms	0 ms
RsDlTmms	Reset delay	This is the time delay after a slip when the slip count is reset. When multiple slips are set the time between slips must be less than this value	0...10000000 ms	1 ms	30000 ms

NOTE: *SlpCnt1* and *SlpCnt2* should meet the formula *SlpCnt1* ≤ *SlpCnt2*.

Characteristics

Table 248 - Characteristics of the *OOSPPAM*

Characteristics		Values
Inner start, Outer start	Accuracy	±5% or ± 0.0001 pu (50%...120% Vn)
	Reset ratio	105% ± 5%
	Minimum transition time	25 ms
Operate delay	Accuracy	±2% or ±10 ms
Characteristic time	Start time	< 45 ms (0.9 Rch)
	Disengaging time	< 30 ms

NOTE: The **Minimum transition time** from *Outer start* to *Inner start* must be exceeded to assert *Start*.

Overpower (*PPDOP*/*QPDOP*, ANSI 32P/32Q)

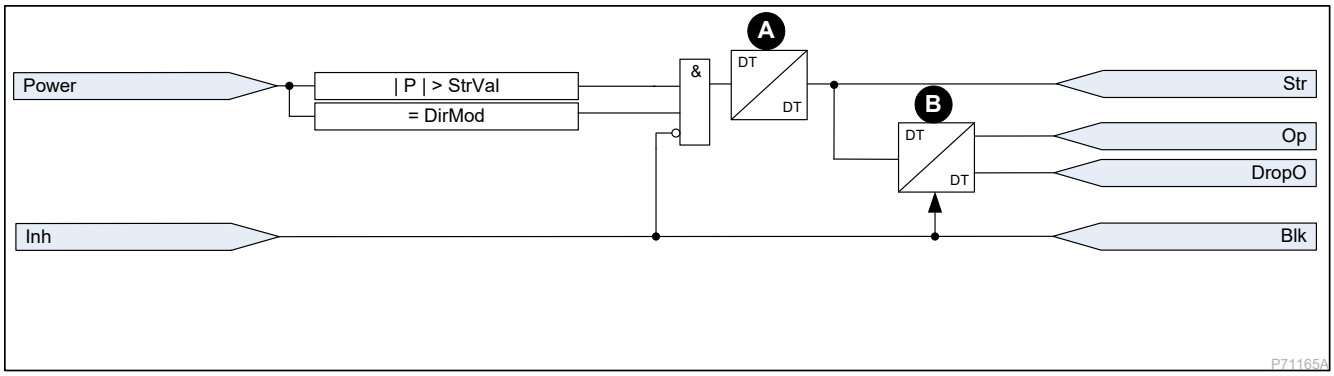
Description

The overpower protection (PDOP) is used to detect overpower conditions to help protect power plants. It is applied to limit total power output (active or reactive) or for reverse power protection of generators depending upon the directional mode. Reactive overpower can also be used to detect underexcitation.

When the absolute value of power exceeds the set threshold, the *Start* signal is issued if the power direction equals the set directional mode for more than 15 ms. The *Operate* signal is issued after the set operate delay.

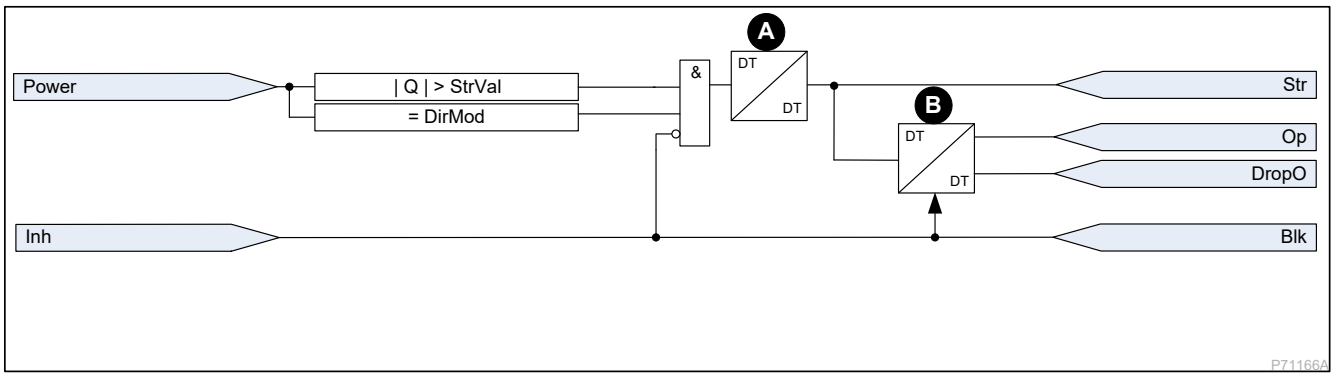
Block diagram

Figure 180 - Block diagram of the *PPDOP*



A	Operate delay: 15 ms Reset delay: 0 ms	B	Operate delay: *OpDITmms* Reset delay: *RsDITmms*

Figure 181 - Block diagram of the *QPDOP*



A	Operate delay: 15 ms Reset delay: 0 ms	B	Operate delay: *OpDITmms* Reset delay: *RsDITmms*

Input and output signals

Table 249 - Input signals of the *PPDOP*/*QPDOP*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
P	Total power	Internal signal from PWRGAPC1

Table 250 - Output signals of the *PPDOP*/*QPDOP*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked

Setting parameters

Table 251 - Settings of the *PPDOP*/*QPDOP*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
DirMod	Directional mode	Directional mode	• Forward • Reverse		Forward
StrVal	Start value	Start value	0.005...3.25 pu	0.001 pu	1 pu
OpDlTmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	0 ms
RsDlTmms	Reset delay	Reset time delay	0...10000000 ms	1 ms	0 ms

Characteristics

Table 252 - Characteristics of the *PPDOP*/*QPDOP*

Characteristics		Values
Start value	Accuracy	±2% or ±0.001 pu (0.01...4 pu) ±10% or ±0.001 pu (0.005...0.01 pu) 0.002 pu (0.003...0.005 pu) 0.001 pu (0.001...0.003 pu)
	Reset ratio	95% ± 5%
Operate delay	DT accuracy	±2% or ±10 ms
Reset time	DT accuracy	< 30 ms
Characteristic time	Start time	< 45 ms at 1.1 Ps

Underpower (*PPDUP*, ANSI 37P)

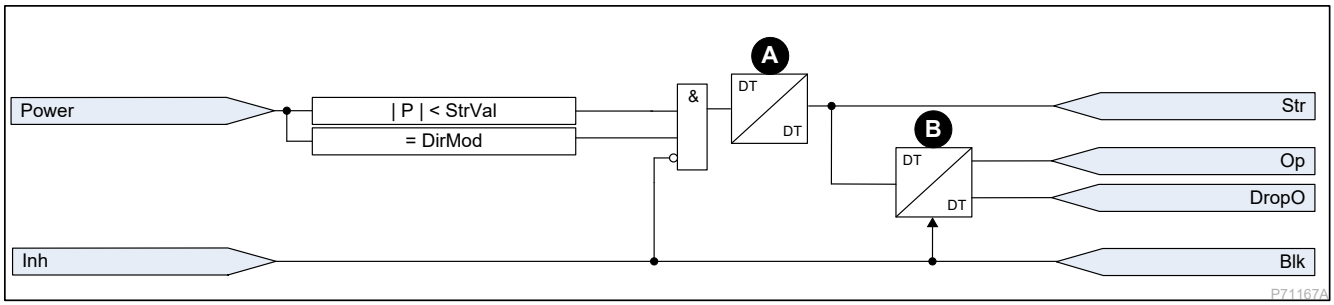
Description

The underpower protection (PDUP) is used to detect underpower conditions to help protect power plants. It can be used to detect loss of load for motors and also for low forward power shutdown of generators.

When the absolute value of power is below the set threshold, the *Start* signal is issued if the power direction equals the set directional mode. The *Operate* signal is issued after the set operate delay. By default the *BayDead* signal will be linked to the Inhibit input blocking operation when the bay is dead. This matrix link can be removed if operation is required when the bay is dead.

Block diagram

Figure 182 - Block diagram of the *PPDUP*



A	Operate delay: 15 ms Reset delay: 0 ms	B	Operate delay: *OpDITmms* Reset delay: *RsDITmms*

Input and output signals

Table 253 - Input signals of the *PPDUP*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
P	Total P	Internal signal from PWRGAPC1

Table 254 - Output signals of the *PPDUP*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked

Setting parameters

Table 255 - Settings of the *PPDUP*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
DirMod	Directional mode	Directional mode	• Forward • Reverse		Forward
StrVal	Start value	Start value	0.005...3.25 pu	0.001 pu	0.2 pu
OpDITmms	Operate delay	Operate time delay	0...10000000 ms	1 ms	1000 ms
RsDITmms	Reset delay	Reset time delay	0...10000000 ms	1 ms	0 ms

Characteristics

Table 256 - Characteristics of the *PPDUP*

Characteristics		Values
Start value	Accuracy	±2% or ±0.001 pu (0.01...4 pu)
	Reset ratio	105% ± 5%
Operate delay	DT accuracy	±2% or ±10 ms
Reset time	DT accuracy	< 30 ms at 1.2 Ps
Characteristic time	Start time	< 45 ms at 0.8 Ps

Measurement functions

CT/VT group and mapping

CT group

Description

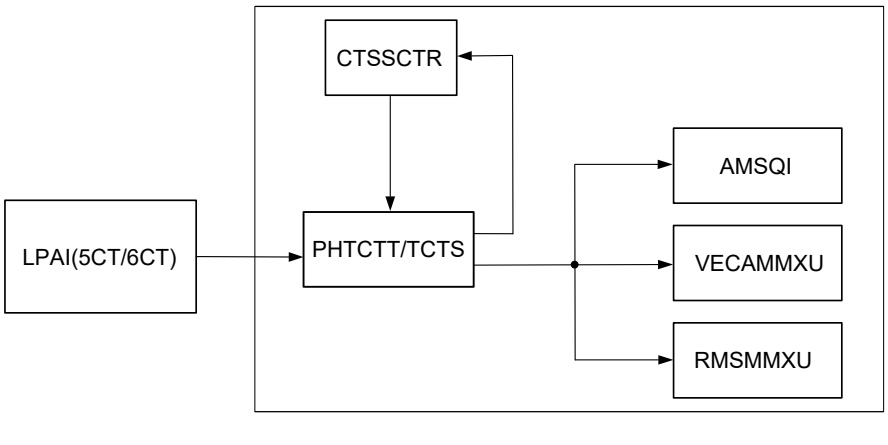
The CT group is a virtual data model, comprised of measurement function blocks (RMS, fundamental and sequence), supervision (*CTSSCTR*) and CT model (*PHTCTT* or *TCTS*).

The CT group maps the physical channels from the Low Power Analog Input (LPAI) module or the digital channels from SV subscriptions to the group's current channels for use in installed application functions.

On the HMI, the CT group measurements can be viewed under **General > Bay x > 3ph CT x** or **1ph CT x > Measurements**.

NOTE: 3ph CT 1 measurements are used as the inputs for **Measurements > Bay x > General**.

Figure 183 - Function block of CT group



Each bay can have multiple CT groups. Two types of CT group are available.

- 3ph CT group is used to handle multiple phases with or without neutral current signals.
- 1ph CT group is used to handle single phase current signal, usually used for neutral measurements using a toroidal CT. An angle correction can be applied to compensate for the external CT angle error for functions like the ground admittance protection. It does not have *CTSSCTR* or *AMSQI* functions.

NOTE: From the HMI or the PowerLogic Engineering Suite, the polarity for both types of CT group can be set as *Standard* or *Opposite* in case of incorrect wiring.

Rating

For the CT groups mapped to physical channels, the LPAI's input is a secondary value, the LPAI's output is a PU value according to the secondary configuration in the associated *PHTCTT* or *TCTS*. Primary values are calculated based on the PU value and primary rating. PU values and primary values are available for use in protection and measurement functions.

For the CT groups mapped to SV channels, the PU value is calculated based on the primary rating in the associated *PHTCTT* or *TCTS* and the primary value, which is received from SV subscriptions.

Connection type

Different connection types are given for the different CT connections available. 3ph (IA IB IC) should be used with three phase CTs. 3ph+N (IA IB IC IN) should be used with three phase CTs which are then paralleled to provide the neutral current in a residual (Holmgren) connection. 2ph (IA IC) is for two phase CTs and 2ph+N (IA IC IN) is for when two phase and ground relays are being replaced which use a residual connection and the wiring is difficult to change. Core balance CTs should not be used in 3ph CT groups. Depending upon which signals are available, the module will provide all valid measurements. Invalid measurements will be indicated via quality.

The connected phase or neutral can be selected for 1ph CT groups. It will be marked as valid and other signals marked as invalid. Connected functions will check the quality and will be blocked if the required signals are not available. Detailed quality output is shown in following truth tables.

NOTE: In the table, **Measured** or **Derived** indicates the quality of the signal is GOOD. **Measured** means that the output signal is directly calculated from the input signal, **Derived** means that the output signal is calculated from multiple measured signals.

Table 257 - Quality relationship between 3ph CT group and vector current outputs

CT connection type	Physical inputs				Vector current			
	IA	IB	IC	IN	IA Vector	IB Vector	IC Vector	IN Vector
3ph	IA	IB	IC	N/A	Measured	Measured	Measured	Derived
3ph+N	IA	IB	IC	IN	Measured	Measured	Measured	Measured
2ph	IA	N/A	IC	N/A	Measured	Invalid	Measured	Invalid
2ph+N	IA	N/A	IC	IN	Measured	Derived	Measured	Measured

Table 258 - Quality relationship between 3ph CT group and sequence current output

CT connection type	Physical inputs				Sequence vector current		
	IA	IB	IC	IN	I0	I1	I2
3ph	IA	IB	IC	N/A	Derived	Derived	Derived
3ph+N	IA	IB	IC	IN	Derived	Derived	Derived
2ph	IA	N/A	IC	N/A	Invalid	Derived	Derived
2ph+N	IA	N/A	IC	IN	Derived	Derived	Derived

Table 259 - Quality relationship between 3ph CT group and RMS current output

CT connection type	Physical inputs				RMS current			
	IA	IB	IC	IN	IARMS	IBRMS	ICRMS	INRMS
3ph	IA	IB	IC	N/A	Measured	Measured	Measured	Derived
3ph+N	IA	IB	IC	IN	Measured	Measured	Measured	Measured
2ph	IA	N/A	IC	N/A	Measured	Invalid	Measured	Invalid
2ph+N	IA	N/A	IC	IN	Measured	Derived	Measured	Measured

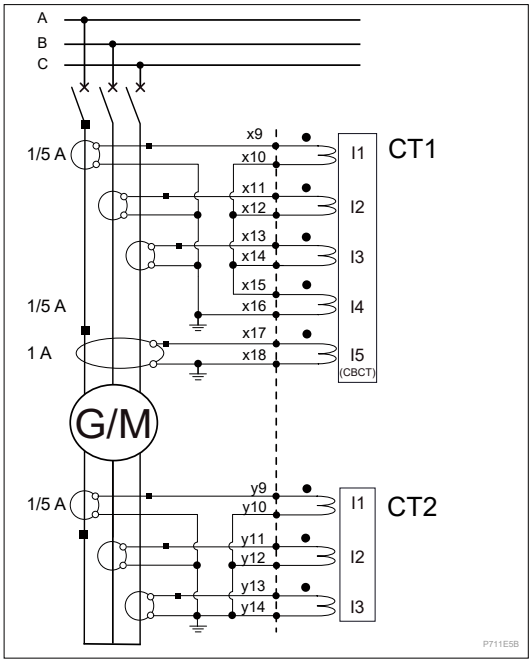
Quality for 1ph CT group

1ph CT group includes CT connection type configuration, the quality will be checked according to CT connection type.

CT application instance

A typical CT application scenario is shown in the figure below. To implement this application, two 3ph CT groups and one 1ph CT group are required. The first 3ph CT group corresponds to the three-phase current of generator terminal, the connection type is 3ph+N. The second 3ph CT group corresponds to the three-phase current of the generator star point, the connection type is 3ph. The 1ph CT group corresponds to the residual current of generator terminal and the connection type is Nph.

Figure 184 - CT application scenario



x: The first slot used by the CT/VT analog module takes 2 slots. For example, if the analog module is fitted in slots B & C then x9 becomes B9.

y: The CT/VT analog module takes 2 slots. For example, if the analog module is fitted in slots D & E then y9 becomes D9.

Phase current

The PowerLogic P7 measures the fundamental and RMS values of phase current inputs using 1A/5A CTs.

Table 260 - Measurements of currents

Value	Description
Fundamental value	
IA	Fundamental value of phase current IA.
IB	Fundamental value of phase current IB.
IC	Fundamental value of phase current IC.
RMS value	
IARMS	RMS value of phase current IA.

Table 260 - Measurements of currents (Continued)

Value	Description
IBRMS	RMS value of phase current IB.
ICRMS	RMS value of phase current IC.

The calculation is performed as follows and is computed over a frequency tracked cycle with n=48.

$$I_{RMS} = \sqrt{\frac{1}{n}\sum_{k=1}^{n} I_k^{\,2}}$$ E71166A

Neutral current

IN can be measured directly if the neutral input is provided. Otherwise, the neutral current is calculated by the vector sum of the three-phase currents.

Sequence current

The PowerLogic P7 measures the sequence current value based on three currents connected to the standard CT.

The calculation is done as follows:

NOTE: In 2ph mode, Ia+Ib+Ic equals zero.

Phase rotation	Formula
ABC	$\vec{I_1} = \frac{1}{3}(\vec{IA} + \alpha\vec{IB} + \alpha^2\vec{IC})$ E71167A
	$\vec{I_2} = \frac{1}{3}(\vec{IA} + \alpha^2\vec{IB} + \alpha\vec{IC})$ E71168A
	$\vec{I_0} = \frac{1}{3}(\vec{IA} + \vec{IB} + \vec{IC})$ E71169A
ACB	$\vec{I_1} = \frac{1}{3}(\vec{IA} + \alpha^2\vec{IB} + \alpha\vec{IC})$ E71170A
	$\vec{I_2} = \frac{1}{3}(\vec{IA} + \alpha\vec{IB} + \alpha^2\vec{IC})$ E71171A
	$\vec{I_0} = \frac{1}{3}(\vec{IA} + \vec{IB} + \vec{IC})$ E71169A

Input and output signals

Table 261 - Input signals of the 3ph CT group (*PHTCTT*)

Name	Short label	Infotip
ZeroIn	Zero	Outputs forced to zero with good quality
ReversalIn	Reversal	Outputs swapped in accordance with bay reversal setting
Fault	CT fault	Quality of outputs set to invalid

NOTE: Reversal will swap the phases in accordance with the Reversal setting in Bay configuration.

Table 262 - Input signals of the 1ph CT group (*TCTS*)

Name	Short label	Infotip
ZeroIn	Zero	Outputs forced to zero with good quality

Setting parameters

Table 263 - Settings of the 3ph CT group (*PHTCTT*)

Name	Short label	Infotip	Setting range	Step size	Default setting
CTCon	Connection type	CTs connected to the function. IN should be summated if used	• IA IB IC • IA IB IC IN • IA IC • IA IC IN		IA IB IC
ARtg	Rated current	Rated primary current	1...30000 A	1 A	100 A
ARtgSec	Secondary	Rated secondary current	1...5 A	1 A	1 A
NbChIA	IA	IA	0...9999	1	9999
NbChIB	IB	IB	0...9999	1	9999
NbChIC	IC	IC	0...9999	1	9999
NbChIN	IN	IN	0...9999	1	9999
PhaseCTpol	Phase polarity	Phase CT polarity	• Standard • Opposite		Standard
INCTpol	Neutral polarity	IN CT polarity	• Standard • Opposite		Standard
Cutoff	Cutoff current	Measurements below this value are forced to zero	0.0001...0.02 pu	0.0001 pu	0.001 pu

NOTE: Reversal phase swap is in Bay configuration.

Table 264 - Settings of the 1ph CT group (*TCTS*)

Name	Short label	Infotip	Setting range	Step size	Default setting
CTCon	Connection type	CT connected to the function	• IA • IB • IC • IN		IN
ARtg	Rated current	Rated primary current	1...30000 A	1 A	100 A
ARtgSec	Secondary	Secondary	1...5 A	1 A	1 A
NbChIx	Ix	Ix	0...9999	1	9999
CTpol	Polarity	CT polarity	• Standard • Opposite		Standard
AngCor	Angle correction	Correction angle for CT errors	-30...30 deg	0.1 deg	0 deg
Cutoff	Cutoff current	Measurements below this value are forced to zero	0.0001...0.02 pu	0.0001 pu	0.001 pu

NOTE: All functions receiving measurements from the *TCTS* will receive currents with the corrected angle.

Characteristics

Table 265 - Characteristics of the current measurement

Characteristics		Values
Phase current	Measurement range	0.001...40 pu
	Unit	A
	Resolution	0.0001 pu
	Accuracy	±0.1% or ±0.1mA (0.001...40 pu) (symmetrical waveforms)
Phase angle	Range	-180°...+180°
	Resolution	0.1°
	Accuracy	±0.5° for range 0.01...0.05 pu ±0.1° for range 0.05...40 pu
Neutral current	Measurement range	IN calculated: 0.01...40 pu IN measured by 1 A / 5 A CT: 0.01...40 pu IN measured by 1 A core balance CT: 0.002...4 A
	Unit	A
	Resolution	0.0001 pu
	Accuracy, IN	Calculated by standard CT: ±0.1% or ±0.1 mA (0.01...40 pu) symmetrical waveforms Measured by standard CT: ±0.1% or ±0.1 mA (0.001...40 pu) symmetrical waveforms Measured by core balance CT: ±0.1% or ±0.1 mA (0.001...4 pu)

VT group

Description

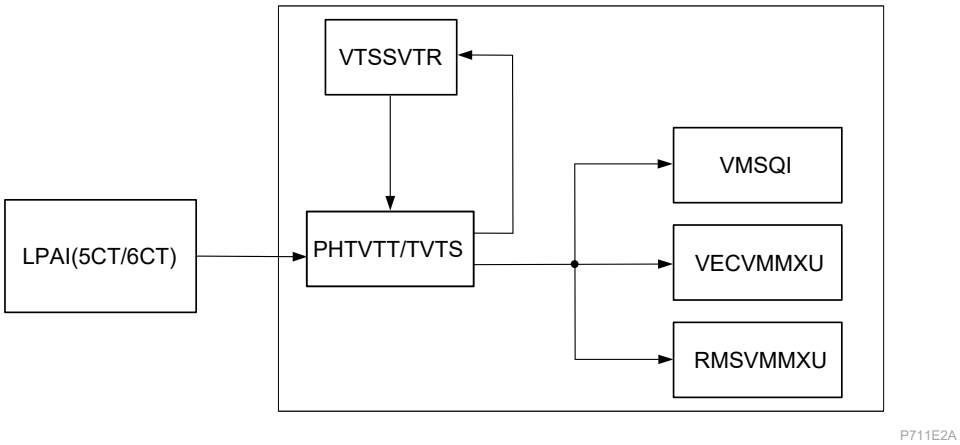
The VT group consists of measurement function blocks (RMS, fundamental and sequence), voltage transformer supervision (*VTSSVTR*) and VT model (*PHTVTT* or *TVTS*). The VT group supports both phase-to-ground and phase-to-phase inputs and measurements.

The VT group maps the physical channels from the Low Power Analog Input (LPAI) module or the digital channels from SV subscriptions to group's voltage which are used by the installed application functions.

On the HMI, the VT group measurements can be viewed under **General > Bay x > 3ph VT x** or **1ph VT x > Measurements**.

NOTE: 3ph VT 1 measurements are used as the inputs for **Measurements > Bay x > General**.

Figure 185 - Function block of VT group



Each bay can have various numbers of VT groups dependent on the application level. Two types of VT group are available.

- 3ph VT group is used to handle multiple phases with or without neutral voltage signals.
- 1ph VT group is used to handle single phase voltage signals. It does not have supervision or sequence measurements.

Rating

For the VT groups mapped to physical channels, the LPAI's input is a secondary value, the LPAI's output is a PU value according to the secondary configuration in *PHTVTT* or *TVTS*. Primary values are calculated based on the PU value and primary rating. PU values and primary values are available for use in protection and measurement functions.

For the VT groups mapped to SV channels, the PU value is calculated based on the primary rating in the associated *PHTVTT* or *TVTS* and the primary value, which is received from SV subscriptions.

Connection type

Different connection types are given for the different VT connections available. 3ph (VA VB VC) should be used with three single phase VTs or a five limb VT. 3ph +N (VA VB VC VN) should be used with VTs with one star and one broken delta secondary. 2pp (VAB VCB) is for two winding or vee connected VTs. 2pp+N (VAB VCB VN) is for two winding VTs when a separate neutral measurement is available such as a generator star point. The connected phase, phase-to-phase or neutral can be selected for 1ph VT groups. It will be marked as valid and other signals marked as invalid. Connected functions will check the quality and will be blocked if the required signals are not available. Detailed quality output is shown in following truth tables.

NOTE: In the table, the Measured and Derived symbols indicate the quality of the signal is GOOD, Measured means that the output signal is directly calculated from the input signal, Derived means that the output signal is calculated from multiple Measured signals.

Table 266 - Quality relationship between 3ph VT group and vector voltage outputs

VT connection type	Physical inputs				Vector voltage						
	VA	VB	VC	VN	VA	VB	VC	VAB	VBC	VCA	VN
3ph	VA	VB	VC	N/A	Measured	Measured	Measured	Derived	Derived	Derived	Derived
3ph+N	VA	VB	VC	VN	Measured	Measured	Measured	Derived	Derived	Derived	Measured

Table 266 - Quality relationship between 3ph VT group and vector voltage outputs (Continued)

2pp+N	VAB	VCB	N/A	VN	Derived	Derived	Derived	Measured	Measured	Derived	Measured
2pp	VAB	VCB	N/A	N/A	Invalid	Invalid	Invalid	Measured	Measured	Derived	Invalid

Table 267 - Quality relations between 3ph VT group and sequence voltage output

VT connec-tion type	Physical inputs				Sequence vector voltage		
	VA	VB	VC	VN	V0	V1	V2
3ph	VA	VB	VC	N/A	Derived	Derived	Derived
3ph+N	VA	VB	VC	VN	Derived	Derived	Derived
2pp+N	VAB	VCB	N/A	VN	Derived	Derived	Derived
2pp	VAB	VCB	N/A	N/A	Invalid	Derived	Derived

Table 268 - Quality relations between 3ph VT group and RMS voltage output

VT con-nection type	Physical inputs				RMS voltage						
	VA	VB	VC	VN	VARMS	VBRMS	VCRMS	VABRMS	VBCRMS	VCARMS	VNRMS
3ph	VA	VB	VC	N/A	Measured	Measured	Measured	Derived	Derived	Derived	Derived
3ph+N	VA	VB	VC	VN	Measured	Measured	Measured	Derived	Derived	Derived	Measured
2pp+N	VAB	VCB	N/A	VN	Derived	Derived	Derived	Measured	Measured	Derived	Measured
2pp	VAB	VCB	N/A	N/A	Invalid	Invalid	Invalid	Measured	Measured	Derived	Invalid

Quality for single phase VT group

Quality for single phase VT group is based on the incoming quality status.

Table 269 - Quality relationship between 1ph VT group and vector voltage outputs

VT connec-tion type	Physical inputs				Vector voltage						
	VA	VB	VC	VN	VA	VB	VC	VAB	VBC	VCA	VN
Aph	VA	N/A	N/A	N/A	Measured	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
Bph	N/A	VB	N/A	N/A	Invalid	Measured	Invalid	Invalid	Invalid	Invalid	Invalid
Cph	N/A	N/A	VC	N/A	Invalid	Invalid	Measured	Invalid	Invalid	Invalid	Invalid
ABph	VAB	N/A	N/A	N/A	Invalid	Invalid	Invalid	Measured	Invalid	Invalid	Invalid
CBph	N/A	VCB	N/A	N/A	Invalid	Invalid	Invalid	Invalid	Measured	Invalid	Invalid
Nph	N/A	N/A	N/A	VN	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Measured

Table 270 - Quality relationship between 1ph VT group and sequence vector & complex voltage outputs

VT connection type	Physical inputs				Sequence vector voltage		
	VA	VB	VC	VN	V0	V1	V2
Aph	VA	N/A	N/A	N/A	Not available		
Bph	N/A	VB	N/A	N/A			
Cph	N/A	N/A	VC	N/A			
ABph	VAB	N/A	N/A	N/A			
CBph	N/A	VCB	N/A	N/A			
Nph	N/A	N/A	N/A	VN			

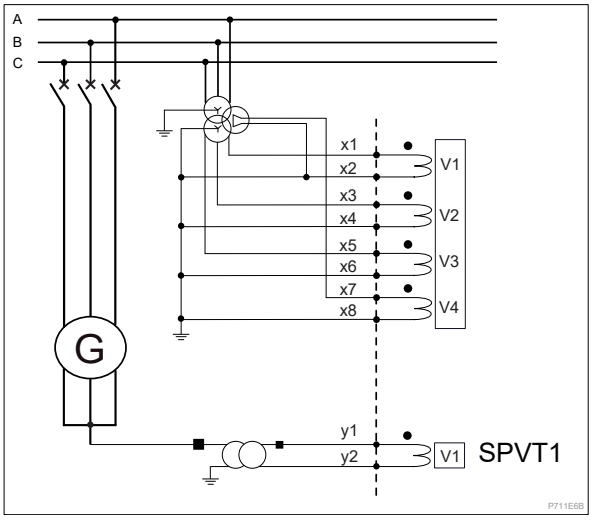
Table 271 - Quality relationship between 1ph VT group and RMS voltage outputs

VT connec-tion type	Physical inputs				RMS voltage						
	VA	VB	VC	VN	VARMS	VBRMS	VCRMS	VABRMS	VBCRMS	VCARMS	VNRMS
Aph	VA	N/A	N/A	N/A	Measured	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
Bph	N/A	VB	N/A	N/A	Invalid	Measured	Invalid	Invalid	Invalid	Invalid	Invalid
Cph	N/A	N/A	VC	N/A	Invalid	Invalid	Measured	Invalid	Invalid	Invalid	Invalid
ABph	VAB	N/A	N/A	N/A	Invalid	Invalid	Invalid	Measured	Invalid	Invalid	Invalid
CBph	N/A	VCB	N/A	N/A	Invalid	Invalid	Invalid	Invalid	Measured	Invalid	Invalid
Nph	N/A	N/A	N/A	VN	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Measured

VT application instance

A typical VT application scenario is shown in the figure below. To implement this application, one 3ph VT group and one 1ph VT group are required. The 3ph VT group corresponds to the 3ph voltage and the open-delta voltage at the generator terminal, and the connection type is 3ph+N. The 1ph VT group corresponds to the neutral voltage at the generator neutral point and the connection type is Nph.

Figure 186 - VT application scenario



x: The first slot used by the CT/VT analog module takes 2 slots. For example, if the analog module is fitted in slots B & C then x1 becomes B1.

y: The CT/VT analog module takes 2 slots. For example, if the analog module is fitted in slots D & E then y1 becomes D1.

Phase voltages

The PowerLogic P7 measures the fundamental values and RMS values of phase-to-phase voltages and phase-to-ground voltages.

The calculation is performed as follows and is computed over a frequency tracked cycle with n=48.

$$V_{RMS} = \sqrt{\frac{1}{n}\sum_{k=1}^{n} V_k^2}$$

E71184A

Neutral voltage

VN can be measured directly if the main transformer includes a broken delta secondary. Alternatively, VN is calculated by taking the internal sum of the three phase-to-ground voltages.

$VN = VA + VB + VC$

Sequence voltage

The sequence voltage value is based on three-phase voltages connected to the VT.

The calculation is performed as follows:

Table 272 - The formula of phase rotation

Phase rotation	Formula
ABC	$\vec{V_1} = \frac{1}{3}(\vec{VA} + \alpha\vec{VB} + \alpha^2\vec{VC})$ E71165A
	$\vec{V_2} = \frac{1}{3}(\vec{VA} + \alpha^2\vec{VB} + \alpha\vec{VC})$ E71178A
	$\vec{V_0} = \frac{1}{3}(\vec{VA} + \vec{VB} + \vec{VC})$ E71162A
ACB	$\vec{V_1} = \frac{1}{3}(\vec{VA} + \alpha^2\vec{VB} + \alpha\vec{VC})$ E71163A
	$\vec{V_2} = \frac{1}{3}(\vec{VA} + \alpha\vec{VB} + \alpha^2\vec{VC})$ E71164A
	$\vec{V_0} = \frac{1}{3}(\vec{VA} + \vec{VB} + \vec{VC})$ E71162A

Table 273 - The formula of phase rotation in 2pp mode

Phase rotation	Formula
2pp_ABC	$\vec{V_1} = \frac{1}{3}(\overrightarrow{VAB} + \alpha^2\overrightarrow{VCB})$ E71179A
	$\vec{V_2} = \frac{1}{3}(\overrightarrow{VAB} + \alpha\overrightarrow{VCB})$ E71180A
	$\vec{V_0} = \frac{1}{3}(\vec{VA} + \vec{VB} + \vec{VC})$ E71162A
2pp_ACB	$\vec{V_1} = \frac{1}{3}(\overrightarrow{VAB} + \alpha\overrightarrow{VCB})$ E71181A
	$\vec{V_2} = \frac{1}{3}(\overrightarrow{VAB} + \alpha^2\overrightarrow{VCB})$ E71182A
	$\vec{V_0} = \frac{1}{3}(\vec{VA} + \vec{VB} + \vec{VC})$ E71162A

NOTE: The calculation of V_0 is only valid in 2pp+N mode, not valid in 2pp mode.

Angle reference

If VA > 0.02 pu, then VA voltage angle will be the reference for other signal angles. If VA is lost, the V1 will become the reference. If all voltages are lost, then IA current angle will be the reference. If IA is also lost, then I1 will be the reference

Input and output signals

Table 274 - Input signals of 3ph VT group (*PHTVTT*)

Name	Short label	Infotip
ZeroIn	Zero	Outputs forced to zero with good quality
ReversalIn	Reversal	Outputs swapped in accordance with bay reversal setting
Fault	VT fault	Quality of outputs set to invalid

Table 275 - Output signals of 3ph VT group (*PHTVTT*)

Name	Short label	Infotip
FuFail	Fuse Fail	Active when fail input is present

Table 276 - Input signals of 1ph VT group (*TVTS*)

Name	Short label	Infotip
ZeroIn	Zero	Outputs forced to zero with good quality
Fault	VT fault	Quality of outputs set to invalid

Table 277 - Output signals of 1ph VT group (*TVTS*)

Name	Short label	Infotip
FuFail	Fuse fail	Active when fail input is present

Setting parameters

VT secondary is always set in terms of system or phase-phase rating.

Table 278 - Settings of 3ph VT group (*PHTVTT*)

Name	Short label	Infotip	Setting range	Step size	Default setting
VTCon	Connection type	VT phases connected to the function. VN should be from the same VT	• VA VB VC • VA VB VC VN • VAB VCB VN • VAB VCB		VA VB VC
VRtg	Rated voltage	Rated phase to phase voltage	100...1e+06 V	1 V	5000 V
VRtgSec	Secondary	Rated phase to phase secondary voltage	100...480 V	1 V	100 V
VRtgSecN	Neutral secondary	Equivalent phase to phase rated neutral secondary voltage	100...480 V	1 V	100 V
Cutoff	Cutoff voltage	Measurements below this value are forced to zero	0.001...0.02 pu	0.0001 pu	0.005 pu
NbChV1	VA/VAB	VA/VAB	0...9999	1	9999
NbChV2	VB/VCB	VB/VCB	0...9999	1	9999
NbChV3	VC	VC	0...9999	1	9999
NbChV4	VN	VN	0...9999	1	9999

NOTE: Reversal is in Bay configuration.

Table 279 - Settings of 1ph VT group (*TVTS*)

Name	Short label	Infotip	Setting range	Step size	Default setting
VTCon	Connection type	VT phase connected to the function	• VA • VB • VC • VAB • VCB • VN		VN
VRtg	Rated voltage	Rated voltage	100...1e+06 V	1 V	5000 V
VRtgSec	Secondary	Rated secondary voltage. Must be on same basis as primary (ph-ph or ph-n)	100...480 V	1 V	100 V
Cutoff	Cutoff voltage	Measurements below this value are forced to zero	0.001...0.02 pu	0.0001 pu	0.005 pu
NbChVx	Vx	Vx	0...9999	1	9999

Characteristics

Table 280 - Characteristics of the voltage measurement

Characteristics		Values
Secondary voltage	Measurement range	0...500 V
	Unit	V
	Resolution	0.001 V
	Accuracy	±0.1% or ±10 mV (0.5...500 V) Nominal frequency: 50 Hz or 60 Hz
Phase angle	Range	-180°...+180°
	Resolution	0.01°
	Accuracy	0.1° (46...300 V) 2.5° (3...500 V)

NOTE: RMS measurements up to 10th harmonic.

CT/VT matrix

Before any analog signal from the CT/VT module(s) can be used, the related hardware or Sampled Value (SV) channels need to be mapped to the virtual channels of the CT/VT group(s). This can be done with the PowerLogic Engineering Suite only. The mapping relationship should match the external wiring of substation CTs and VTs to the different physical inputs of the CT/VT module. Configure different physical analog channels to different groups.

In the PowerLogic Engineering Suite, the mapping of the analog channel is performed within the CT and VT Group. For example, the mapping of the three phase CTs can be configured under **Bay 1 configuration > Three phase CTs > 3ph CTx > Scaling**. The signals are mapped by reference to the instance number of the module and the signal of the voltage or current input on the board; for example, 6CT1 VT1.

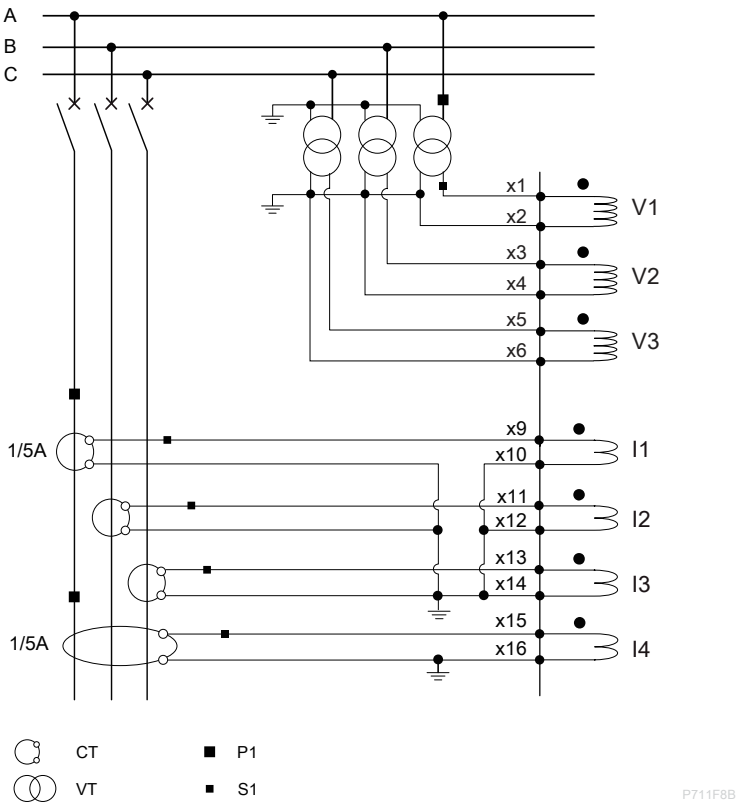
NOTE:

- If SV subscriptions are configured, the CT/VT groups can be mapped to the digital channels of received SVs with the PowerLogic Engineering Suite. The group settings of *Rated current* or *Rated voltage* must match the received SVs.
- The mix of channels from different SV streams, or the mix of physical acquisitions and SV channels are not allowed within the same three phase CT/VT group.
- If SV subscriptions are configured, the sampling rate of local CT/VT acquisition is forced to 4800 Hz (same as the subscribed SV) for better synchronization. Then all local and SV signals are resampled to 48 samples per cycle.
- For protection functions using SV signals as input, the start time will increase by 2-4 ms.

On the HMI, the connected hardware/SV channel is indicated in the CT/VT group settings. For example, the connected hardware channel of three phase VT 1 can be viewed under ☰ **> General > Bay 1 > 3ph VT 1 > Measurements > Settings**. The first digit represents the slot with the CPU as slot 0. The next two digits indicate the channel with *I1* as channel 00 and *V1* as channel 06. For example, VT1 on an analog board in slot BC will be channel 206.

For the application scenario shown in the figure below, CT1 sensor connection type should be set as 3ph (IA IB IC), mapping IA with PHCT1, IB with PHCT2, IC with PHCT3, single CT is mapped with PHCT4. VT1 package connection type should be set as VA VB VC, mapping VA/VAB with VT1, VB/VCB with VT2, VC with VT3.

Figure 187 - Application scenario



- Wiring diagrams represent the protection and control device not energized.
- Default connections are shown.
- The terminal reference x refers to the first slot used by the first analog module which takes 2 slots. For example, if the first analog module is fitted in slots B & C then x1 becomes B1.

Sampled values

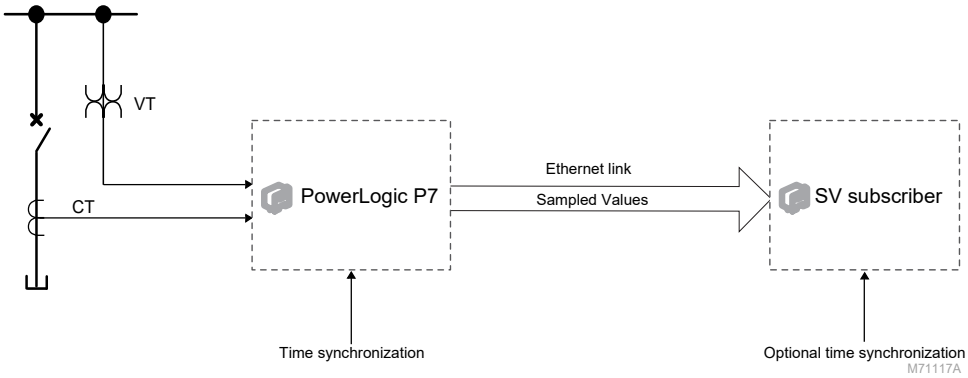
Sampled value publication

Description

The SV publishing function is available on all PowerLogic P7S devices which can be configured to publish SV in accordance with IEC 61869-9 class d standard. Other devices in the PowerLogic P7 range may also be able to publish SV depending upon their main application and application level.

The SV publisher converts the analog currents/voltages from conventional CT/VTs to Sampled Values (SVs), time-tags the SVs, then transmits the SVs over a common Ethernet network to SV subscribers for various protection, control, measurement, and monitoring purposes.

Figure 188 - SV publication on PowerLogic P7



SV publisher characteristics

SV acquisition

The multicast sampled value control block (MSVCB) defines the sampling parameters and includes the dataset to be published, which specifies a selection of current/voltage channels with their individual quality. The number of SV streams and publishing rate are dependent on the device type.

At every sampling instant, the MSVCB collects the values of all current/voltage channels in the dataset within an ASDU (Application Service Data Unit).

The MSVCB defines the number of ASDUs (up to 6) contained in each published SV frame.

SV synchronization

When an SV subscriber compares the SVs sent by different SV publishers, or compares SVs with physical CT/VT acquisitions, the published SVs must be synchronized. The SV publisher uses an external IEEE 1588 (PTP) or IRIG-B clock as the synchronization reference. Other methods of time synchronization are not sufficiently accurate.

Each ASDU is tagged with its sample counter (*SmpCnt*) and synchronization status (*SmpSynch*). The *SmpCnt* is an incremental value that codes the specific moment each ASDU is captured, while the *SmpSynch* indicates the clock time synchronization applied.

The *SmpSynch* can indicate the ASDU as *Globally synchronized*, *Locally synchronized*, or *Not synchronized*. All ASDUs that are synchronized with the same time source are synchronized with each other.

- *Globally synchronized* means the ASDU is synchronized with a global area clock that meets the accuracy requirement.
- *Locally synchronized* means the ASDU is synchronized with a local area clock.
- *Not synchronized* means the ASDU is not synchronized with any of the clocks mentioned above, or has lost the signal from a qualified global or local area clock for longer than the holdover time.

  NOTE: During the holdover time, which starts after the external clock is lost, the device can maintain the time accuracy of the time-tagging for the published samples.

SV transmission

ASDUs are transmitted in streams from the SV publisher to SV subscribers over Ethernet-based network, communicating the primary values of current and voltage to other parts of the substation without the need for additional primary sensors or complex wiring. Each stream corresponds to a configured MSVCB.

The number and type of streams which can be published depend on the main application and application level.

The PowerLogic P7 can only publish SV on its redundant interface (Port 2/Port 3).

Available SV variants

The SV variants that can be published are dependent on the main application and application level:

Application	Available SV variants[13]
Level 1 of motor, generator, feeder and transformer applications	F4800S1-2I4U4
Level 0 of SAMU application	• F4800S1-2I4U4 • F4000S1I4U4 • F5760S1I4U4
Level 1 of SAMU application	• F4800S2I0-24U0-24 • F14400S6I0-8U0-8 • F4000S1I4U4 • F4800S1I4U4 • F5760S1I4U4

Default MSVCB configuration

Applicable PowerLogic P7 devices have a default MSVCB configuration that can be further modified with the PowerLogic Engineering Suite and EPAS-E, both of which are also required for configuring new MSVCBs.

NOTE: For details about configuring SV publications, see the PowerLogic P7 Protection and Control Device Communication User Manual.

Table 281 - Default MSVCB configuration

Parameter	Value
Name	MSVCB03
Dataset	PhsMeas1 (contains TCTR1–4, TVTR1–4)

13.
- F is the digital output sample rate expressed in samples per second
- S is the number of ASDUs (samples) contained in a sampled value message
- I is the number of current quantities contained in each ASDU
- U is the number of voltage quantities contained in each ASDU

Table 281 - Default MSVCB configuration (Continued)

Configuration Revision	1
SMV ID	<name>MU0101 (<name> is the device name in PowerLogic Engineering Suite)
Multicast	Yes
Sample Rate	4800 Hz
Number of ASDU	2
Sample Mod	Samples per seconds
MAC Address	01-0C-CD-04-00-00
Application ID (AppID)	4000
VLAN ID	000
VLAN priority	0

SV monitoring (*LSVP*)

The *LSVP* is used to monitor and diagnose SV publications. One SV publication corresponds to one *LSVP* instance.

After configuring SV publications, the following information can be viewed on an IEC 61850 client installed on a computer connected to the device.

Name	Short label	Infotip
Mod	Mode	Can be used to control whether the SV is published
St	Status	Indicates whether SV are being published
SvCBRef	SV control block	SV control block reference
TmSyn	Time sync level	Indicates internal, local or global sync

Sampled value subscription

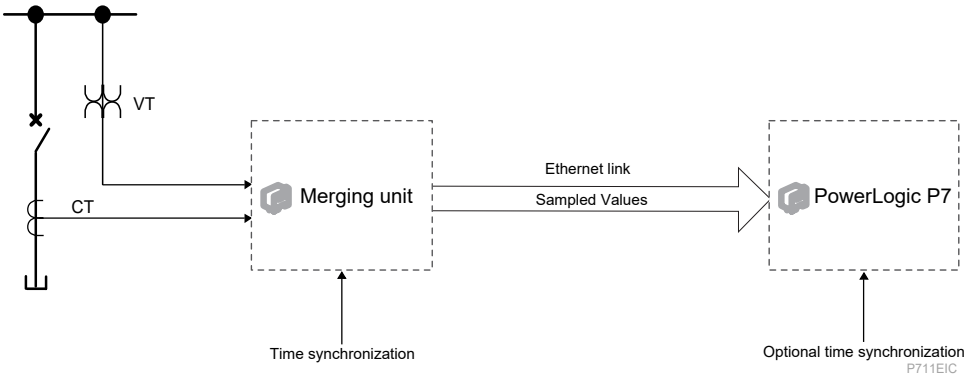
Description

The PowerLogic P7 can source the current/voltage signals from the installed CT/VT boards (local acquisition), subscribed Sampled Value (SV) streams from a remote device (remote acquisition), or a mix of both. From the perspective of later signal processing such as protection or monitoring functions, the PowerLogic P7 does not differentiate between local and remote acquisitions.

The main benefits of remote acquisition are the flexibility and cost-saving it offers to digital substation deployment. The merging unit functionality converts the analog signals acquired from CT/VT into digital SV frames and broadcast them to any other interested IEDs over a common Ethernet network, thus greatly reducing the need for complex copper wirings and multiple primary sensors that a traditional substation relies on for its data acquisition layer. This approach also introduces higher requirements for the network, since a link or switch failure will potentially expose the system to a great outage. In most cases, redundancy is used to help ensure system availability in such scenarios.

The PowerLogic P7 provides the SV subscription functionality through the existing CPU board, allowing the device to subscribe to SVs published by one or more merging units (MU) complying with the IEC 61869-9 standard.

Figure 189 - SV subscription on P7



SV subscriber characteristics

As an SV subscriber, the PowerLogic P7 uses its redundant interface (Port 2/Port 3) to receive SV frames from SV publishers. The number and type of subscriptions are model dependent.

The device can only subscribe to SV streams of 4800 Hz.

Synchronization

Some functions are sensitive to the phase angle differences between different current/voltage sources, which can be multiple MUs, or a mix of MUs and local CT/VT. In such cases, the signals from different sources must be synchronized to each other with a common time reference. The PowerLogic P7 supports IEC 61850-9-3 profile of PTP or IRIG-B for this purpose.

When receiving an SV stream, the device determines its synchronization level with the *SmpSynch* tag and compares with the device's clock level. If they have the same synchronization level, then all the acquisitions are synchronized to each other. Otherwise, when the received SV stream are not synchronized with the device's clock level then the SV stream will be marked as invalid, and all functions using this SV stream will be blocked.

SV mapping

Local and remote acquisitions can be mapped to the available CT/VT groups, which vary depending on the application and are shared between local and remote acquisitions. If a CT/VT group is mapped to one type of acquisition then it cannot be mapped to another.

NOTE: For more information about mapping, see the CT/VT matrix chapter in the PowerLogic P7 Protection and Control Device User Manual.

A three-phase CT/VT group can be mapped to four channels of one single SV stream. The mix of channels from different SV streams, or the mix of local and remote acquisitions are not allowed in a three-phase CT/VT group.

A single phase CT/VT group can be mapped to any channel of an SV stream.

Data quality

An SV stream indicates its quality, synchronization level, and sample capturing time with different tags. The PowerLogic P7 actively monitors these tags and other attributes to determine if the incoming SV stream is acceptable or not.

In the following cases, the SV stream is treated as invalid and the functions requiring the problematic SV stream are temporarily blocked:

- The quality flag of the SV stream changes to *Invalid*.
- The SV stream is lost.

- The received SV stream has invalid synchronization level.
- The SV stream has been delayed beyond the permitted time.
- The received SV stream does not match the requested sampling rate or ASDU quantity.
- The SV stream is being re-synchronized.

SV monitoring (*LSVS*)

The *LSVS* is used to monitor and diagnose SV subscriptions. One SV subscription corresponds to one *LSVS* instance.

After configuring SV subscriptions, the following information can be viewed on an IEC 61850 client installed on a computer connected to the device.

Name	Short label	Infotip
Mod	Mode	Mode
St	Subscription active	Valid messages received
SimSt	Simulation active	Simulation messages are being used
SvCBRef	MSVCB reference	MSVCB reference
TmSyn	Publisher sync level	Time sync level of the received SV
TmSynLkd	Relative sync	The value is locked when the publisher sync level matches the LTMS clock sync and both are local or global. When the levels don't match the value is unlocked and the subscribed SV are marked as invalid

Simulated SV

During commissioning or testing, the device can be configured to process simulated SV streams by setting *Simulation accepted* to *On* (*LPHD.Sim* = *True*) under **Control > Device mode** of the HMI.

When in simulation mode, the device continues treating a normal SV stream as valid until its simulated SV stream is received, after which the device only accepts the simulated SV stream and treats the normal one as invalid until *Simulation accepted* is set to *Off*.

NOTE: Such behavior applies to each subscribed SV stream independently.

Bay measurements

PHTCTT 1 and *PHTVTT* 1 are used as the inputs for the bay measurements. These are used to display the load measurements, power and energy.

Load measurements (*BAYMMXU*)

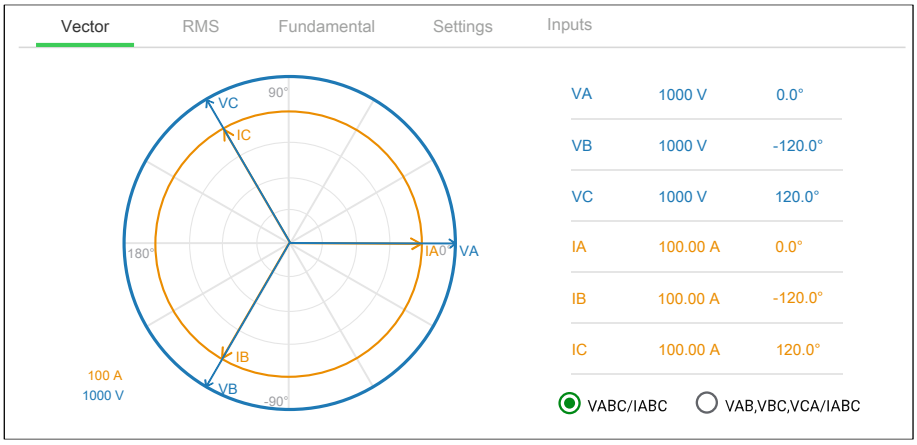
The PowerLogic P7 can provide a graphical view of the voltage and current vectors using a phasor diagram.

From the HMI of the device, expand ☰ **> Measurement > Bay 1 > General**, two options are provided to allow the voltages to be viewed as phase-to-ground or phase-to-phase values.

The choice between phase-to-ground and phase-to-phase voltages can be made using the selector below the measurement table.

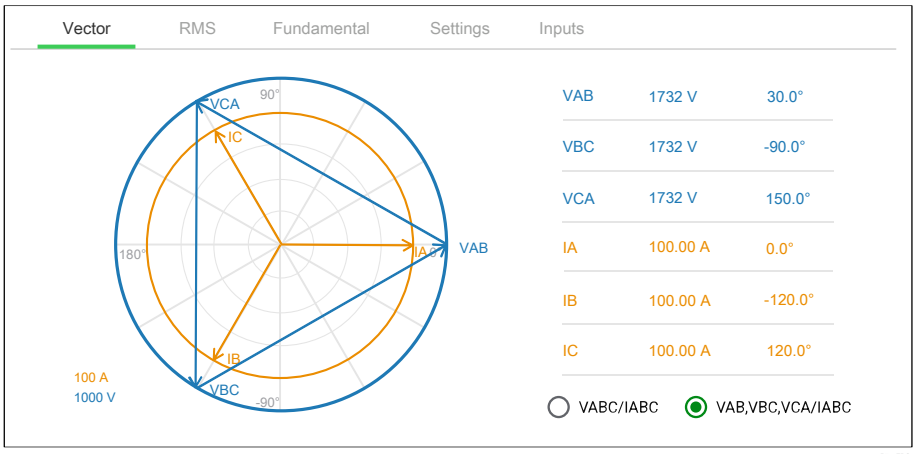
- VABC/IABC

Figure 190 - Phase-to-ground voltage/current



- VAB, VBC, VCA/IABC

Figure 191 - Phase-to-phase voltage/Phase-to-ground current



In both modes, the range of the vectors is indicated by thick lines on the vector diagram.

- The magnitude of the thick lines is shown in the lower left corner of the vector panel.
  - The blue circle indicates the range for the voltage vectors.
  - The amber circle indicates the range for the current vectors.
- The magnitude and angle for each vector displayed is shown in the table to the right of the vector diagram.

Input and output signals

Table 282 - Output signals of the *BAYMMXU*

Name	Short label	Infotip
ARMS	Phase RMS current	Phase RMS current
PPVRMS	Line RMS voltage	Line RMS voltage
PhVRMS	Phase RMS voltage	Phase RMS voltage
TotWRMS	Total RMS power	Total RMS power
WRMS	Phase RMS power	Phase RMS power
TotVArRMS	Total RMS reactive power	Total RMS reactive power

Table 282 - Output signals of the *BAYMMXU* (Continued)

Name	Short label	Infotip
VArRMS	Phase RMS reactive power	Phase RMS reactive power
TotVARMS	Total RMS apparent power	Total RMS apparent power
VARMS	Phase RMS apparent power	Phase RMS apparent power
TotPFRMS	Total RMS power factor	Total RMS power factor
PFRMS	Phase RMS power factor	Phase RMS power factor
A	Current	Current
PPV	Line voltage	Line voltage
PhV	Phase voltage	Phase voltage
Hz	Frequency	Frequency
HzSlope	df/dt	df/dt
TotW	Total power	Total power
W	Power	Power
TotVAr	Total reactive power	Total reactive power
VAr	Reactive power	Reactive power
TotVA	Total apparent power	Total apparent power
VA	Apparent power	Apparent power
TotPF	Total power factor	Total power factor
PF	Power factor	Power factor
PosZ1	Z1	Z1

Setting parameters

Table 283 - Settings of the *BAYMMXU*

Name	Short label	Infotip	Setting range	Step size	Default setting
CmpAng	Power compensation angle	Power compensation angle for 3ph power measurements to correct for CT/VT errors	-20...20 deg	0.1 deg	0 deg

RMS power (*PRMSGAPC*)

Description

The PowerLogic P7 calculates the active, reactive and apparent Root Mean Square (RMS) values of the power system based on the connected currents and voltages. This RMS power measurement function is used in energy measurement and demand value.

The power values are generally calculated as follows:

- Apparent power

$$S_{ARMS} = \sqrt{(P_{ARMS})^2 + (Q_{ARMS})^2}$$

E71183A

S_{BRMS}, S_{CRMS} are calculated similarly.

- Active power

$$P_{ARMS} = \frac{1}{N}\sum_{K=0}^{N-1} V_{Ak} \times I_{Ak}$$ E71124A

V_{Ak} and I_{Ak} represent instantaneous phase-to-ground voltage and current sample values, where N is 48 samples per tracked frequency cycle, P_{BRMS}, P_{CRMS} are calculated similarly.

- Reactive power

For reactive power calculation, the voltages are shifted forward 90 degrees to participate in the calculation.

$$Q_{ARMS} = -(\frac{1}{N}\sum_{k=0}^{N-1} V_{A(k+SampRate/4)} \times I_{Ak})$$ E71125A

$V_{A(k+SampRate/4)}$ represent instantaneous phase-ground voltage which are shifted forward 90 degrees. Q_{BRMS}, Q_{CRMS} can also be calculated similarly.

- Total active power

$$P_{3PhRMS} = \frac{1}{N}\sum_{K=0}^{N-1} V_{ABk} \times I_{Ak} - \frac{1}{N}\sum_{K=0}^{N-1} V_{BCk} \times I_{Ck}$$ E71126A

V_{ABk}, V_{BCk} and I_{Ak}, I_{Ck} represent instantaneous phase-to-phase voltage and current sample values. This is a classical two element wattmeter method which assumes the system is 3 wire.

- Total reactive power

The voltages are shifted forward 90 degrees for the calculation.

$$Q_{3PhRms} = -(\frac{1}{N}\sum_{K=0}^{N-1} V_{AB(k+SampRate/4)} \times I_{Ak} - \frac{1}{N}\sum_{K=0}^{N-1} V_{BC(k+SampRate/4)} \times I_{Ck})$$ E71127B

$V_{AB(k+SampRate/4)}$ and $V_{BC\ (k+SampRate/4)}$ represent instantaneous phase-to-phase voltages which are shifted forward 90 degrees. This assumes the system is 3 wire.

- Total apparent power

$$S_{3PhRMS} = \sqrt{(P_{3PhRms})^2 + (Q_{3PhRms})^2}$$ E71128A

- Power factor

$PF_{ARMS} = P_{ARMS}/S_{ARMS}$, PF_{BRMS}, PF_{CRMS} are calculated similarly.

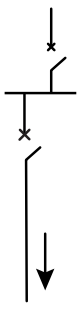
Total power factor is computed as:

$PF_{3PhRMS} = P_{3phRms}/S_{3PhRMS}$

Power direction

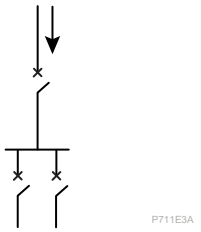
The power direction can be changed to suit the application:

- For the outgoing circuit:
  - Power supplied by the busbars is positive.
  - Power supplied to the busbars is negative.



P711E4A

- For the incoming circuit:
  - Power supplied to the busbars is positive.
  - Power supplied by the busbars is negative.



The positive sign of output indicates the forward flow direction, while the negative sign indicates the backward direction.

Input and output signals

Table 284 - Input signals of the *PRMSGAPC*

Name	Short label	Infotip
IAIBICRms	Phase RMS current	Internal signal from TCTT1
VAVBVCRms	Phase RMS voltage	Internal signal from TVTT1

Table 285 - Output signals of the *PRMSGAPC*

Name	Short label	Infotip
PAPBPCRms	Phase RMS power	Phase RMS power
QAQBQCRms	Phase RMS reactive power	Phase RMS reactive power
SASBSCRms	Phase RMS apparent power	Phase RMS apparent power
P3PhRms	Total RMS power	Total RMS power
Q3PhRms	Total RMS reactive power	Total RMS reactive power
S3PhRms	Total RMS apparent power	Total RMS apparent power
PFAPFBPFCR-ms	Phase RMS power factor	Phase RMS power factor
PF3PhRms	Total RMS power factor	Total RMS power factor

Characteristic

Table 286 - Characteristics of the RMS measurement

Characteristics		Range
Active power	Accuracy	±1% for measurement at 0.8 pu < V < 1.2 pu 0.02 pu < I < 20 pu, cosφ > 0.8
	Resolution	0.01 W
Reactive power	Accuracy	±1% for measurement at 0.8 pu < V <1.2 pu, 0.02 pu < I < 20 pu, cosφ < 0.6
	Resolution	0.01 Var
Apparent power	Accuracy	±1% for measurement at 0.8 pu < V <1.2 pu, 0.02 pu < I < 20 pu
	Resolution	0.01 VA
Factor	Accuracy	0.01 for measurement at Vn, In, cosφ > 0.8
	Resolution	0.001

Fundamental power (*PWRGAPC*)

Description

The power measurement function provides the calculation of active, reactive and apparent powers based on Fourier filter outputs from the voltage and current. This calculation is made based on connected voltages and currents.

This function is used in power measurement based on phasors and power protection (*PPDOP*/*QPDOP* and *PPDUP*) and apparent overpower. A compensation angle can be entered which corrects all fundamental power measurements for known CT and VT angular errors.

- Apparent power

$$S_A = |\overrightarrow{V_A}| \times |\overrightarrow{I_A}|$$

E71129A

The vector of V_A and the vector of I_A represent the phase-to-ground voltage and the phase current complex. S_B and S_C can be calculated in a similar fashion.

- Active power

$$P_A = \overrightarrow{V_A} \times \overrightarrow{I_A} \times \cos(\varphi - CmpAng)$$

E71130A

φ represents the angle of the vector of V_A ahead of the vector of I_A. P_B and P_C can be calculated in a similar fashion.

- Reactive power

$$Q_A = \overrightarrow{V_A} \times \overrightarrow{I_A} \times \sin(\varphi - CmpAng)$$

E71131A

Q_B and Q_C can be calculated in a similar fashion.

- Total 3ph active power

$$P_{3ph} = \overrightarrow{V_{AB}} \times \overrightarrow{I_A} \times \cos(\theta_1 - CmpAng) + \overrightarrow{V_{CB}} \times \overrightarrow{I_C} \times \cos(\theta_2 - CmpAng)$$

E71132A

θ_1 represents the angle of the vector of V_{AB} ahead of the vector of I_A, θ_2 represents the angle of the vector of V_{CB} ahead of the vector of I_C. This is a classical two element wattmeter method which assumes the system is 3 wire.

- Total 3ph reactive power

$$Q_{3ph} = \overrightarrow{V_{AB}} \times \overrightarrow{I_A} \times \sin(\theta_1 - CmpAng) + \overrightarrow{V_{CB}} \times \overrightarrow{I_C} \times \sin(\theta_2 - CmpAng)$$

E71133A

This assumes the system is 3 wire.

- Total 3ph apparent power

$$S_{3ph} = \sqrt{P_{3ph}^2 + Q_{3ph}^2}$$

E71134A

- Power factor

Total power factor is calculated as

$$\frac{P_{3ph}}{S_{3ph}}$$

E71135A

per phase power factor can be calculated as

$$\frac{P_A}{S_A}$$

E71136A

power factor B and power factor C can be calculated in a similar fashion.

Power direction

Refer to Power direction section of Root Mean Square (RMS) power, page 355.

Input and output signals

Table 287 - Input signals of the *PWRGAPC*

Name	Short label	Infotip
IAIBICCplx	Phase complex current	Internal signal from PHTCTT1
VAVBVCCplx	Phase complex voltage	Internal signal from PHTVTT1
UABUBCU-CACplx	Line complex voltage	Internal signal from PHTVTT1
IAIBICVec	Phase current	Internal signal from PHTCTT1
VAVBVCVec	Phase voltage	Internal signal from PHTVTT1

Table 288 - Output signals of the *PWRGAPC*

Name	Short label	Infotip
PAPBPC	Phase power	Phase power
QAQBQC	Phase reactive power	Phase reactive power
SASBSC	Phase apparent power	Phase apparent power
P3Ph	Total power	Total power
Q3Ph	Total reactive power	Total reactive power
S3Ph	Total apparent power	Total apparent power
PF3Ph	Total power factor	Total power factor
PFABC	Phase power factor	Phase power factor

Characteristics

Table 289 - Characteristics of the fundamental power measurement

Characteristics		Range
Active power	Accuracy	±1% Sn typically
Reactive power	Accuracy	±1% Sn typically
Apparent power	Accuracy	±1% Sn typically
Power factor	Accuracy	0.01

Frequency (*FTGAPC*)

Description

The PowerLogic P7 supports 50 Hz and 60 Hz rated frequency. This function determines the frequency based on the samples come from 3ph CT1 (TCTT1) or 3ph VT 1 (TVTT1). The frequency will be automatically adapted to the availability and quality of the related signal inputs:

- If positive sequence voltage V1 ≥ 10 V, the frequency tracking algorithm is based on V1.
- If V1 ≤ 10 V, then if I1 ≥ 0.2 A, the frequency tracking algorithm is based on I1.

- If both V1 < 10 V and I1 < 0.2 A, the frequency will be set to rated frequency.

  NOTE: V1 is the positive sequence voltage calculated from down sampled voltage values, I1 is the positive sequence current calculated from down sampled current value.

When the calculated frequency is out of the range from 10 Hz to 72 Hz, the frequency will be set to rated frequency.

This function also uses the determined frequency to calculate the rate of change of frequency (ROCOF) within a fixed 50 ms measuring window.

Characteristics

Table 290 - Characteristics of the frequency measurement

Characteristics	Range
Measurement range	10...72 Hz
Units	Hz
Resolution	0.001 Hz
Frequency Accuracy	±0.01 Hz
ROCOF Accuracy	±0.05 Hz/s (50 ms measuring window)

NOTE: For measured current and voltage inputs, when the operation frequency range is from 10...39 Hz, the tolerance is ±5%.

Demand values (*DVALMMXU*)

Description

The PowerLogic P7 calculates the average demand values of phase currents IA, IB, IC and power values S, P and Q. They are calculated over an adjustable demand time in a range from 1 to 100 minutes. If the calculated demand is more than the stored maximum demand it will replace that value. If it is less than the stored minimum demand, it will replace that value. If the power is lost, the minimum and maximum values are retained.

The maximum and minimum, demand values can be reset by control command. This will set all measurements to zero and restart the integration period. At the end of the next integration period the minimum and maximum values will be set to the demand values.

Input and output signals

Table 291 - Input signals of the *DVALMMXU*

Name	Short label	Infotip
P3PhRms	Total RMS power	Internal signal from PRMSGAPC1
Q3PhRms	Total RMS reactive power	Internal signal from PRMSGAPC1
S3PhRms	Total RMS apparent power	Internal signal from PRMSGAPC1
ResetIn	Reset	Reset

Table 292 - Output signals of the *DVALMMXU*

Name	Short label	Infotip
MaxDemA	Maximum current	Maximum current
MinDemA	Minimum current	Minimum current
DemA	Last period current	Last period current
MaxDemW	Maximum power	Maximum power
MaxDemVAr	Maximum reactive power	Maximum reactive power
MaxDemVA	Maximum apparent power	Maximum apparent power
MinDemW	Minimum power	Minimum power
MinDemVAr	Minimum reactive power	Minimum reactive power
MinDemVA	Minimum apparent power	Minimum apparent power
DemW	Last period power	Last period power
DemVAr	Last period reactive power	Last period reactive power
DemVA	Last period apparent power	Last period apparent power
ValRs	Reset demands	Reset demands

Setting parameters

Table 293 - Settings of the *DVALMMXU*

Name	Short label	Infotip	Setting range	Step size	Default setting
ClcIntvPer	Calculation interval	The demands are calculated over this period. The period starts from the reset of the function or startup of the IED	60000...6000000 ms	60000 ms	1800000 ms
ClcIntvTyp	Interval unit	Interval unit	• ms • per cycle • cycle • day • week • month • year • external		ms
ClcMod	Calculation mode	Calculation mode	• From reset • Periodic • Sliding window		From reset
ClcMth	Calculation method	Calculation method	• Unspecified • True RMS • Peak fundamental • Fundamental • Minimum • Maximum • Average • Standard Deviation • PREDICTION • RATE		Average

Characteristic

Characteristics		Values
Currents	Accuracy	Refer to Phase current, page 338.
Powers	Accuracy	Refer to RMS power, page 355.

Active and reactive energy (*EMMTR*)

Description

The PowerLogic P7 measures the active and reactive energy values, calculating on basis of the three-phase active power RMS and three-phase reactive power RMS.

If the sign of P_{3PhRMS} is positive,
$\Delta WhDmd = 0$ and $\Delta WhSup = P_{3PhRMS} \times \Delta T$[14]

If the sign of P_{3PhRMS} is negative,
$\Delta WhSup = 0$ and $\Delta WhDmd = |P_{3PhRMS}| \times \Delta T$

And the accumulated active energy is:

$WhSup = WhSup + \Delta WhSup$ (kWh)

$WhDmd = WhDmd + \Delta WhDmd$ (kWh)

The same algorithm is used for reactive energy calculation:

If the sign of Q_{3PhRMS} is positive,
$\Delta VArhDmd = 0$ and $\Delta VArhSup = Q_{3PhRMS} \times \Delta T$

If the sign of Q_{3PhRMS} is negative,
$\Delta VArhSup = 0$ and $\Delta VArhDmd = |Q_{3PhRMS}| \times \Delta T$

And the accumulated reactive energy is:

$VArhSup = VArhSup + \Delta VArhSup$ (kVarh)

$VArhDmd = VArhDmd + \Delta VArhDmd$ (kVarh)

When the maximum storage value exceeds 2^{63} MWh, the output is reset and starts from zero.

In case of power failure, these energy values will be stored in the device and used when next initializing.

Input and output signals

Table 294 - Input signals of the *EMMTR*

Name	Short label	Infotip
P3PhRms	Total P RMS	Internal signal from PRMSGAPC1
Q3PhRms	Total Q RMS	Internal signal from PRMSGAPC1

Table 295 - Output signals of the *EMMTR*

Name	Short label	Infotip
WhSup	Energy supply	Energy supply
WhDmd	Energy demand	Energy demand

14. Time interval input between two execution cycles (ms).

Table 295 - Output signals of the *EMMTR* (Continued)

Name	Short label	Infotip
VArhSup	Reactive energy supply	Reactive energy supply
VArhDmd	Reactive energy demand	Reactive energy demand

Characteristics

Table 296 - Characteristics of the active and reactive energy

Characteristics		Values
Active energy	Accuracy	±1% for measurement at Vn, In, cosφ > 0.8, t > 1 h
	Resolution	1 kWh
Reactive energy	Accuracy	±1% for measurement at Vn, In, cosφ < 0.6, t >1 h
	Resolution	1 kVarh

Measured value supervision

Each measured value has range and quality attributes.

The available states of the range attribute are:

- normal
- high
- low
- high-high
- low-low

The determination of the range value is based on the boundary values:

- **Low-Low Limit**
- **Low Limit**
- **High Limit**
- **High-High Limit**

The boundary values can be configured through **Bay 1 measurement > Ranges > Configuration** in the PowerLogic Engineering Suite.

The available values of the validity in quality are:

- good
- invalid (usually due to a VTS/CTS condition)
- questionable (usually value outside of minimum/maximum range)

NOTE: The measured value with quality **invalid** will be shown in gray on HMI.

In addition, the minimum and maximum values are settable. If the value is below minimum or above maximum, the quality will change to questionable.

NOTE: Deadband range must respect **Minimum ≤ Low-Low Limit ≤ Low Limit ≤ High Limit ≤ High-High Limit ≤ Maximum**.

Figure 192 - Measurement range on HMI

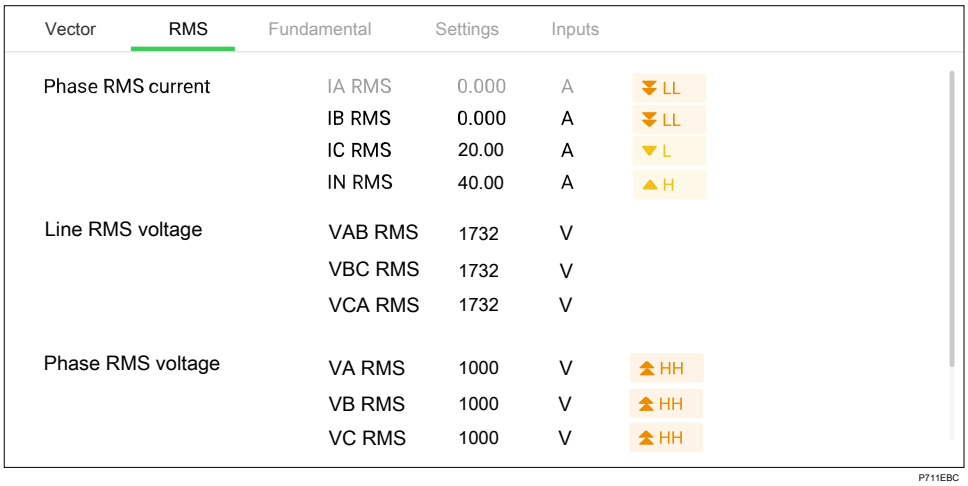


Table 297 - Out of range indicator

Out of range indicator	Description
Min	measured value < **Minimum**
LL	**Minimum** ≤ measured value < **Low-Low Limit**
L	**Low-Low Limit** ≤ measured value < **Low Limit**
H	**High Limit** < measured value ≤ **High-High Limit**
HH	**High-High Limit** < measured value ≤ **Maximum**
Max	measured value > **Maximum**

Analog dead band

For each measurement function block, the dead band of analog values can be set separately. If the changed analog does not exceed the original data plus/minus dead band value, the device will consider the analog has not changed.

Harmonics (*MHAI*)

Description

The harmonics function is applied for power quality analysis, maintenance, and troubleshooting.

This function calculates the magnitude, phase angle, RMS value, and total harmonic distortion (THD) value for three-phase voltage and three-phase current of the 2nd-20th harmonics. Among the calculated results, RMS values and THD values are accessible from the HMI, the PowerLogic Engineering Suite, communication ports and part of logs.

NOTE: Only if the frequency falls within the range of 80% to 120% of the rated frequency are THD values calculated and displayed:

- If the fundamental current is above 1% of the rated current, the THD values of overall, odd, and even harmonics for the 2nd-20th harmonic currents are calculated.
- If the fundamental voltage is above 10% of the rated voltage, the THD values of overall, odd and even harmonics for the 2nd-20th harmonic voltages are calculated. Both line and phase voltage THD values are available.

All calculations are based on three-second measuring windows. Each window itself is aggregated from three one-second slots, each of which comprises one 10-cycle or 12-cycle measurement period depending on the fundamental frequency.

If the line or phase voltage THD value exceeds the configured threshold, an alarm is raised.

A resettable counter records the number of raised THD alarms. If the counter value exceeds the configured threshold, the THD counter alarm is raised.

NOTE: The harmonic measurement of array type is not supported in IEC 61850 Report and GOOSE function, Modbus protocol and DNP3 protocol of P7 devices. For more information, see the *Protocols used and data exchanged* section of PowerLogic P7 Communication User Manual.

Harmonics and THD calculation

Harmonics calculation

The aggregated value for a harmonic current or voltage is calculated with the following equation:

$$RMS_{i3s} = \sqrt{\frac{\left(\sum_{n=0}^{2} (Si)^2\right)}{3}}$$

E71199B

Si is the magnitude of each harmonic in every 10/12 cycles.

THD calculation

The THD is calculated with the following equation:

$$THD = \frac{\sqrt{\sum_{i=2}^{20} (RMS_{i3s})^2}}{RMS_{H1}} \times 100\%$$

E71199A

RMS_{i3s} is the RMS value of the 2-20th harmonic within 3s.

RMS_{H1} is the RMS value of the fundamental.

NOTE: THD calculations for odd and even harmonics are performed in the same manner.

Input and output signals

Table 298 - Input signals of the *MHAI*

Name	Short label	Infotip
CntRs	Reset THD alarm count	Reset THD alarm count

Table 299 - Output signals of the *MHAI*

Name	Short label	Infotip
HA	Current harmonic	Current harmonic
HPhV	Phase voltage harmonic	Phase voltage harmonic
HPPV	Line voltage harmonic	Line voltage harmonic
ThdA	Current THD	Current THD
ThdOddA	Current THD odd	Current THD odd
ThdEvnA	Current THD even	Current THD even
ThdPhV	Phase voltage THD	Phase voltage THD
ThdOddPhV	Phase voltage THD odd	Phase voltage THD odd
ThdEvnPhV	Phase voltage THD even	Phase voltage THD even
ThdPPV	Line voltage THD	Line voltage THD
ThdOddPPV	Line voltage THD odd	Line voltage THD odd
ThdEvnPPV	Line voltage THD even	Line voltage THD even
ThdAlm	THD alarm	THD alarm
ThdCnt	THD alarm counter	Counter for the number of THD alarms
ThdCntAlm	Counter alarm	Counter alarm

Setting parameters

Table 300 - Settings of the *MHAI*

Name	Short label	Infotip	Setting range	Step size	Default setting
ThdVVal	THD alarm value	THD alarm value	1...25 %	0.1 %	8 %
ThdCntVal	Counter alarm value	When the number of THD alarms exceeds this value a count alarm is raised	1...10000	1	10

Characteristics

Table 301 - Characteristics of the MHAI

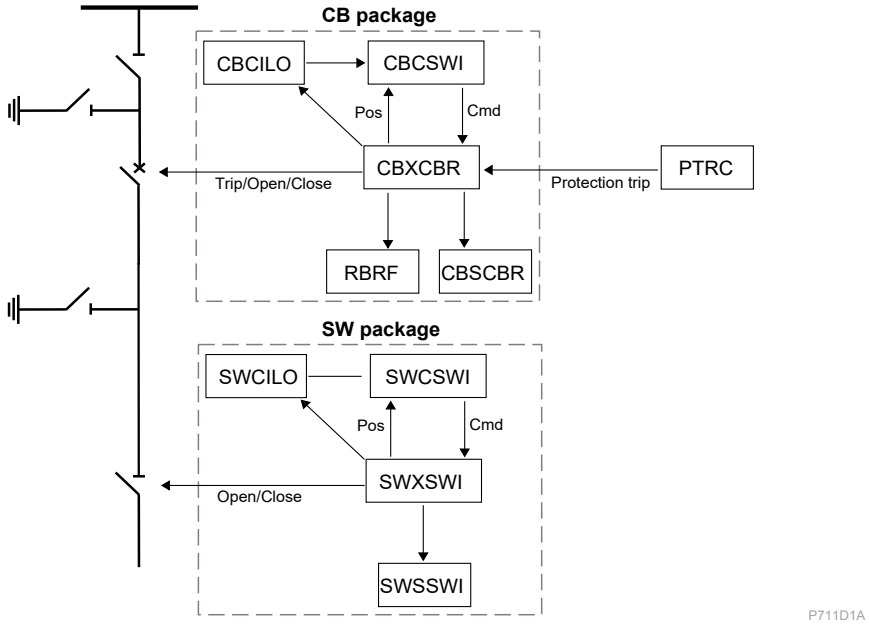
Characteristics		Values
Current harmonic	Accuracy	±5% (only applicable to 2nd-10th harmonic when the sampling rate is 4800 Hz)
Voltage harmonic	Accuracy	±5% (only applicable to 2nd-10th harmonic when the sampling rate is 4800 Hz)

Control functions

General introduction

The PowerLogic P7 provides CB and switch package functions, which can be used to realize CB and switch control and monitoring.

Figure 193 - Bay control overview



The CB package contains the following functions that are needed for three-pole CB control:

- Circuit breaker control (*CBCSWI*)

  Receive local/remote opening and closing orders.

  Manage opening and closing operations.

  Publish CB calculated position.
- Circuit breaker proxy (*CBXCBR*)

  Receive orders from protection functions and CB control.

  Make the CB position available.
- Circuit breaker interlocking (*CBCILO*)

  Check the interlocking.
- Circuit breaker supervision (*CBSCBR*)

  Monitor the CB condition.
- Circuit breaker failure (*RBRF*)

  Retrips or backtrips when a fault condition is not cleared due to failure of the circuit breaker to operate.

The switch package contains the following functions:

- Switch control (*SWCSWI*)

  Receive local/remote opening and closing orders.

  Manage opening and closing operations.

  Publish switch calculated position.
- Switch proxy (*SWXSWI*)

  Receive orders from switch control.

  Make the switch position available.

- Switch interlocking (*SWCILO*)

  Check the interlocking conditions.
- Switch monitoring (*SWSSWI*)

  Monitor the switch.

The PowerLogic P7 can control and monitor one CB and five switches in the basic application level.

Local and remote authority

Before the control command is issued, the control function will check whether the interface is consistent with local and remote authority. This authority is applicable to all CB and switches in one bay.

The control authority is determined by the combination of local key status (***LocKey***), switching authority setting (***MltLev***) and the control authority at station level (***LocSta***). The *LocKey* status can be changed by the virtual function key on front panel or a binary input. The setting *MltLev* is available in each bay. It shows if more than one source of control commands are accepted at a certain level at the same time. The *LocSta* shows the control authority at station level. If *LocSta* is set to *false*, control commands are allowed from remote.

Table 302 - Local and remote authority

Bay control			Command from		
LLN0.LocKey	LLN0.MltLev	LLN0.LocSta	Local control	Station control	Remote control
F	F	F	NA	NA	AA
F	F	T	NA	AA	NA
T	F	N/A	AA	NA	NA
F	T	F	AA	AA	AA
F	T	T	AA	AA	NA
T	T	N/A	AA	NA	NA

N/A = not applicable
AA = always allowed
NA = not allowed

NOTE: *LocSta* is a control object, check the control authority (BayLD0/LLN0/LocInd=True) first to make this object to be configurable on HMI.

CB and switch control (*CBCSWI*/*SWCSWI*)

Description

Control interface

The control function is used to process and manage the CB and switch command issued from any interface:

- Local control from the bay station level using HMI interface.
- Substation control using supported protocols.
- Remote control using supported protocols.
- Direct control via matrix inputs.

Check condition

The following consistency should be verified before sending the command to the local CB and switch.

- Enable opening/enable closing inputs are set by the interlock function *CBCILO*/*SWCILO*.
- Primary equipment control not blocked by process or user command.
- Block opening/block closing are inactive from *CBCSWI*/*SWCSWI*.
- No protection function is tripped.

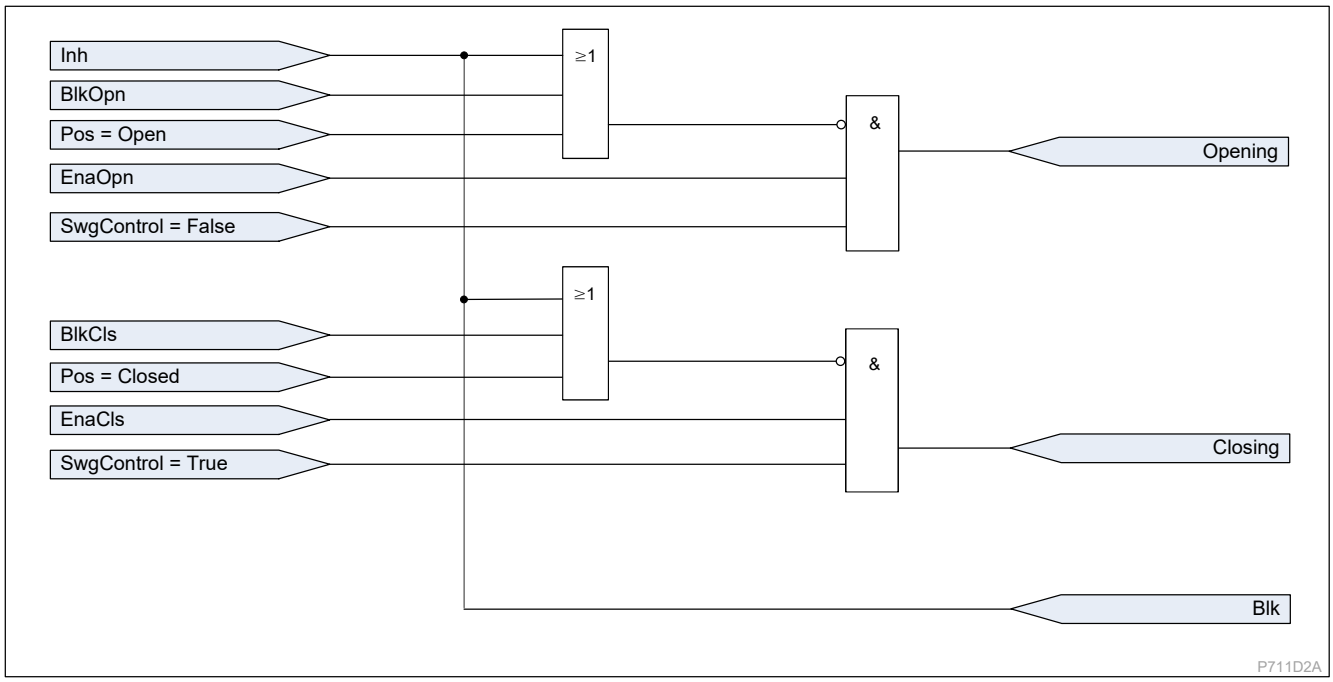
Command logic

Opening command is issued when CB/switch position is *Closed*, *Inhibit* inputs are inactive, *BlkOpn* is inactive, and *EnaOpn* is active.

Closing command is issued when CB/switch position is *Open*, *Inhibit* inputs are inactive, *BlkCls* is inactive, and *EnaCls* is active.

Blk output is set to active when *Inhibit* input is active.

Figure 194 - Command logic



For the control via matrix manual inputs, the bay mode must be *Local* or *Local +Remote*, the control command will be issued on the rising edge of opto input ***OptoOpn***/***OptoCls***, the condition check is same as above logic for HMI control and protocol control.

CB/switch position management

This function is used to provide CB/switch position for reporting and logging.

Generally, it will pass the device position received from *CBXCBR*/*SWXSWI* to the output, except when ***CBPosSup*** is set to *Yes*, *VirtualPos* output of the device only provides *Open* or *Closed*, intermediate status is suppressed.

Take closing control for example, the initial CB position is *Open*, if the closing command is executed successfully, CB position is set to *Closed*. Otherwise, CB position remains *Open* during the ***oper Timeout*** time interval.

Failure reason

This function is used for providing acknowledgements and AddCause for control command.

The authorization sequence is:

1. Authorization from *Inhibit* input check.
2. Authorization from interlocking check.
3. Authorization from protection checks (not applicable to switch).
4. Authorization from blocking inputs (*BlkOpn* and *BlkCls*) check.
5. Authorization from position checks (position valid/position reached/ maintenance position).

AddCause conditions are shown in the table below:

Table 303 - Control function AddCause

AddCause	Description
Blocked-by-Mode	Device mode is different with control command.
None	The result of control is successful.
Time-limit-over	Exceed the *oper Timeout*, control function failure.
Position-reached	The position of object is same with control target.
Invalid-position	CBBadPositon/SwBadPosition or CBIntermediate/ SwIntermediate.
Blocked-by-interlocking	Fail to fulfil the Interlocking condition.
Abortion-by-trip	Protection trip during control process.
Blocked-by-process	The status of *BlkOpn*/*BlkCls* is True.
Not supported	Inhibit is True.
Blocked by Synchrocheck	Synchro-check conditions are out of limit
Command already in execution	Closing process is in progress
Locked by other client	Controllable object already selected
Inconsistent parameters	Controllable object already selected

Input and output signals

Table 304 - Input signals of the *CBCSWI* control

Name	Short label	Infotip
Inh	Inhibit	Inhibit function
OptoCls	Man close	Manual close
OptoOpn	Man open	Manual open
EnaOpn	Enable open	Internal signal from CBCILO
EnaCls	Enable close	Internal signal from CBCILO
BlkOpn	Open blocked	Internal singal from CBXCBR
BlkCls	Close blocked	Internal singal from CBXCBR
CmdBlk	Operation blocked	Control operations blocked
Rel	Sync release	Synchrocheck release
SynOoLim	Sync fail	Synchrocheck fail to start - bypass operation timeout
SynChkByp	Sync bypass	Synchrocheck bypass

Table 304 - Input signals of the *CBCSWI* control (Continued)

Name	Short label	Infotip
AutoOpPrg	External op	External operation - block controls
SwModKeyIn	Local bypass	Bypass interlocks for local (matrix/HMI) operations
SwModKey	Local bypass	Interlocks bypassed for local (matrix/HMI) operations
AutoCls V2.2.1	Auto close	Close from automation function
AutoOpn V2.2.1	Auto open	Open from automation function
ManCmdBlk V2.2.1	Block man ops	Block manual operations

CmdBlk blocks operator control of all controllable objects.

Rel **(*Sync release*)** input allows to authorize close command according to voltage conditions of both sides of the circuit breaker. This can be from an internal or external synchro-check element.

SynChkByp allows to bypass synchro-check for local control.

SynOoLim **(*Sync fail*)** input indicates that synchro-check conditions are out of limits to be able to be synchronized and hence bypasses the synchro-check time out setting. If false (condition ready) at the close command request, CSWI launches the synchro-check timer. This is usually applied when a long synchro-check timer is used for applications such as asynchronous closing and can also be used to provide anti-pumping. It is normally connected using an inverted link to the synchronizer start signal.

SwModKeyIn **(*Local bypass*)** bypasses the interlock for local control only, it is limited to Manual Close or Manual Open (Matrix input *OptoCls*/*OptoOpn*). ***Interlock bypass*** from user control (SPC) is permanent or time limited according the *SwModKey* Control Pulse configuration that can be configured as *Persistent* or *Pulse*.

AutoOpPrg indicates that closing is in progress from automation, and blocks all other controls. This can be connected to any automation function that should block manual commands such as auto-reclose (internal or external).

NOTE:

- If *SynOoLim* = *true* and *Sync release* = *false*, then the close command is immediately rejected (acknowledge negative with add cause = blocked by synchro-check)
- If *SynOoLim*= *false* and *Sync release* remains *false* at the end of synchro-check timeout, then the close command is rejected (acknowledge negative with add cause = blocked by synchro-check)
- If the *SynOoLim* input is not connected, it is considered as *false* (wait for the *Sync release* up to the time out).
- If the *Rel* input is not connected is considered as false.
- If *SynChkEna* is set to *false*, then the synchronism is not checked regardless of whether the synchro-check is requested in control command (control synchro flag is not considered).
- If any of these inputs are invalid, they are considered as false.

Table 305 - Input signals of the *SWCSWI* control

Name	Short label	Infotip
Inh	Inhibit	Inhibit function
OptoCls	Man close	Manual close
OptoOpn	Man open	Manual open
EnaOpn	Enable open	Internal signal from SWCILO

Table 305 - Input signals of the *SWCSWI* control (Continued)

Name	Short label	Infotip
EnaCls	Enable close	Internal signal from SWCILO
BlkOpn	Open blocked	Internal signal from SWXSWI
BlkCls	Close blocked	Internal signal from SWXSWI
CmdBlk	Operation blocked	Control operations blocked
SwModKeyIn	Local bypass	Bypass interlocks for local (matrix/HMI) operations
SwModKey	Local bypass	Interlocks bypassed for local (matrix/HMI) operations
AutoCls V2.2.1	Auto close	Close from automation function
AutoOpn V2.2.1	Auto open	Open from automation function
ManCmdBlk V2.2.1	Block man	Block manual control

Table 306 - Output signals of the *CBCSWI* control

Name	Short label	Infotip
CtlPrg	Control in progress	A control operation is in progress
OpCls	Close signal	Close signal
OpOpn	Open signal	Open signal
Blk	Blocked	Blocked
Loc	Local	Local

Table 307 - Output signals of the *SWCSWI* control

Name	Short label	Infotip
CtlPrg	Control in progress	A control operation is in progress
OpCls	Close signal	Close signal
OpOpn	Open signal	Open signal
Blk	Blocked	Blocked
Loc	Local	Local

Setting parameters

Table 308 - Settings of the *CBCSWI* control

Name	Short label	Infotip	Setting Range	Step Size	Default Setting
CBPosSup	Position filter	Stops intermediate indication during position change	• Off • On		Off
SynChkEna	Synchrocheck	Release input required for closing	• Off • On		Off
SyncTmms	Synchrocheck timeout	Wait time for release	0...600000 ms	1 ms	0 ms

Table 309 - Settings of the *SWCSWI* control

Name	Short label	Infotip	Setting Range	Step Size	Default Setting
SWPosSup	Position filter	Stops intermediate indication during position change	• Off • On		Off

Interlocking (*CBCILO*/*SWCILO*)

Description

The switching commands to the controllable switching devices in the bay are enabled only after interlocking conditions have been checked.

Boolean signals can be mapped to the block inputs via matrix.

The interlocking function only blocks control actions and has no effect on the operation of protection functions.

Interlocking matrix

With the PowerLogic Engineering Suite, navigate to **Bay 1 control > Circuit breaker > CB interlocking** to set up the interlocking matrix.

Interlocking is used to prevent control objects operations based on the status of other equipment. The interlocking function only blocks control actions and has no effect on the operation of protection functions.

The interlocking matrix is used to link binary inputs, virtual inputs, function buttons, protection stage outputs, CB status, grounding switch status, logic outputs, alarm signals and GOOSE signals to inhibit the control of a control object, e.g. a circuit breaker or a grounding switch.

Typical signals to inhibit the control of the objects like circuit breaker are active protection stages, status of other objects, interlocking signals received from the programmable Logic or GOOSE. These and other signals are linked to objects through the object block matrix.

Input and output signals

Table 310 - Input signals of the *CBCILO*/*SWCILO* function

Name	Short label	Infotip
BlkCls	Block close	Block close
BlkOpn	Block open	Block open

Table 311 - Output signals of the *CBCILO*/*SWCILO* function

Name	Short label	Infotip
EnaCls	Enable close	Enable close
EnaOpn	Enable open	Enable open

Characteristics

Table 312 - Characteristics of the *CBCILO*/*SWCILO*

Characteristics	Values
Disengaging time	< 20 ms

Circuit breaker failure (*RBRF*, ANSI 50BF)

Description

The Circuit Breaker Failure (CBF) protection function operates when a fault condition is not cleared due to failure of the circuit breaker to operate when a protection-initiated tripping order is sent. In this case, the CBF function sends a tripping order to the upstream or adjacent circuit breaker to help clear the fault.

In applications where a circuit breaker has two sets of trip coils, the CBF function may send a tripping order to the second set of trip coils (retripping) and if this does not result in fault clearance, the CBF function will then send a tripping order (backtripping) to the upstream or adjacent circuit breaker.

The PowerLogic P7 CBF function has two stages. The retrip stage can be enabled or disabled via a setting and the backtrip stage is always enabled.

The input signals *AInit* and *CBInit* (configured by Matrix) are used to initiate the CBF function depending on the CBF mode setting. By default the trip conditioner output is linked to both inputs and reset based on current or breaker status is determined by the breaker failure detection mode. Selective reset by function can be achieved by setting the detection mode to *Current and CB status* (*52a & I<*) and changing the matrix links. For example, *AInit* is configured to the trip signals from the current related protections (e.g. PTOC, EFOC, NPSOC). *CBInit* is mapped to the trip signals from the non-current related protections (e.g. PTOV, PTUV, PTOF, PTUF). The *AInit* and *CBInit* are pulse inputs and the CBF initiation will be latched once the signals are present for more than 20 ms.

CBF mode

The CBF function may optionally be reset from undercurrent or CB position or a combination of both by means of setting ***FailMod***.

- Undercurrent criterion only mode ***I<***

  The CBF is initiated by *AInit* and *CBInit* is ignored. The CBF timers will be reset by undercurrent check.

- CB position only mode ***52a***

  The CBF is initiated by *CBInit* and *AInit* is ignored. The CBF timers will be reset by CB position.

- Undercurrent and CB position mode ***52a & I<***
  The CBF can be initiated by *AInit* or *CBInit*. When the CBF is initiated by *AInit*, it will be reset by undercurrent check. When the CBF is initiated by *CBInit*, it will be reset by CB position.

Current zero crossing check

For high offset faults after the breaker operates a subsidence current can occur. The secondary current is a decaying DC value with no primary current. The CBF must not operate during these conditions and this is a achieved using a zero crossing check. When current zero crossing detects one sample current is above 1.414×0.015 In and another sample is below -1.414×0.015 In in 3/4 cycle time, a zero crossing is detected. The CBF can only operate when the zero crossing

detector is active indicating the secondary current has crossed zero in the last 3/4 cycle.

CBF logic

The CBF retrip timer and backtrip timer are started by *AInit* or *CBInit*.

While the timers are running, the CBF function can be reset by undercurrent check (initiated by *AInit*) or CB position (initiated by *CBInit*).

When the retrip timer or backtrip timer is expired, some checks are needed before issuing *retrip* or *backtrip* output signal.

- For CBF initiated by *AInit*, the fault current clearance is checked. Following conditions should be met simultaneously:
  - The current zero crossing is detected.
  - Any of the overcurrent checks fulfill. The phase current exceeds the threshold (***PhChkValA***), or the neutral current exceeds the threshold (***NeutChkValA***), or negative sequence current exceeds the threshold (***I2ChkValA***). If one of the current threshold is set to *0*, related checks are all ignored.
  - The phase current exceeds the undercurrent check threshold (***DetValA***).
- For CBF initiated by *CBInit*, the CB position is checked.

  CB is in *Close* status.

A reset delay timer is provided to ensure a minimum trip pulse is issued. This allows direct tripping of breaker trip coils. Alternatively, contacts used for retripping and backtripping can be set as latching. The block diagrams give an overview of the CBF functionality, based on consideration of phase A current for simplicity.

Block diagram

Figure 195 - Block diagram of the *RBRF* with AInit (phase A as an example)

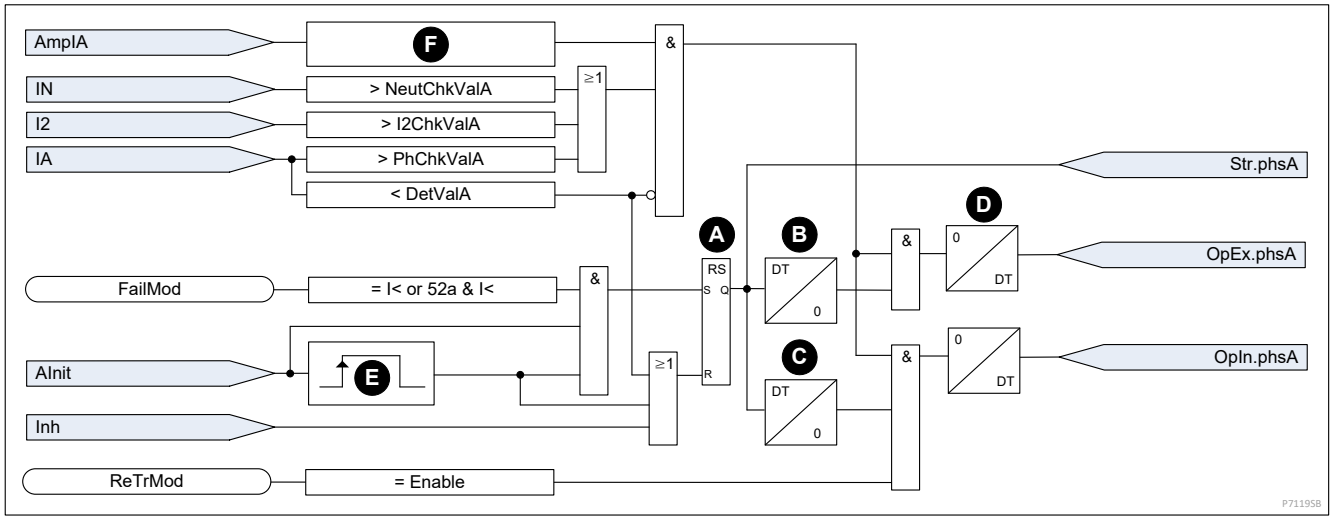
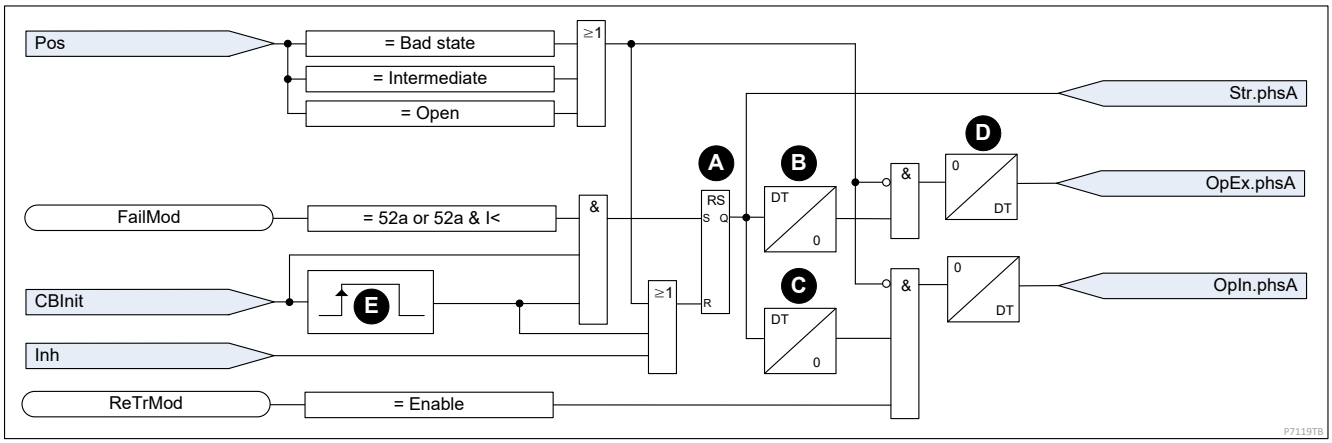


Figure 196 - Block diagram of the *RBRF* with CBInit (phase A as an example)



A	Set dominant	B	Operate delay: *TPTrTmms* Reset delay: 0	C	Operate delay: *FailTmms* Reset delay: 0
D	Operate delay: 0 Reset delay: *RstTmms*	E	Pulse time: 20 ms	F	Current zero crossing check

Input and output signals

Table 313 - Input signals of the *RBRF*

Name	Short label	Infotip
Inh	Inhibit	Inhibit function
AInit	Current init	Initiate current reset CBF
CBInit	Status init	Initiate status reset CBF
IAIBIC	Phase current	Linked to CB routing source
IN	IN	Linked to CB routing source
I2	I2	Linked to CB routing source
Pos	Position	Internal singal from CBXCBR

Table 314 - Output signals of the *RBRF*

Name	Short label	Infotip
Str	Start	Start
StrA	Current start value	Current start value
StrOvPhCur	Phase current check	Phase current Op block
StrZCDPhCur	Zero crossing detector	Zero crossing detector
StrOvNeutCur	Neutral current check	Neutral current Op block
StrOvI2Cur	Neg seq current check	Neg seq current Op block
OpIn	Retrip	Retrip
OpEx	Backtrip	Backtrip
Blk	Blocked	Blocked

Setting parameters

Table 315 - Settings of the *RBRF*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		On
FailMod	Breaker fail mode	Breaker fail mode	• Current • CB status • Current and CB status		Current
ReTripMod	Retrip	Retrip	• Off • On		Off
DetValA	Current start value	Reset current for current mode	0.02...20 pu	0.001 pu	0.2 pu
PhChkValA	Phase current check value	Minimum phase current for current mode. If zero element is always released	0...20 pu	0.001 pu	0 pu
NeutChkValA	Neutral current check value	Minimum neutral current for current mode. If zero element is always released	0...20 pu	0.001 pu	0 pu
I2ChkValA	Neg seq current check value	Minimum negative phase sequence current for current mode. If zero element is always released	0...20 pu	0.001 pu	0 pu
TPTrTmms	Retrip delay	Retrip time delay	0...10000000 ms	1 ms	100 ms
FailTmms	Backtrip delay	Backtrip time delay	0...10000000 ms	1 ms	250 ms
RstTmms	Reset time	Reset time for retrip and backtrip. This provides a minimum pulse to remote trip coils	0...10000000 ms	1 ms	250 ms

Characteristics

Table 316 - Characteristics of the *RBRF*

Characteristics		Values
Phase current check value, Neutral current check value, Neg seq current check value	Accuracy	±5% or ±0.01 A
	Reset ratio	95% ± 5%
Current start value	Accuracy	±5% or ±0.01 A
	Reset ratio	105% ± 5%
Operate delay	Accuracy	2% or ±10 ms
Characteristic time	Disengaging time	< 15 ms
	Overshoot time	<15 ms

Circuit breaker proxy (*CBXCBR*)

Description

The functions of the circuit breaker proxy are shown below:

- Issue CB state information based on CB auxiliary contacts.

- Block control operations when trips are present. The trip signal is also provided as an output allowing trips to be inhibited when required.
- Process the closing/opening request coming from CB control function.
- Count CB operation number.

CB opening and closing logic

1. Protection trip logic

   If trip input is active and either of the *Inhibit* and *BlkOpn* is inactive, trip output is triggered.

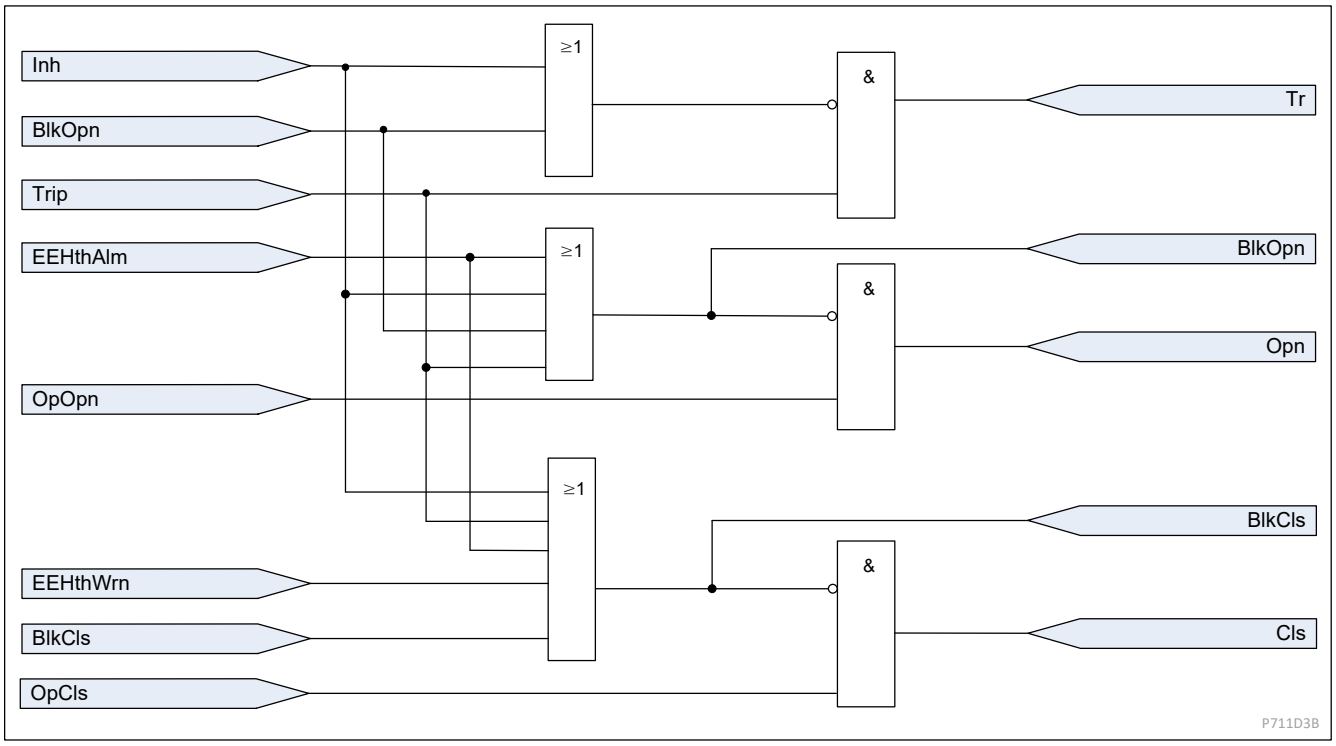
2. Control opening logic

   CB opening will be blocked by *Inhibit*, *BlkOpn*, Protection trip and CB severe problems (*EEHthAlm*).

3. Control closing logic

   CB closing will be blocked by *Inhibit*, *BlkCls*, Protection trip, CB minor problems (*EEHthWrn*) and CB severe problems (*EEHthAlm*).

Figure 197 - Block diagram of the *CBXCBR*



4. Other logic

   If *Inhibit* input is *True*, CB function is blocked, *Blk* output is set to *True*.

   If *EEHthAlm* input is *True*, severe problems are present in the CB, *EEHealth* status is set to *Alarm*.

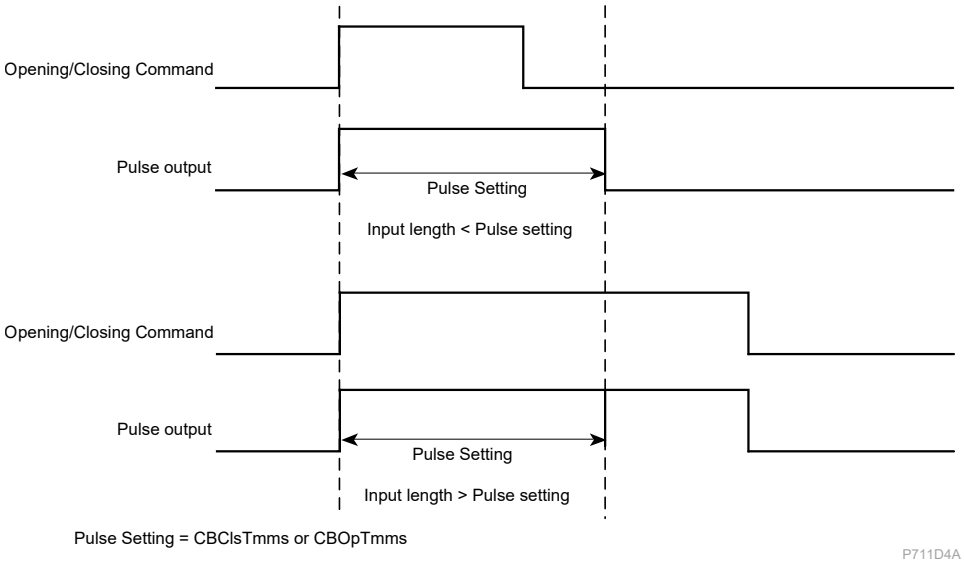
   If *EEHthWrn* input is *True*, minor problems are present in the CB, *EEHealth* status is set to *Warning*.

Opening and closing pulse generation

The PowerLogic P7 provides two pulse modes for CB opening and closing. Protection trip pulse is implemented in PTRC, it is not covered in the circuit breaker function.

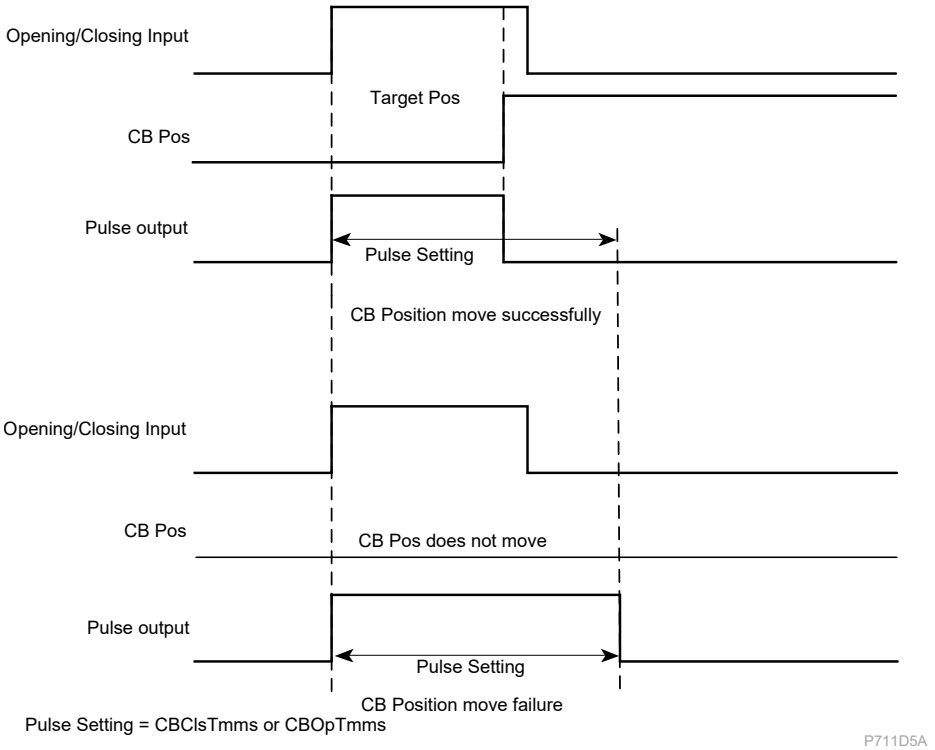
In dwell mode, the minimum pulse length depends on setting *CBClsTmms*/*CBOpTmms*. The maximum pulse length follows the input open/close signals. If the input signal is latched, the output signal will also be latched.

Figure 198 - The time sequence for dwell mode



In status reset mode, the opening/closing pulse will be reset after reaching the target CB position. The maximum length for opening/closing pulse depends on setting *CBClsTmms*/*CBOpTmms*.

Figure 199 - The time sequence for status reset mode



CB position logic

When inhibit input is true, CB position is forcibly set to Open (off), the quality of CB position is valid/substituted. This case assumes the inhibit input is mapped to CB truck status and the status signals will be lost when the breaker is racked out.

When setting *CBAuxM* is *None*, CB position is determined by *BayDead* Status. If *BayDead* is *TRUE*, CB position is *Open* with questionable/inconsistent quality.

When setting *CBAuxM* is *52a*, CB position depends on the status of *52a*, the quality of CB position will inherit the quality of *52a*.

When setting *CBAuxM* is *52b*, CB position depends on the status of *52b*, the quality of CB position will inherit the quality of *52b*.

When setting *CBAuxM* is *Both*, CB position refers to the following table.

Table 317 - The *CBXCBR* position (*CBAuxM = Both*)

52A status	52B status	CB state detected
False	True	Open
True	False	Closed
False	False	Intermediate
True	True	Bad state

The quality of CB position refers to the following table.

Table 318 - The *CBXCBR* position quality (*CBAuxM = Both*)

52A quality	52B quality	CB position quality
Valid	Valid	Valid
Valid	Oscillatory	Questionable/oscillatory
Oscillatory	Valid	Questionable/oscillatory
Oscillatory	Oscillatory	Invalid/oscillatory

Input and output signals

Table 319 - Input signals of the *CBXCBR*

Name	Short label	Infotip
CBAux52b	52b	52b auxiliary contact (closed when CB open)
CBAux52a	52a	52a auxiliary contact (closed when CB closed)
Inh	Inhibit	Can be connected to the truck status. When active the position is forced open with substituted quality
Trip[general]	Trip	Trip (open) breaker
OpOpn	Open signal	Internal signal from CBCSWI
OpCls	Close signal	Internal signal from CBCSWI
BlkCls	Block close	Block breaker closing
BlkOpn	Block open	Block breaker opening
EEHthAlm	CB alarm	CB health alarm (block open and closing)
EEHthWrn	CB warn	CB health warning (block closing)
LocIn	Local	Set breaker to local operation (disable control)
ResetOpCnt	Count reset	Reset operation count
PoleDead	Bay dead	Internal signal from PDGAPC1
ARCls	Auto close signal	Auto close signal

Table 320 - Output signals of the *CBXCBR*

Name	Short label	Infotip
Pos	Position	Position
Loc	Local	Local
Tr	Trip command	Trip command to breaker
Opn	Open command	Open command to breaker
Cls	Close command	Close command to breaker
BlkOpn	Open blocked	Open blocked
BlkCls	Close blocked	Close blocked
EEHealth	Breaker health	Breaker health
OpCnt	Operation count	Operation count
Blk	Blocked	Blocked

Setting parameters

Table 321 - Settings of the *CBXCBR*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		On
CBAuxM	Status input	Used for position. If set to None position will use bay dead signal	• None • 52a • 52b • Both		None
CBCmdM	Command mode	The control signal will be held for at least the pulse time in dwell mode or reset when the position changes in status reset mode	• Dwell • Status reset		Dwell
CBClsTmms	Close pulse time	Close pulse time	100...10000 ms	10 ms	200 ms
CBOpTmms	Open pulse time	Open pulse time	100...10000 ms	10 ms	200 ms
CBTmms	CB closing time	Closing time of the breaker	0...1000 ms	1 ms	50 ms

Switch proxy (*SWXSWI*)

Description

The functions of the switch proxy are shown below:

- Issue switch state information based on the switch auxiliary contacts.
- Process the closing/opening requests coming from switch control function.
- Count the number of switch operations (*OpCnt*).
- Directly control the switchgear motor

Switch opening and closing logic

1. Control opening logic

   Switch opening will be blocked by *Inhibit*, *BlkOpn* and switch severe problems (*EEHthAlm*). The logic diagram of switch control opening is the same with CB control opening.

2. Control closing logic

   Switch closing will be blocked by *Inhibit*, *BlkCls*, switch minor problems (*EEHthWrn*) and switch severe problems (*EEHthAlm*). The logic diagram of switch control closing is the same with CB control closing.

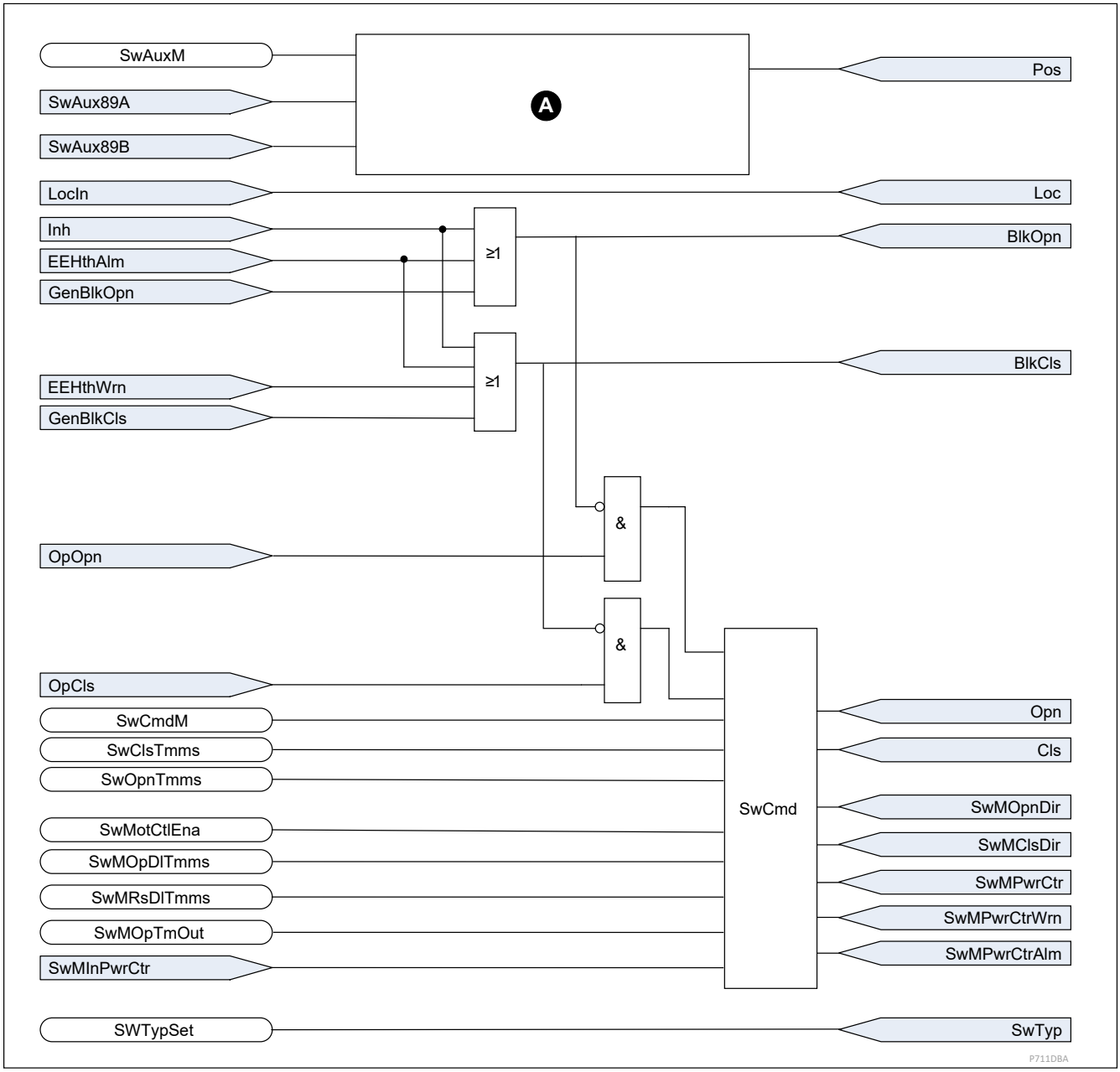
3. Other logic

   If *Inhibit* input is *True*, switch proxy function is blocked, *Blk* output is set to *True*.

   If *EEHthAlm* input is *True*, severe problems exist in the switch, *EEHealth* status is set to *Alarm*.

   If *EEHthWrn* input is *True*, minor problems exist in the switch, *EEHealth* status is set to *Warning*

Figure 200 - Block diagram of the *SWXSWI*



Opening and closing pulse generation

The PowerLogic P7 provides two pulse modes for switch opening and closing. The opening and closing pulse generation is the same as *CBCSWI*.

Switch position logic

When inhibit input is true, switch position is forcibly set to *Open* (*Off*), the quality of switch position is valid/substituted. This case assumes the *inhibit* input is mapped to CB truck status and the switch status signals will also be lost when the breaker is racked out.

When setting ***SwAuxM*** is *None*, switch position is set to *Closed*, the quality of switch position is questionable/inconsistent.

When setting ***SwAuxM*** is *89a*, switch position is decided by the status of 89a, the quality of switch position will inherit the quality of 89a.

When setting ***SwAuxM*** is *89b*, switch position is decided by the status of 89b, the quality of switch position will inherit the quality of 89b.

When setting ***SwAuxM*** is *Both*, switch position refers to the following table.

Table 322 - The *SWXSWI* position (*SwAuxM* = *Both*)

89a status	89b status	Switch state detected
False	True	Open
True	False	Closed
False	False	Intermediate
True	True	Bad state

The quality of switch position refers to the following table.

Table 323 - The *SWXSWI* position quality (*SwAuxM* = *Both*)

89a quality	89b quality	Switch position quality
Valid	Valid	Valid
Valid	Oscillatory	Questionable/oscillatory
Oscillatory	Valid	Questionable/oscillatory
Oscillatory	Oscillatory	Invalid/oscillatory

Open counter

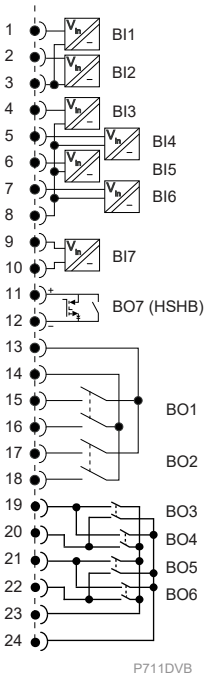
The switch proxy records the number of switch openings.

Switchgear motor direct control

The switchgear motor direct control function is used to directly drive the isolator motor open or closed to change the isolator status. The motor is driven in one direction by positive voltage and the other direction by negative voltage.

This function is enabled by the ***SwMotCtlEna*** setting. The inversion can be easily performed using the Direct Motor Control board which has dedicated motor outputs to invert the applied voltage. For more information, see Slot D, E, F, G: additional direct motor control (DMC) module (7I7O) , page 63.

Figure 201 - Wiring diagram for direct motor control board



Opening and closing pulse generation

Two signals (*SwMOpnDir*/*SwMClsDir*) select the switchgear motor direction. These signals are used to select whether positive or negative voltage is applied to the motor. Each signal can drive 2 standard contacts or dedicated motor contacts on the direct motor control board. After the *Motor op delay* the *Power contactor* signal is raised. This is used to drive an external power contactor or to drive the high break contact on the direct motor control board. These are in series with the direction contacts and are used to make and break the DC current of the isolator motor.

The motor will be driven in the selected direction for a period of time dependent upon whether dwell or status reset mode is selected. In dwell mode, the minimum pulse length depends on setting *SwOpnTmms*/*SwClsTmms*. The maximum pulse length follows the input open/close signals, which would need to be set longer than the maximum possible isolator travel time.

Figure 202 - The time sequence for dwell mode, input length < pulse setting

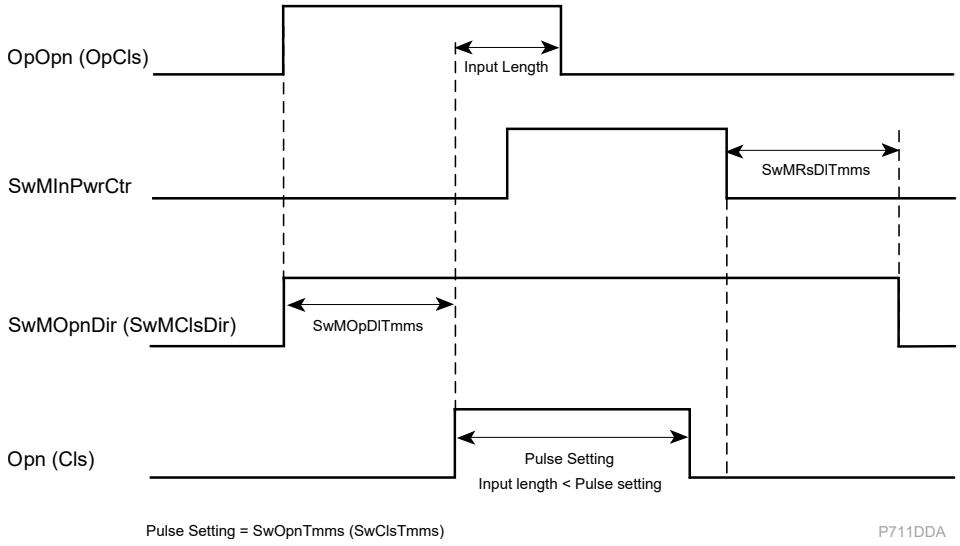
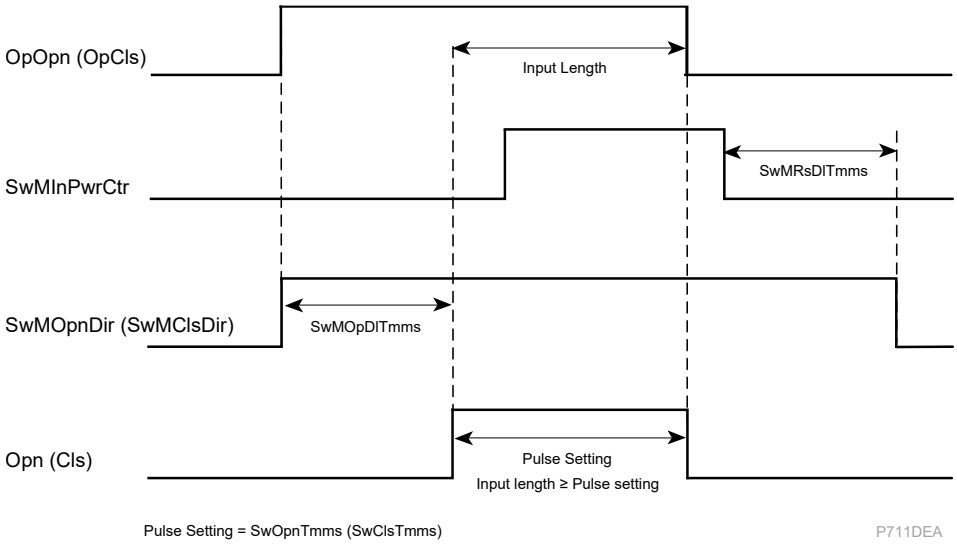


Figure 203 - The time sequence for dwell mode, input length ≥ pulse setting



In status reset mode, the opening/closing pulse will be reset after reaching the target switch position. The maximum length for opening/closing pulse depends on setting *SwOpnTmms*/*SwClsTmms*.

Figure 204 - The time sequence for status reset mode, switch position successfully moves

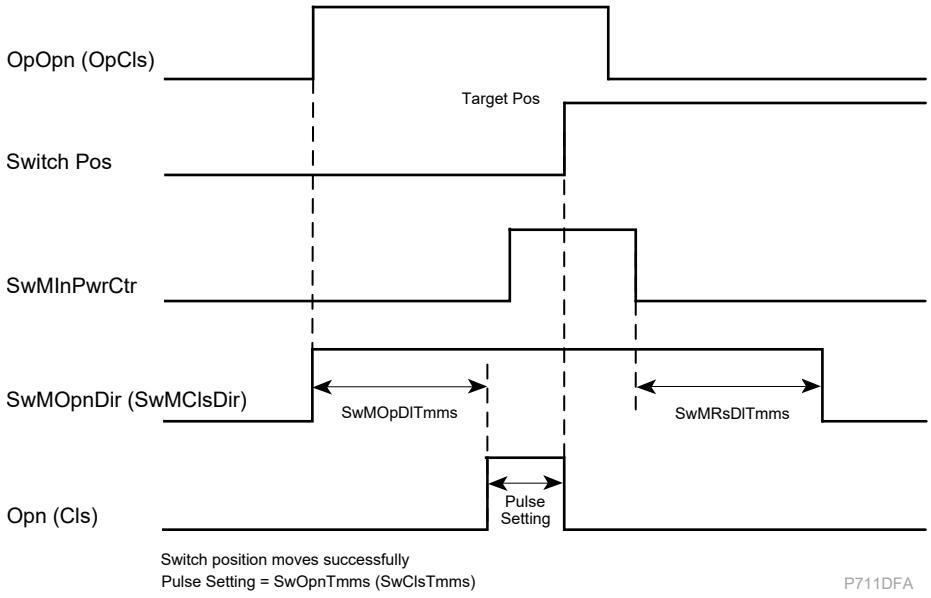
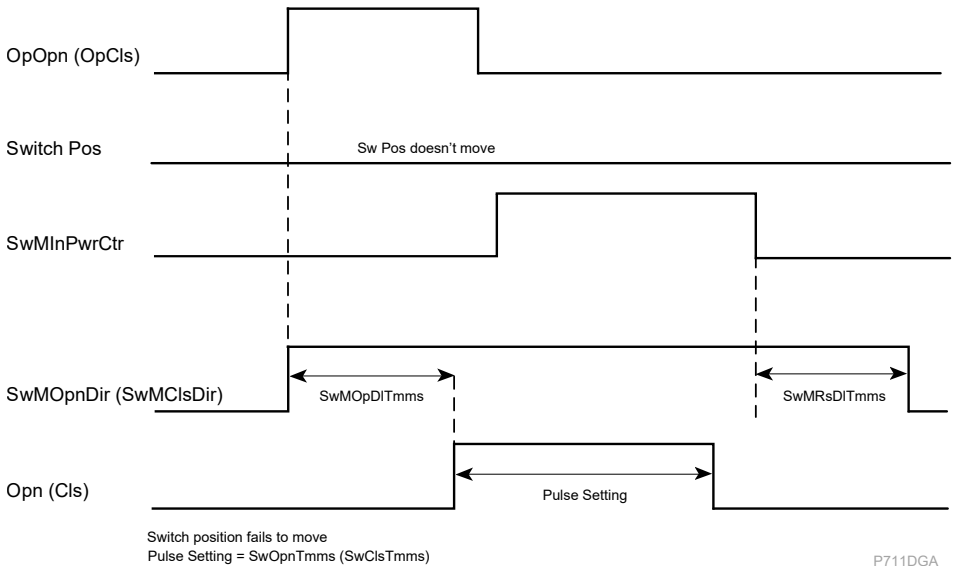


Figure 205 - The time sequence for status reset mode, switch position fails to move



After the opening/closing pulse resets, the power contactor will drop out removing voltage across the motor. After the *Motor reset delay*, the direction contacts are opened and operation is completed. If the *Power op* input does not drop out within the *Motor reset delay* after pulse resets, the *Power contactor reset fail* alarm is raised.

Supervision

The motor voltage can be supervised by connecting the switched voltage to the *Power op* input. The switched voltage is after the contactor or high break contact used to make and break the motor current. The *Motor control timeout* can then be set to alarm if the switched voltage does not pick up or drop out as expected.

- If *SwMOpTmOut* is set to *0*, the *SwMInPwrCtr* input is ignored, warnings and alarms are not processed.
- If *SwMOpTmOut* is set to values other than 0 and the power contractor stays off, after the *Power contactor* output is energized, the *Power contactor op fail* alarm is raised and the control operation is canceled. The *Power contactor* output resets and the direction output resets after the reset delay. The alarm resets when a new *OpOpen* or *OpCls* signal is set.
- If *SwMOpTmOut* is set to values other than 0 and the power contractor stays on, after the *Power contactor* output is de-energized, the *Power contactor reset fail* alarm is raised. The alarm resets when the *SwMInPwrCtr* input returns to *False*.

Input and output signals

Table 324 - Input signals of the *SWXSWI*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
SwAux89a	89a	89a auxiliary contact (closed when switch closed)
SwAux89b	89b	89b auxiliary contact (closed when switch open)
GenBlkCls	Block close	Block close
GenBlkOpn	Block open	Block open

Table 324 - Input signals of the *SWXSWI* (Continued)

Name	Short label	Infotip
EEHthAlm	SW alarm	Switch health alarm (block open and closing)
EEHthWrn	SW warn	Switch health warning (block closing)
LocIn	Local	Set switch to local operation (disable control)
ResetOpCnt	Count reset	Reset operation count
OpOpn	Open signal	Open signal from SWCSWI
OpCls	Close signal	Close signal from SWCSWI
SwMInPwrCtr	Power ind	Power indication from motor contactor

Table 325 - Output signals of the *SWXSWI*

Name	Short label	Infotip
SwTyp	Switch type	Switch type
Pos	Position	Position
Loc	Local	Local
SwMOpnDir	Open direction	Direct motor control open direction
SwMClsDir	Close direction	Direct motor control close direction
Opn	Open command	Open command to switch
Cls	Close command	Close command to switch
SwMPwrCtr	Power contactor	Direct motor control power contact
BlkOpn	Open blocked	Open blocked
BlkCls	Close blocked	Close blocked
SwMPwrCtrWrn	Power contactor op fail	Power operation input did not pick up
SwMPwrCtrAlm	Power contactor reset fail	Power operation input did not reset
EEHealth	Switch health	Switch health
OpCnt	Operation count	Operation count
Blk	Blocked	Blocked

Setting parameters

Table 326 - Settings of the *SWXSWI*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
SwTypSet	Switch type	Used for Switch type indication	• Load break switch • Disconnector • Grounding switch • High speed grounding switch		Load break switch
SwAuxM	Status input	Used for position indication	• None • 89a • 89b • Both		None

Table 326 - Settings of the *SWXSWI* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
SwCmdM	Command mode	The control signal will be held for at least the pulse time in dwell mode or reset when the position changes in status reset mode	• Dwell • Status reset		Status reset
SwClsTmms	Close time	Close pulse length	100...100000 ms	10 ms	200 ms
SwOpnTmms	Open time	Open pulse length	100...100000 ms	10 ms	200 ms
SwMotCtlEna	Direct motor control	Allows direct drive of the switch mechanism. The Power contactor outputs will select open or close direction and then power the DC drive in that direction	• Off • On		Off
SwMOpDlTm-ms	Motor op delay	Time delay between selecting direction and applying power	1...1000 ms	1 ms	100 ms
SwMRsDlTmm-s	Motor reset delay	Time delay between disconnecting power and releasing direction	1...1000 ms	1 ms	100 ms
SwMOpTmOut	Motor control timeout	Time between power contactor output and feedback on power operation input. Set 0 to ignore power operation input	0...1000 ms	1 ms	0 ms

Characteristics

Table 327 - Characteristics of the *SWXSWI*

Characteristics		Values
Operate delay	DT accuracy	±1% or ±10 ms

Synchro-check (*RSYN*, ANSI 25)

Description

The synchro-check function checks the synchronization of the electrical networks on either side of a circuit breaker to avoid shocks to the system or breaker flashover during closing.

The *RSYN* function monitors the voltage amplitude, frequency and phase angle difference between two voltages.

The function operates in different conditions according to four synchronization modes:

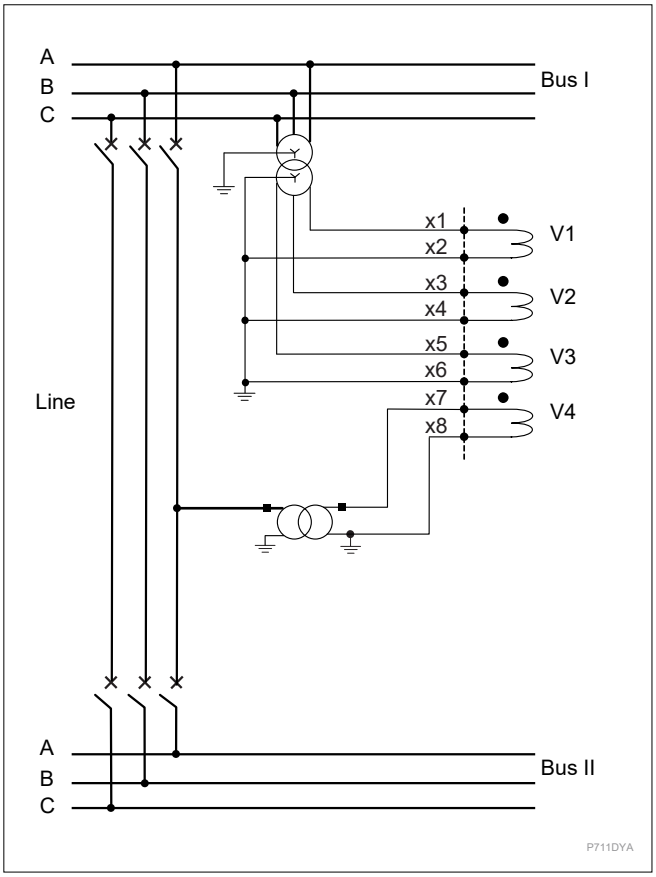
- In case of ***Off*** mode, the circuit breaker is not released when the voltage is present on both sides.
- In case of ***Synchronous*** mode, the conditions to release are defined as:
  - The phase angle difference is less than setting.
  - The slip is less than setting.
  - The magnitude difference is less than setting.
- In case of ***Asynchronous*** mode, the conditions to release are defined as:
  - The phase angle difference is less than the circuit breaker operate time multiplied by the slip, and the phase angle difference is reducing.
  - The slip is less than setting.
  - The magnitude difference is less than setting.

- In case of ***Generator*** mode, the conditions to release are defined as:
  - The phase angle difference is less than the setting.
  - The slip is less than setting, and the frequency of generator is above the system.
  - The magnitude difference is less than setting, and the magnitude of generator is above the system.

For ***Synchronous*** and ***Generator*** modes, when the conditions for closing are satisfied, a *Start* signal is issued. After the conditions have been maintained for the synchro-check time, the *Release* signal is issued. For ***Asynchronous*** mode, the *Start* signal is issued when the voltage and slip are less than the settings for the synchro-check time. The *Release* signal is issued when the angle difference is predicted to be zero based on the current slip and angle measurements.

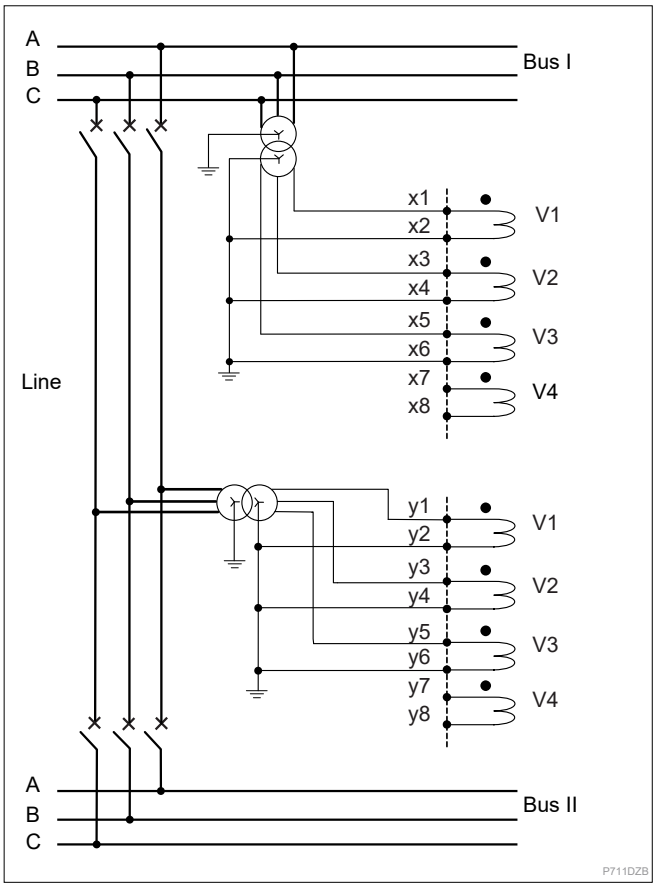
CT/VT connection diagrams

Figure 206 - Typical single phase synchro-check using one CT/VT module (5CT + 4VT)



NOTE: Refer to Three phase-to-ground voltages and one phase-to-ground voltage, page 51 and Three phase-to-ground voltages and one phase-to-phase voltage, page 52 for single phase connection.

Figure 207 - Typical three phase synchro-check using two CT/VT modules (5CT + 4VT)



NOTE: Refer to Three phase-to-ground voltages, page 51 and Two phase-to-phase voltages , page 52 for three phase connections.

Voltage check

When one of the two voltages is absent, coupling may be authorized according to one of the seven checking modes:

- VBus and VLine absent (*DLDB*)
- VBus absent and VLine present (*LLDB*)
- VBus present and VLine absent (*DLLB*)
- VBus absent regardless of VLine state (present or absent) (*DLDB* OR *LLDB*)
- VLine absent regardless of VBus state (present or absent) (*DLDB* OR *DLLB*)
- One voltage is present while the other one is absent (*LLDB* OR *DLLB*)
- At least one voltage is absent (*DLDB* OR *LLDB* OR *DLLB*)

The presence of bus/line voltage is detected by comparing the voltage to the ***LiVBusVal***/***LivLinVal*** limit setting. The absence of the bus or line voltage is detected by comparing the voltage to the ***DeaBusVal***/***DeaLinVal*** limit setting.

When the required live/dead conditions are met, a *Start* signal is issued. Providing the conditions are maintained, the *Release* signal is then issued after the voltage check time.

Phase selection

Eight voltage types are available in phase selection function for synchro-check or voltage check.

- VA: phase A voltage

- VB: phase B voltage
- VC: phase C voltage
- VAB: phase A to phase B voltage
- VBC: phase B to phase C voltage
- VCA: phase C to phase A voltage
- 3VPN: VA for synchro-check, minimum voltage among VA, VB and VC for voltage presence checking, maximum voltage among VA, VB and VC for voltage absence check.
- 3VPP: VAB for synchro-check, minimum voltage among VAB, VBC and VCA for voltage presence checking, maximum voltage among VAB, VBC and VCA for voltage absence check.

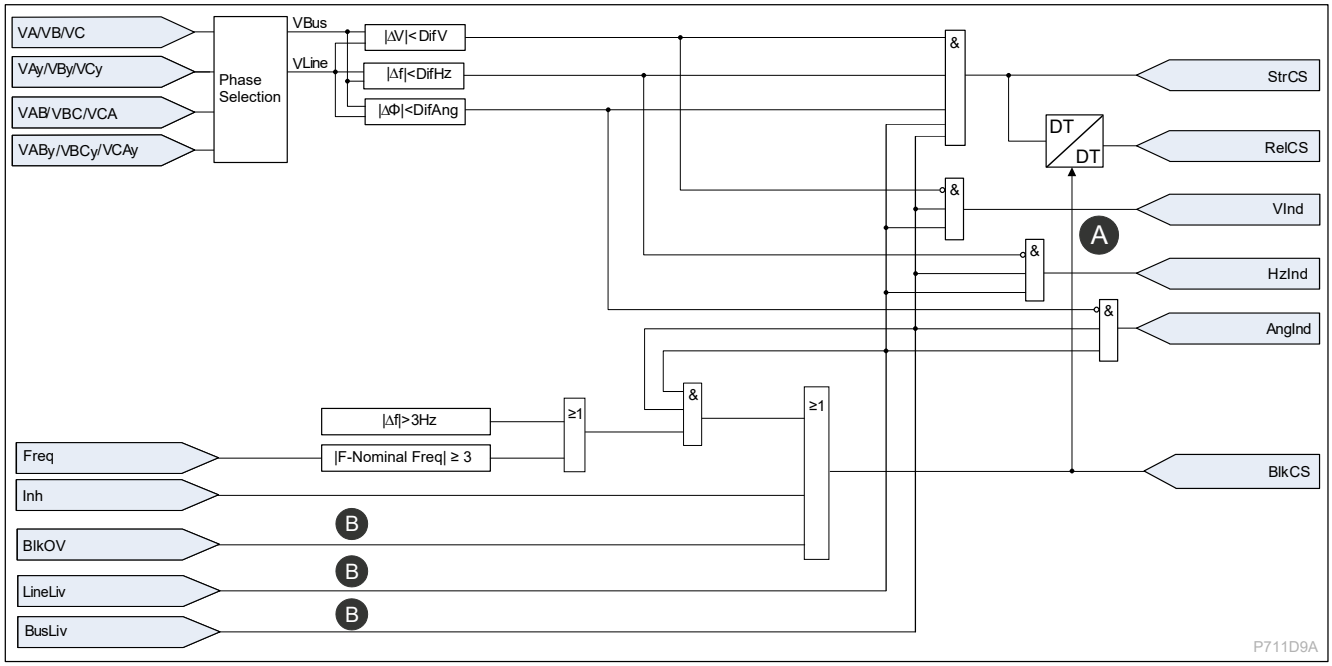
NOTE: 3VPN and 3VPP phase selection can only be chosen when the Vy is mapped from three phase VT, if not, this function will be blocked.

Synchro-check bypass

In the PowerLogic P7, the synchro-check can be bypassed via the ***Bypass*** input. This will force a *Release*.

Block diagram

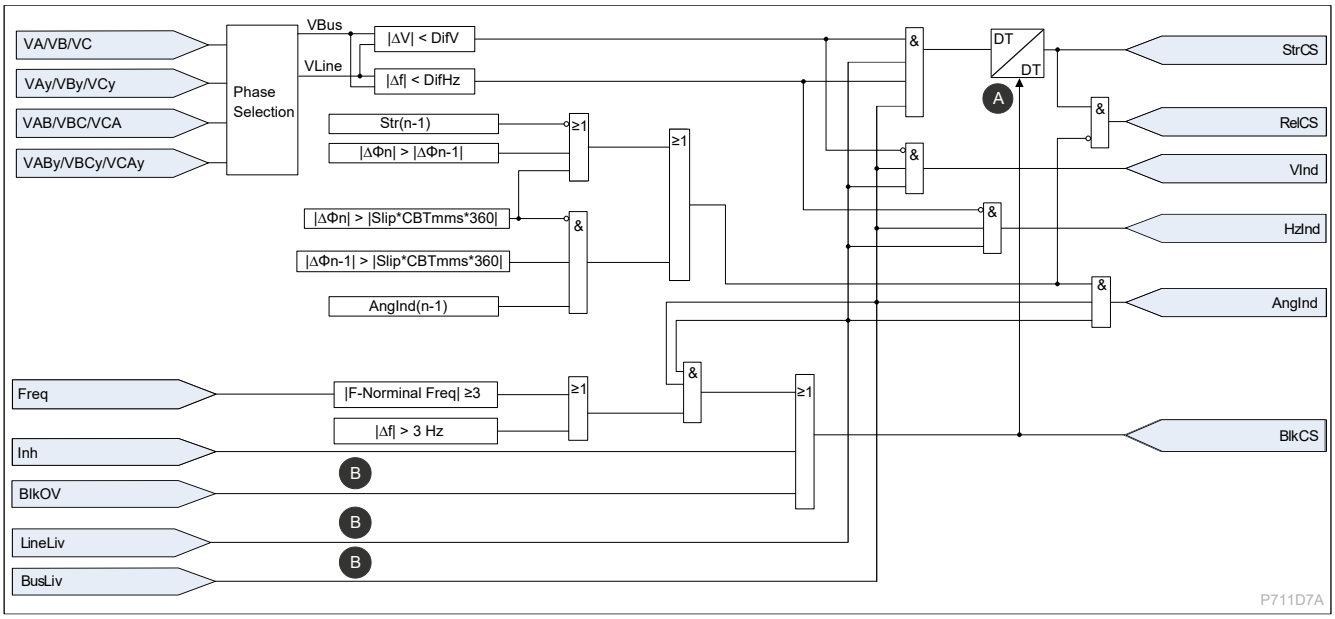
Figure 208 - Block diagram of the *RSYN* (Synchronous mode)



A Synchro-check time: *OpDITmms*
Reset delay: 0 ms

B The output signal from voltage status as the input signal.

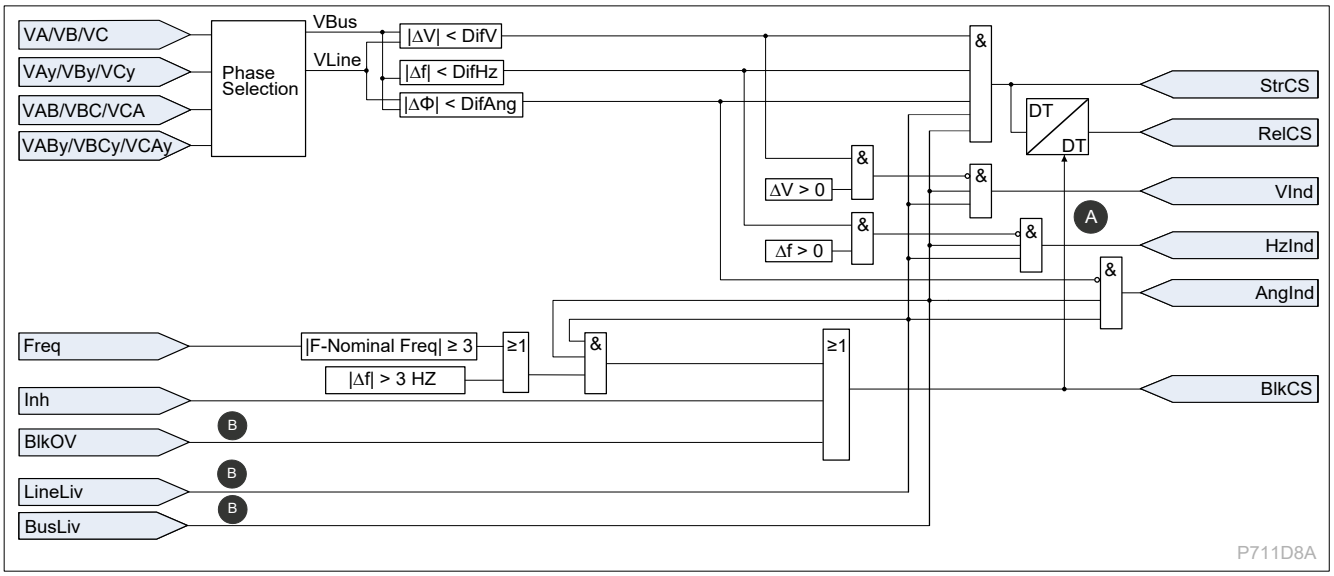
Figure 209 - Block diagram of the *RSYN* (Asynchronous mode)



A Synchro-check time: *OpDITmms*
Reset delay: 0 ms

B The output signal from voltage status as the input signal.

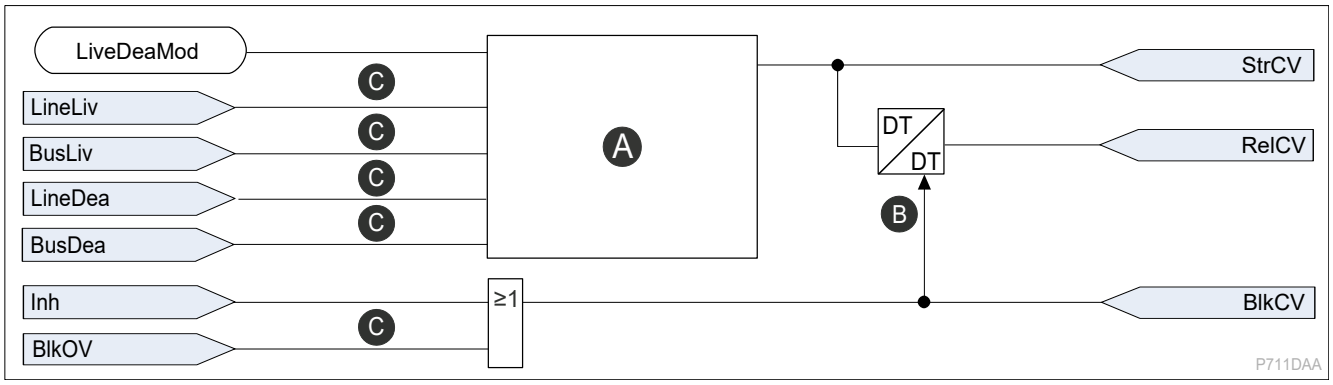
Figure 210 - Block diagram of the *RSYN* (Generator mode)



A Synchro-check time: *OpDITmms*
Reset delay: 0 ms

B The output signal from voltage status as the input signal.

Figure 211 - Block diagram of the *RSYN* (Voltage check)



A Voltage check function

B Voltage check time: *DeaTmms*
Reset delay: 0 ms

C The output signal from voltage status as the input signal.

Figure 212 - Block diagram of the *RSYN* (Voltage status)

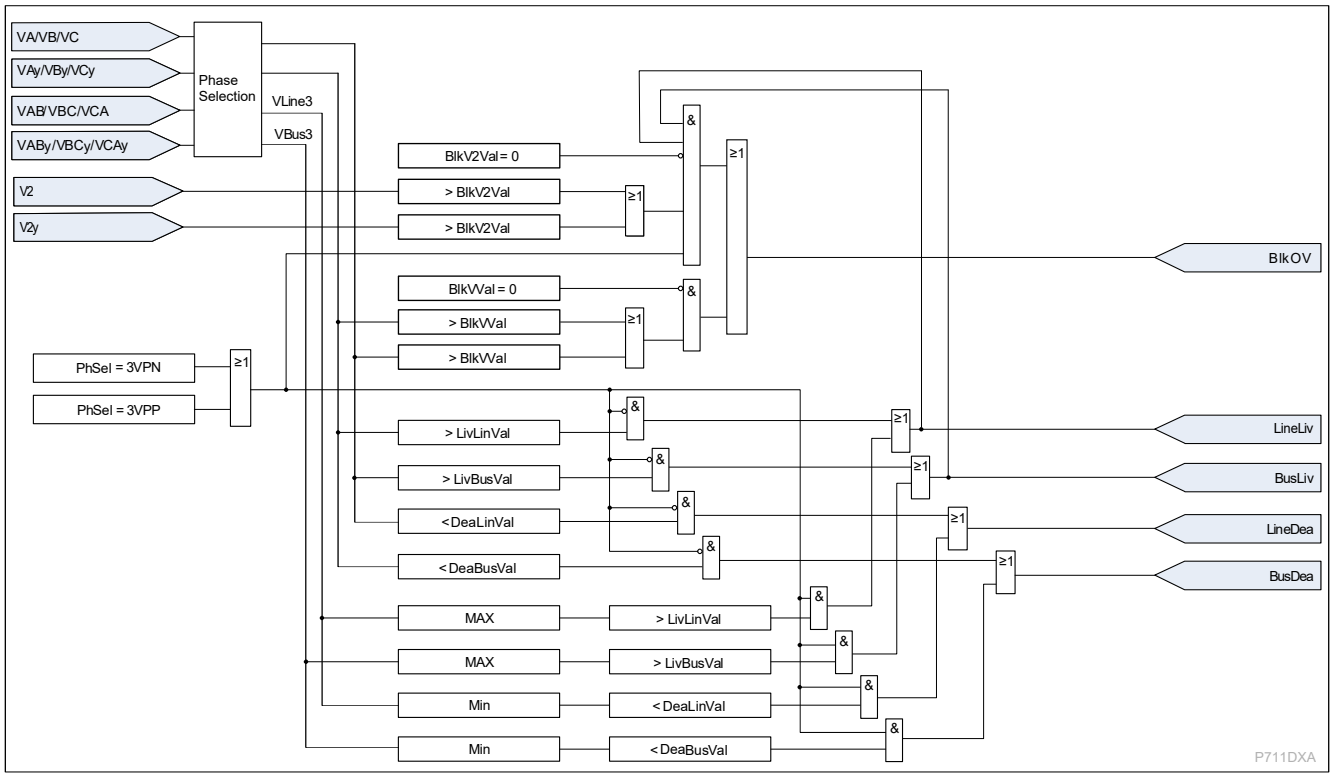
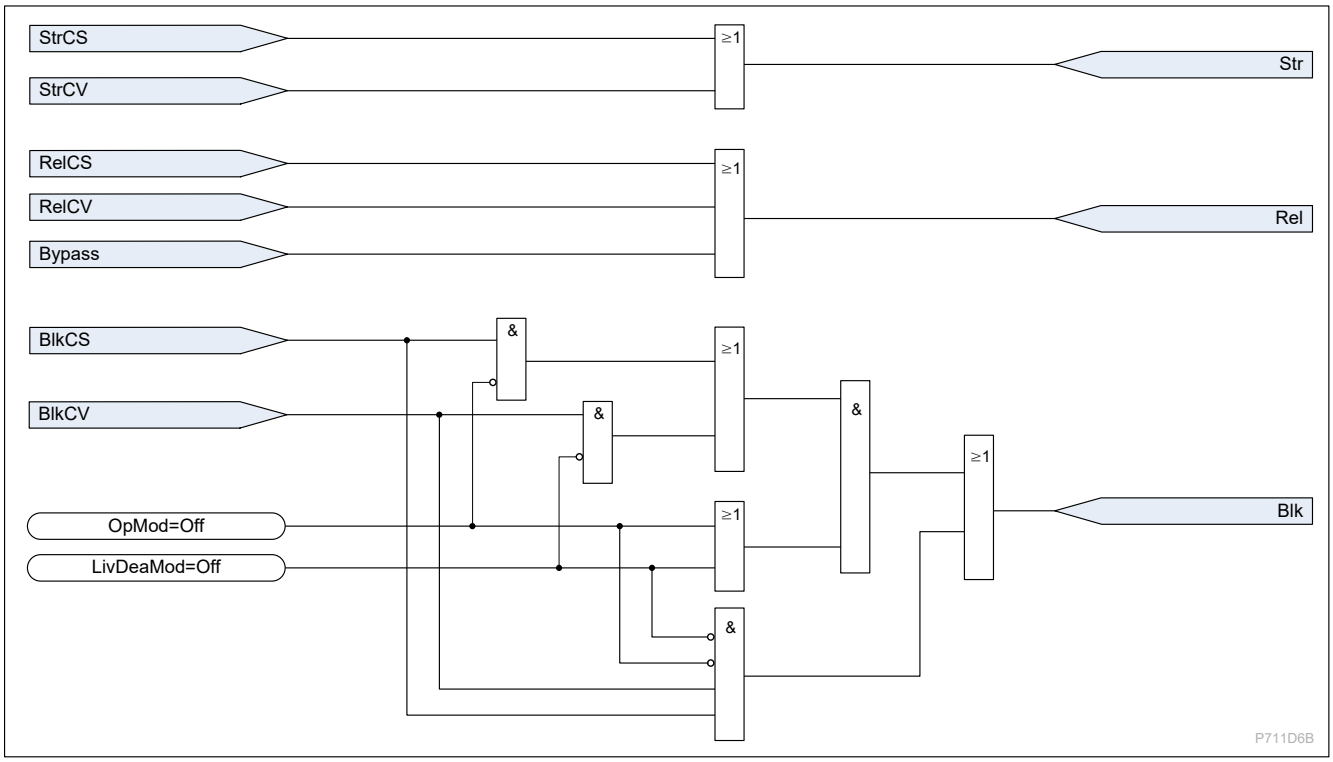


Figure 213 - Block diagram of the *RSYN* (Combined functions)



Input and output signals

Table 328 - Input signals of the *RSYN*

Name	Short label	Infotip
Inh	Inhibit	Inhibit function
Bypass	Bypass	Bypass synchrocheck (force Release)
VBayPN	Bay voltage	Bay voltage
VBayPP	Bay line voltage	Linked to bay voltage input source
VCheckPN	Check voltage	Check voltage
VCheckPP	Check line voltage	Linked to check voltage input source
VBayV2	Bay V2	Linked to bay voltage input source
VCheckV2	Check V2	Linked to check voltage input source
Freq	Frequency	Internal signal from FTGAPC1

NOTE: Vx should be mapped from three phase VT, and Vy should be mapped from another three phase VT or single phase VT. Vx refers to VBus and Vy refers to VCheck.

Table 329 - Output signals of the *RSYN*

Name	Short label	Infotip
BusDea	Bus dead	Bus dead
BusLiv	Bus live	Bus live
LineDea	Line dead	Line dead
LineLiv	Line live	Line live
Str	Start	Start
Rel	Release	Connected to CB control to allow close

Table 329 - Output signals of the *RSYN* (Continued)

Name	Short label	Infotip
VInd	Voltage diff inhibit	Voltage difference inhibiting release
HzInd	Slip inhibit	Frequency slip inhibiting release
AngInd	Angle diff inhibit	Angle difference inhibiting release
BlkOV	Overvoltage block	Blocked for high or unbalanced voltage
Blk	Blocked	Blocked
DifVClc	Voltage diff	Voltage diff
DifHzClc	Slip	Slip
DifAngClc	Angle diff	Angle diff
ClsDifVClc	Closing voltage diff	Closing voltage difference
ClsDifHzClc	Closing slip	Closing slip frequency
ClsDifAngClc	Closing angle diff	Closing angle difference

Setting parameters

Table 330 - Settings of the *RSYN*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
BayVT	Bay VT location	Select bay VT location as Bus or Line	• Bus • Line		Bus
PhSel	Phase selection	Phase selection	• VA • VB • VC • VAB • VBC • VCA • 3VPN • 3VPP		VAB
OpMod	Sync check mode	Synchronous is used for systems in sync. Asynchronous is used for unsynched systems and uses the CB closing time to close with minimal angle difference. Generator operates in a similar fashion to Synchronous except the frequency and voltage differential must both be positive	• Off • Synchronous • Asynchronous • Generator		Off
DifV	Max voltage diff	Max voltage difference for closing	0.01...2 pu	0.01 pu	0.06 pu
DifHz	Max slip	Max frequency slip for closing	0.005...2 Hz	0.005 Hz	0.05 Hz
DifAng	Max angle diff	Max angle difference for closing	1...90 deg	1 deg	20 deg
OpDlTmms	Sync check time	Check time for Sync check modes	0...10000000 ms	1 ms	100 ms
LivDeaMod	Volt check mode	Allows closing when either the line or bus is dead. DLDB enables Dead Line Dead Bus closing. LLDB enables Live Line Dead Bus closing. DLLB enables Dead Line Live Bus closing	• Off • DLDB • LLDB • DLLB • DLDB-LLDB • DLDB-DLLB • LLDB-DLLB • DLDB-LLDB-DLLB		Off

Table 330 - Settings of the *RSYN* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
LivLinVal	Live line value	Live line value	0.01...2 pu	0.01 pu	0.5 pu
LivBusVal	Live bus value	Live bus value	0.01...2 pu	0.01 pu	0.5 pu
DeaLinVal	Dead line value	Dead line value	0.01...2 pu	0.01 pu	0.15 pu
DeaBusVal	Dead bus value	Dead bus value	0.01...2 pu	0.01 pu	0.15 pu
DeaTmms	Volt check time	Check time for Live dead modes	0...10000000 ms	1 ms	100 ms
CBTmms	CB closing time	Closing time of the breaker	0...1000 ms	1 ms	50 ms
BlkVVal	Overvoltage block	If any voltage used for sync check or voltage check exceeds this level the function is blocked	0.01...2 pu	0.01 pu	1.2 pu
BlkV2Val	Unbalance block	Unbalance block	0...2 pu	0.01 pu	0.1 pu

Characteristic

Table 331 - Characteristics of the *RSYN*

Characteristics		Values
Voltage	Accuracy	±1% or ±0.001 pu (Slip frequency=0)
	Hysteresis	< 1%
Angle	Accuracy	±1%
	Hysteresis	< 1°
Slip Frequency	Accuracy	±5 mHz or ±5%
	Hysteresis	< 5 mHz
Start delay (Asynchronous mode)	Accuracy	±1% or ±10 ms
Operate delay (Synchronous mode and Generator mode)	DT Accuracy	±2% or ±5 ms
Operate delay (voltage check)	DT Accuracy	±2% or ±5 ms
Asynchronous Angular difference at closing	Accuracy	±1° @ 0.5 Hz slip setting, or + 5...0 ms
Characteristic time	Voltage check Start time/Reset time	< 35 ms
	Synchro-check Start time/Reset time (only for angle sync)	< 35 ms
	Synchro-check Start time/Reset time (only for slip frequency sync)	< 135 ms
Blocked	Block time	< 20 ms
	Reset time	< 40 ms

Auto-recloser (*TRIRREC*, ANSI 79)

Description

Dependent on the application, a high percentage of faults on the electrical network are transient, such as lightning or insulator flashovers. The auto-recloser (AR)

function is designed to automatically restore power to a feeder or overhead line after a protection trip has occurred by a trip/close sequence (auto-reclosing cycle), to minimize the down-time of the network power in case of a transient fault.

This means that in most fault incidents, if the faulty line is immediately tripped, reclosure of the CB will result in the line being successfully reenergized (such as Closed/Open/Closed cycle).

But, as permanent faults can also occur, an AR scheme must be also designed, to allow elimination of this fault case by, after a defined number of auto-reclosing cycles, leaving the circuit breaker in the open state (such as Closed/Open/Closed/Open cycle).

Auto recloser function

The AR function can provide up to 4 reclosing attempts or shots. A reclosing shot is initiated by operation of a protective element (internal or external trip).

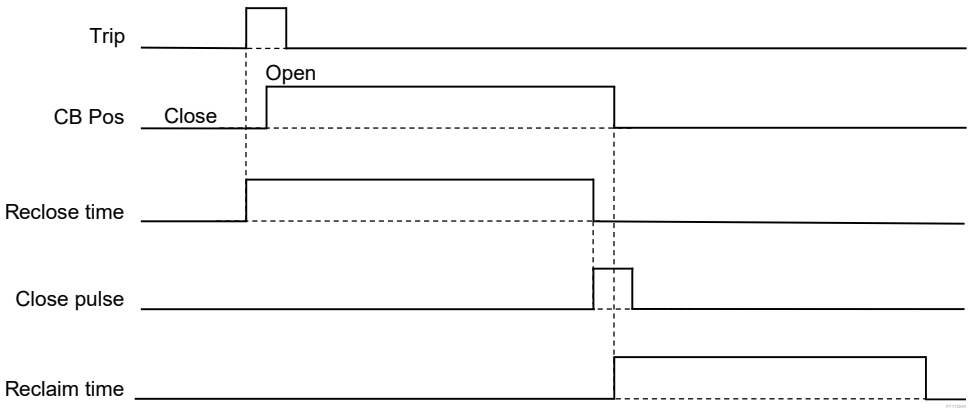
The appropriate reclose time (*Rec3Tmms*) of the cycle is launched when the trip appears or when the trip disappears, depending on the setting (*RecStrMod*). At the end of the reclose time, the closing sequence is started. If the shot has sync check, it will check the release signal and close the breaker when it is received. If the shot does not have sync check, the close pulse (*OpCls*) is generated, which leads finally to a CB close command by the *CBXCBR* to the CB, if all CB closing conditions are met.

The reclaim time (*RclTmms*) starts with the CB Closed state detection. If the CB has not been tripped again, the AR logic is reset at the end of the reclaim time, to move the AR back to start a new cycle again from the first shot (for future faults).

If the protection re-trips during the reclaim time, the relay either advances to the next shot in the programmed AR cycle, or if all programmed reclose attempts have been made, goes to lockout.

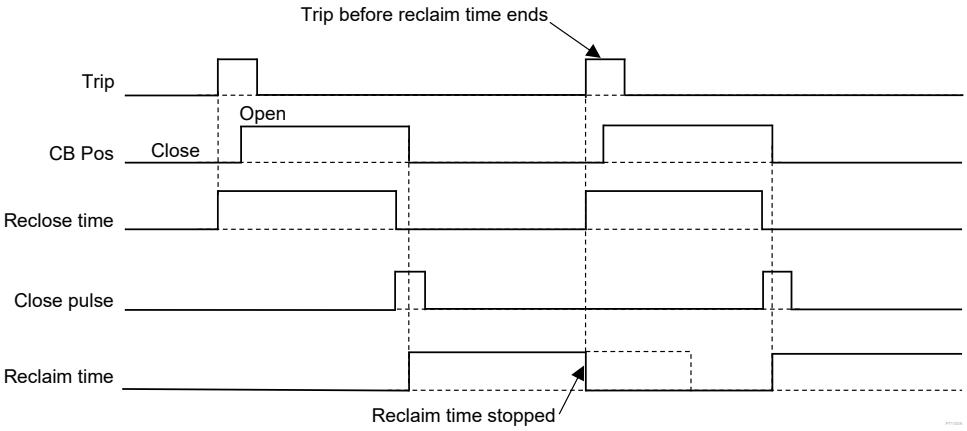
The following diagram summarizes the auto recloser procedure for a successful reclose.

Figure 214 - Successful reclose



The following diagram illustrates a second trip command before the end of the reclaim time:

Figure 215 - Unsuccessful reclose during the first cycle



Settings

The user can define:

- If the AR is enabled or disabled (*SetMod*)
- The maximum number of cycles (*UseCyc*)
- The timeout window for synchro check (*SyncTmms*)
- The timeout window after the CB operates (*CBOpTmms*)
- The timeout window after a Manual Close (*ManClsTmms*)
- If the protection trips initiate the AR cycle with rising or falling edge (*RecStrMod*)

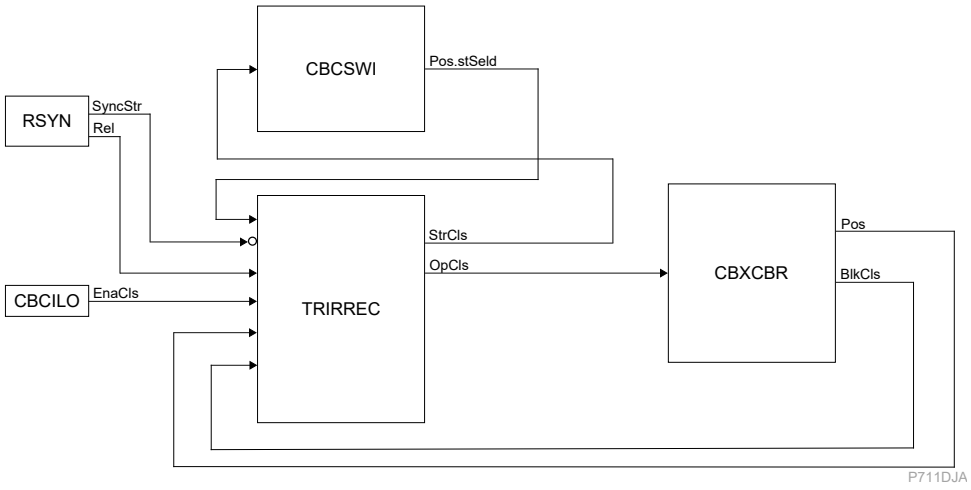
For each cycle, the user could define:

- The reclose dead time (time to reclose command after trip, *Rec3Tmms*1-4)
- The reclaim time, after the CB close (*RclTmms*)
- If the synchrocheck conditions are mandatory or not (*SyncChk*1-4)

Interconnection with other functions

A conceptual overview, based on IEC 61850 logical nodes is given in the diagram below:

Figure 216 - AR interconnection overview



The interconnection signals from the auto recloser (*TRIRREC*) to other LN are hardwired, meaning there is no configuration of the input and output signals required.

- *Pos*: CB Position, input link from the circuit breaker proxy *CBXCBR*
- *BlkCls*: CB Block close, input link from the circuit breaker proxy *CBXCBR*
- *EnaCls*: CB Enable close, input link from the circuit breaker interlocking *CBCILO*
- *Pos.stSeld*: CB Position control selected or running, input link from the circuit breaker control *CBCSWI*
- *OptoCls*: Manual close command from the circuit breaker control *CBCSWI*
- *OpCls*: Operate close command impulse, output link to the circuit breaker proxy *CBXCBR*

  NOTE: The connections to the synchronizer are made with the matrix to allow internal or external sync check to be used.

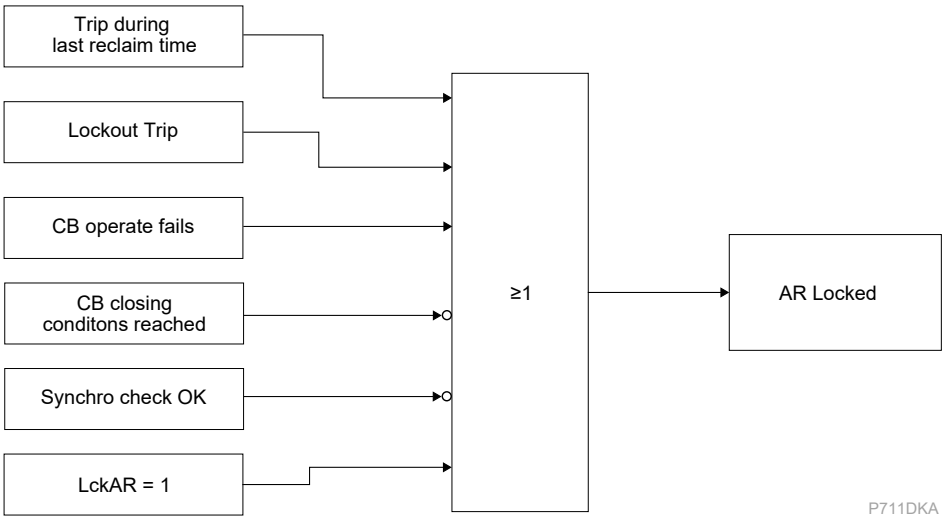
AR ready, AR lock, and AR unlock

The AR is ready, when all conditions are fulfilled to activate the function, for example the CB position must be closed and no event shall have locked the function.

The AR is locked in the following cases:

- If there is still a trip during the reclaim time of the last cycle
- If a slow trip occurs and the used number of reclose cycles is 1
- If the AR receives a lockout trip
- If CB operation fails
- If the CB closing conditions are not reached
- If the Synchro-check prevents any closing
- If the dedicated input *LckAR* is set to 1

Figure 217 - Lockout of AR



When the AR is not *Out of service* but *Locked*, the AR cannot send any Close order *OpCls* to the *CBXCBR*. The current AR status *AutoRecSt* is then set to *Not Ready*, *LckCond* is filled with the reason of the lock and the AR logic is reset:

- *StrCyc* and *OpCls* are set to 0
- *RecCyc* is set to 0
- All timers are reset. *NxtCyc* is set to None

The auto-recloser can be unlocked by a user or an automation function:

- With an unlock control input (*RstLckCtl*) from the HMI or communication link
- With an unlock input assigned to *RstLck* in the matrix
- Following a successful manual close

- After removal of the *Out of service* state with control command (*OutServCtl*) or binary input (*OutOfServ*)

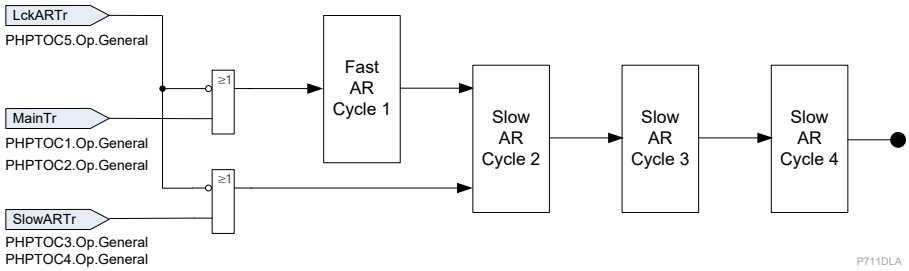
Trip configuration

The recloser is initiated by linking the protection operate signal to the *Initiate AR* (*MainTr*) input. This provides a standard 1-4 shot auto-reclose for the connected functions.

It is also possible to vary the number of shots depending upon which protection operates by using the *Initiate AR* and *Skip shot AR* (*SlowARTr*) inputs. In these schemes, the first shot is normally connected to instantaneous protection and has a short dead time and is referred to as high speed or fast auto-reclose. Subsequent reclose shots have a longer dead time and are referred to as time delayed or slow auto-reclose. Non-instantaneous protection skips the fast stage and only initiates the slow stages.

The trip(s) which shall initiate the fast AR cycle are configured in the input matrix using the *Initiate AR* input signal. The trip(s) to trigger directly a slow and therefore 2nd AR cycle is to be assigned to the *Skip shot AR* input signal. All trip(s) which shall lock the AR, are assigned to the *Lockout trip* (*LckARTr*) input signal which immediately locks the recloser function. The following figure shows the principle of the trigger or lock logic for the AR function.

Figure 218 - Trips to trigger or lock AR cycles



Depending upon the number of cycles configured as maximum with setting parameter *Number of shots* (*UseCyc*), only a fast (*UseCyc* = 1), a fast and a slow (*UseCyc* = 2), a fast and up to 2 (*UseCyc* = 3) or a fast and up to 3 slow (*UseCyc* = 4) cycles are provided.

Several trips can occur for the same fault in parallel. Therefore, a priority between the trips has been defined:

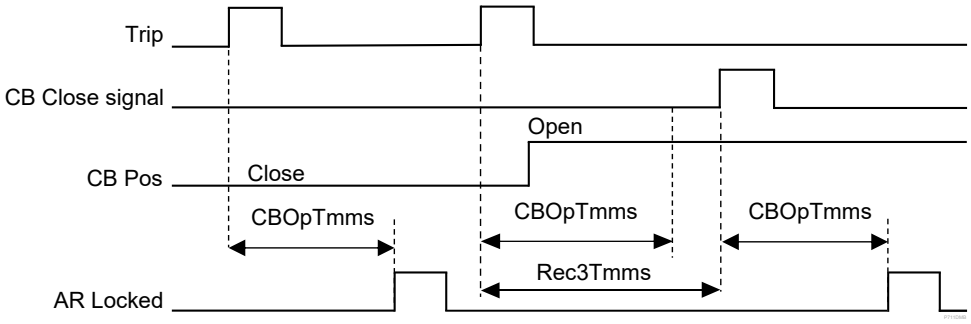
- *LckARTr* has the highest priority: if such trip occurs, the AR is immediately locked
- *MainTr* has the second priority: if there is no *LckARTr* trip but there is *MainTr*, the AR is launched with all the cycles
- *SlowARTr* has the lowest priority: if there is only *SlowARTr* trips, the AR is launched with the first cycle skipped

CB operation check

Immediately after the trip is detected, a time-out (*CBOpTmms*) is launched to wait for the CB opening. The AR is locked if the CB has not opened at the end of this time.

At the end of the shot dead time, the CB close signal is sent and the same time-out is launched to wait for the CB closing. The AR is locked if the CB is not closed at the end of this timer.

Figure 219 - Operate fail conditions



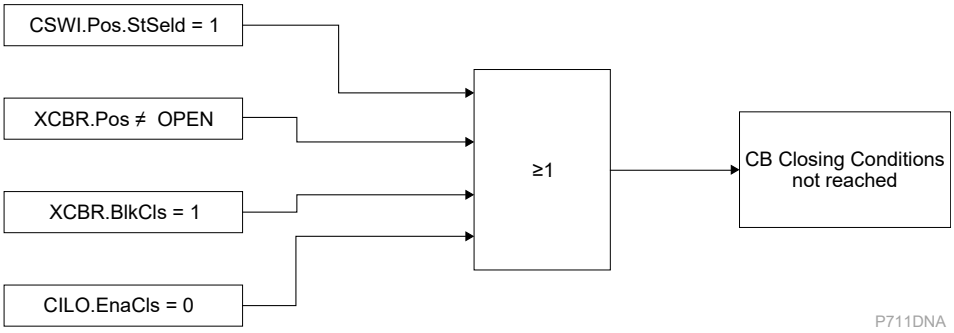
CB closing check

The AR conducts checks prior to initiating the *Close signal* which are dependent on the application. The checks ensue that:

- The *CB position* is *Open* at the end of the *CB operation timeout* (*CBOpTmms*) or at the end of the Reclose Time (*Rec3Tmms*)
- There is not a CB *Close blocked* input present from the Circuit Breaker (*CBXCBR.BlkCls*)
- No Position Control is selected or running (*CBCSWI.Pos.stSeld*)
- The external switchgear is in a suitable state for closing the CB (interlock checks)

If the CB closing conditions are not reached at the end of the Reclose Time, the AR is locked.

Figure 220 - CB closing conditions not reached logic



AR with synchronism check

For operation with synchonism check, the sync *Release* input must be present when the synchro-check is set for the shot to allow reclose. This input is connected to the release output of the relevant synchro-check stage. This can allow a different synchro-check configuration for manual and auto reclosing by varying which synchro-check element release is connected.

With a setting for each cycle, the user can choose to check or not the synchronism.

When this setting is set to disabled, no system checks are required that may be preferred when high speed AR is applied to avoid the extra time for a system check.

When this setting is set to enabled, an extra delay (*SyncTmms*) is introduced after the reclose time. At the end of this delay, if the synchro-check is not OK (Rel = 0), the AR fails and is locked. If a release is received within this timeout, then it will issue a CB *Close signal*.

The *Sync fail* (*SynOoLim*) input can also be used to ensure the synchronizer is seeing valid closing conditions during the synchronizer timeout period. This is normally applied when this period is quite long and it is an advantage to lockout quickly if synchronism will not be met. For example, if asynchronous closing is being used, an inverted link can be made to the synchronizer start signal to ensure it is seeing valid voltage and frequency conditions and will close at the next voltage alignment. If the start is not present the at the end of the reclose time the AR will fail immediately and lockout without waiting for the synchrocheck to time out.

Figure 221 - Synchronism check logic

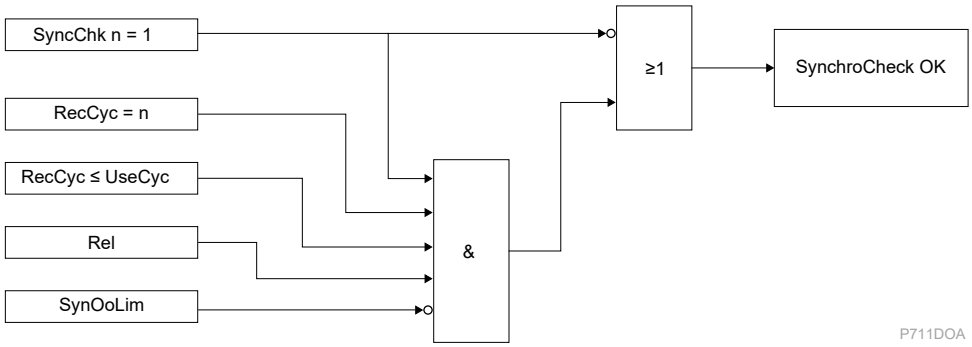


Figure 222 - Synchrocheck OK



Figure 223 - Locked due to no Synchrocheck release

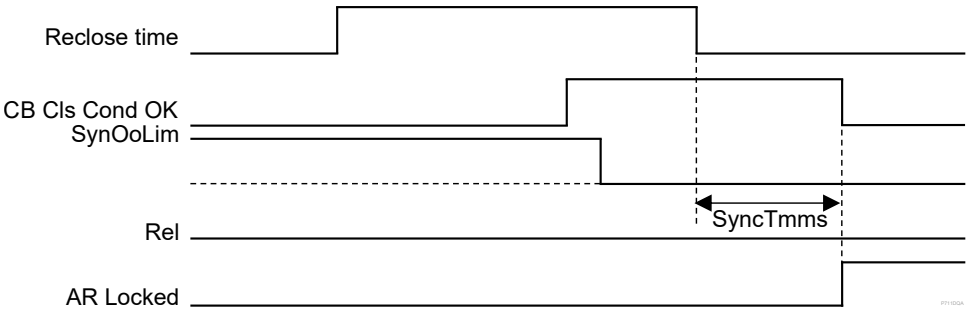
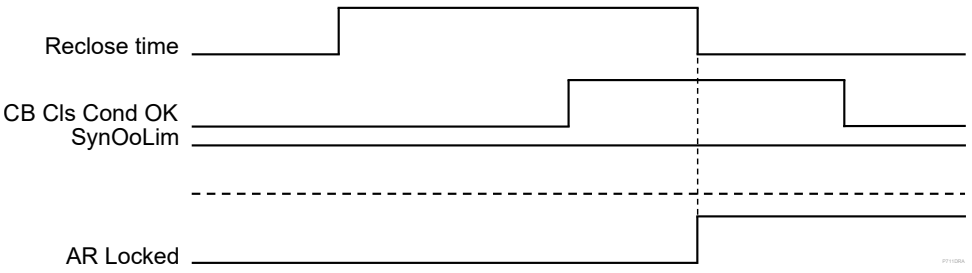


Figure 224 - Locked due to no Synchrocheck Start

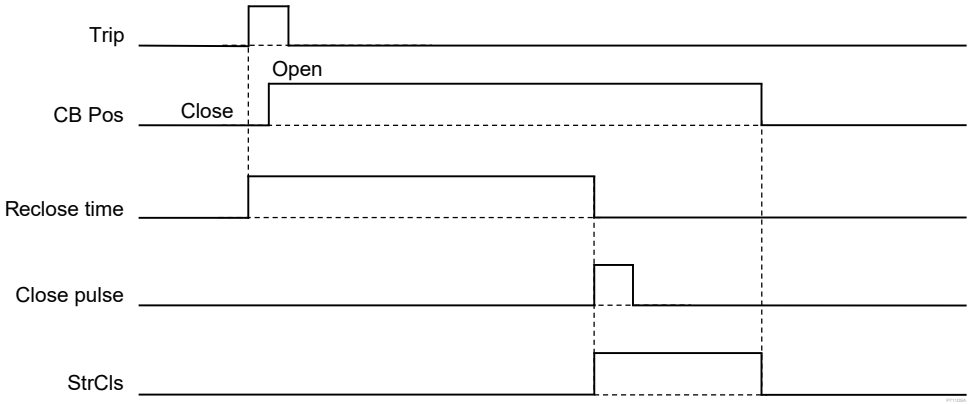


Operator control

No automation or operator control, except *Out of service*, is allowed during an AR closing sequence.

The output signal *Close in progress* (*StrCls* = 1) signals this critical phase, which can be used as required to block manual CB control. The signal is active from the start of the AR sequence, including synchro-check phase when used, until the CB has reached the closed state or fail to close has been recognized. By default, this is linked to the *External op* (*AutoOpPrg*) of the CB control function (*CBCSWI*) to block operator actions during reclosing.

Figure 225 - Status of StrCls



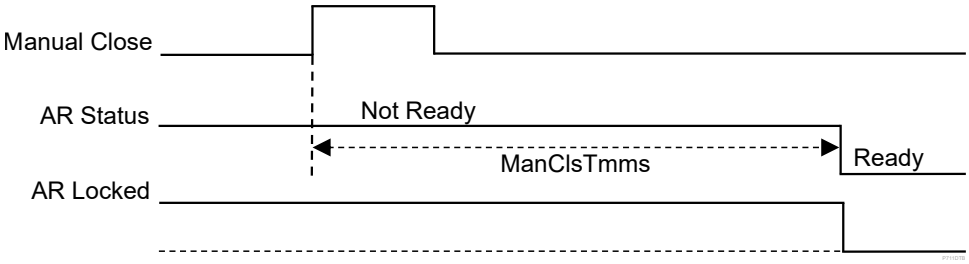
Manual close

After a manual close, the AR is inhibited by a configurable time delay (for safety reasons if the line has a permanent fault after a long opening) and the current auto reclosing status (*AutoRecSt*) is set to *Not Ready*.

At the end of this delay, the AR is ready to start a new cycle from the first shot and the current *Recloser status* (*AutoRecSt*) is set back to *Ready*.

If the AR was locked before closing, it is unlocked after this time delay.

Figure 226 - Unlocked due to Manual Close



Out of service

The auto-recloser function can be set to *Out of service* by the user using the HMI, a control command *OutServCtl* via the communication link or by a signal assigned to the input *OutOfServ*.

If the auto-recloser is out of service, no cycle is authorized. The current *Recloser status* is set to *Not Ready* and the *Next shot* is *None*.

If an *Out of service* request (command or binary input equal to 1) is received during an AR cycle, the cycle stops immediately and the AR logic is reset.

Monitoring

All stages of the AR operation are monitored to check the AR sequences:

- If the function is enabled or disabled (*Beh*)
- Which reclose cycle is running (*RecCyc*)
- Which reclose cycle is coming next (*NxtCyc*)

  NOTE: The *NxtCyc* signal can be linked to protection elements to change/block/enable functions depending upon whether the recloser is active or the shot number. Typical applications are fuse saver schemes where the first shot trip is fast followed by slower shots.
- Which AR state is running (*AutoRecSt*)
- If CB close is in progress or in operation (*StrCls*, *OpCls*)
- If AR is dynamically blocked (*Blk*)
- Which event caused the lockout (*LckCond*)
- How many three phase reclosing operations are made since the previous reset (*Rec3PhCnt*)

Table 332 - States of NxtCyc, AutoRecSt, and LckCond

Parameter	Value and shown value	Description
NxtCyc	0 - None	None
	1 - 1	1
	2 - 2	2
	3 - 3	3
	4 - 4	4
AutoRecSt	1 - Ready	Ready
	2 - In progress	Autoreclose in progress
	3 - Successful	Autoreclose successful
	4 - Waiting for trip	Waiting for trip
	5 - Trip received	Trip issued by protection
	6 - Fault cleared	Trip input has reset
	7 - Closing	Close in progress. Close issued as soon released by synchroceck if enabled
	8 - CB closed	Circuit breaker closed
	9 - Shot fail	The current cycle was unsuccessful and the recloser will move to the next shot
	10 - Unsuccessful	Autoreclose unsuccessful
	11 - Aborted	Aborted
	12 - Not ready	Not Ready
LckCond	0 - Unlocked	The recloser is not blocked
	1 - Num shots	Max number of shots reached
	2 - Lockout trip	The lockout trip input was activated
	3 - Close fail	The CB failed to close in response to the close signal
	4 - CB checks	The closing conditions are not reached
	5 - Sync fail	Synchrocheck did not issue a start or release
	6 - BAR input	Block AR input activated

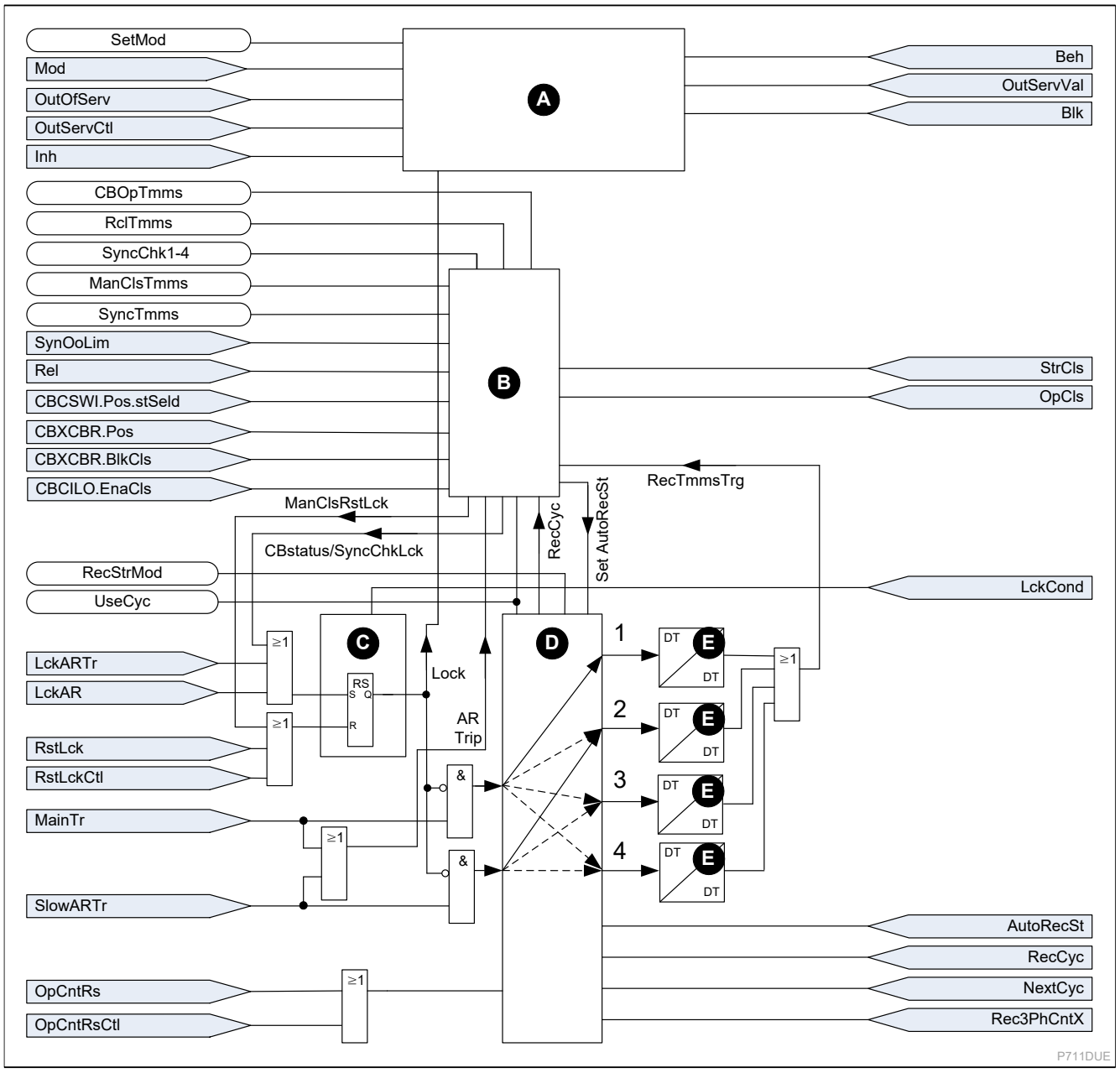
Controls

The following control objects are provided on the HMI and via the communication links:

- Control to put AR out of service (*OutServCtl*)
- Control to unlock AR (*RstLckCtl*)
- Control to reset the AR closing counter *Rec3PhCnt* (*OpCntRsCtl*)

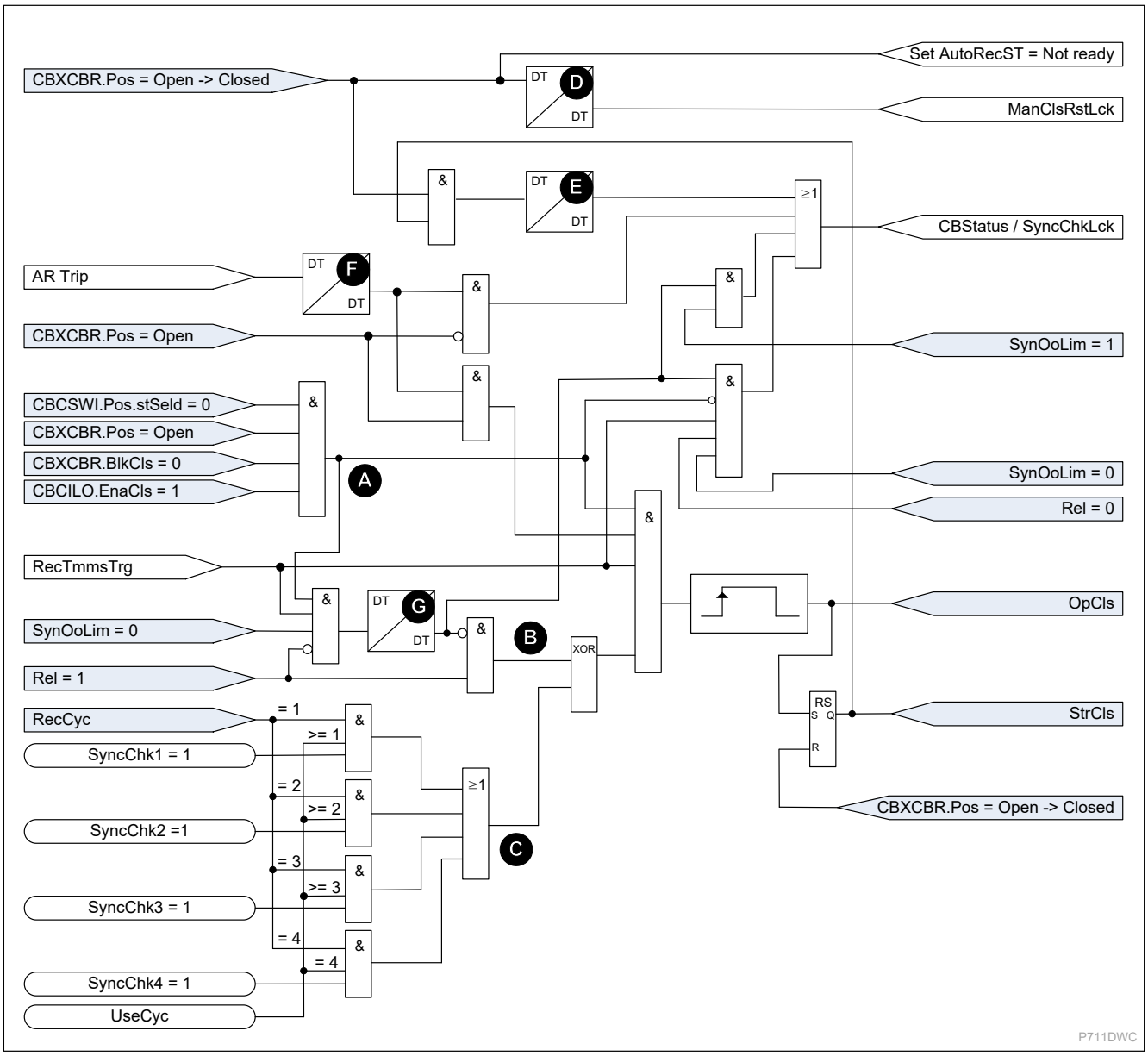
Block diagram

Figure 227 - Block diagram of the *TRIRREC*



A	Function mode logic	B	CB closing logic	C	AR lockout control
D	AR cycle control	E	Dead (reclose) time: *Rec3Tmms*1-4 Reset delay: 0 ms		

Figure 228 - Block diagram of the CB closing



A	CB Close Condition OK	B	SynChk OK	C	SynChk used
D	Manual close timeout: *ManClsTmms* Reset delay: 0 ms	E	Reclaim time: *RclTmms* Reset delay: 0 ms	F	CB operation timeout: *CBOpTmms* Reset delay: 0 ms
G	Synchrocheck timeout: *SyncTmms* Reset delay: 0 ms				

Input and output signals

Table 333 - Input signals of the *TRIRREC*

Name	Short label	Infotip
Inh	Inhibit	Inhibit function
LckARTr	Lockout trip	Trip signals connected to this input will force recloser to lockout
MainTr	Initiate AR	Trip signals connected to this input trigger reclosing

Table 333 - Input signals of the *TRIRREC* (Continued)

Name	Short label	Infotip
SlowARTr	Skip shot AR	Trip signals connected to this input trigger reclosing skipping the first shot
LckAR	Block AR	Lockout recloser
Rel	Sync release	Sync release
SynOoLim	Sync fail	Synchrocheck fail to start - bypass operation timeout
OutOfServ	Out of service	Out of service
RstLck	Unlock	Unlock
OpCntRs	Count reset	Reset close counter
Pos	Breaker position	Internal singal from CBXCBR
EnaCls	Enable close	Internal signal from CBCILO
BlkCls	Close blocked	Internal singal from CBXCBR
CBstSeld	Control in progress	Internal signal from CBCSWI

Table 334 - Output signals of the *TRIRREC*

Name	Short label	Infotip
AutoRecSt	Recloser status	Recloser status
NxtCyc	Next shot	Next shot (cycle). Can be used linked to protection elements to vary operation based on the upcoming shot
RecCyc	Current shot	Current shot (cycle)
StrCls	Close in progress	Close in progress. This starts at the end of the dead time and ends when the breaker closes
OpCls	Close signal	Close signal to breaker. It is a pulse issued to the breaker
LckCond	Lockout status	This indicates the current lockout status
Blk	Blocked	Blocked
Rec3PhCntX	Close count	Number of reclose operations
OutServVal	Intern Out Serv Val	Internal value Out of Service
OutServCtl	Out of service	Out of service
RstLckCtl	Unlock	Unlock
OpCntRsCtl	Count reset	Count reset

Setting parameters

Table 335 - Settings of the *TRIRREC*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
UseCyc	Number of shots	Number of shots (cycles)	1...4	1	4
Rec3Tmms1	Dead time 1	Dead (reclose) time for shot 1	10...10000000 ms	10 ms	10000 ms

Table 335 - Settings of the *TRIRREC* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
Rec3Tmms2	Dead time 2	Dead (reclose) time for shot 2	10...10000000 ms	10 ms	60000 ms
Rec3Tmms3	Dead time 3	Dead (reclose) time for shot 3	10...10000000 ms	10 ms	180000 ms
Rec3Tmms4	Dead time 4	Dead (reclose) time for shot 4	10...10000000 ms	10 ms	180000 ms
RclTmms	Reclaim time	Reclaim time	1000...600000 ms	10 ms	180000 ms
SyncChk1	Synchrocheck shot 1	Synchrocheck is required for the first shot	• Off • On		Off
SyncChk2	Synchrocheck shot 2	Synchrocheck is required for the second shot	• Off • On		Off
SyncChk3	Synchrocheck shot 3	Synchrocheck is required for the third shot	• Off • On		Off
SyncChk4	Synchrocheck shot 4	Synchrocheck is required for the fourth shot	• Off • On		Off
SyncTmms	Synchrocheck timeout	Synchrocheck timeout	10...600000 ms	10 ms	1000 ms
CBOpTmms	CB operation timeout	The recloser goes to lockout if the requested operation is not successful in this period. It will check opening occurs within this period when the recloser is initiated and closing occurs within this period when the recloser issues a close signal	10...600000 ms	10 ms	5000 ms
ManClsTmms	Manual close timeout	The recloser is blocked for this time after a manual close	10...3600000 ms	10 ms	5000 ms
RecStrMod	Initiate on trip reset	If On the dead time will start when the trip signal resets otherwise the dead time will start from the trip signal	• Off • On		Off

Characteristics

Table 336 - Characteristics of the *TRIRREC*

Characteristics		Values
Time stages	Accuracy	±2% or ±20 ms

Logging and recording functions

Time tagging

The PowerLogic P7 stores time tagged logs and records which can be used for fault analysis. These data can be read from the device and analyzed using the corresponding tools.

The items that are time tagged and logged are:

- Sequence of events (SOE)
- Disturbance record
- Operation log
- Communication record
- Fault record

The PowerLogic P7 time stamp resolution is 1 ms.

Sequence of event (*GENGLOG*)

Description

The PowerLogic P7 is capable of logging and recording of all events that happen during power system operation. All operationally relevant signals, each fully tagged with date and time at signal start and signal end, are registered and stored in chronological order. For example, an event can be, start-on, start-off, trip-on or trip-off of any protection stage, alarm-on or alarm-off, a binary input change, etc.

Table 337 - Example of SOE record

Parameter	Value	Description
Date	2021-08-18	Time stamp of the log, date.
Time: hh:mm:ss.ms	16:45:51.000 ms	Time stamp, time of day.
Label	IED_nameBayLD/ *PHPTOC*1.Op	Event source.
Language reference	I>1 Operate	Event simple text description.
Event status	General: true PhsA: true PhsB: false PhsC: false	SOE is stored in Data Object level. All the Data Attribute status in the Data Object will be saved in one single SOE.

The logged events can be read from the HMI under ☰ **> Logs > Sequence of events**.

The maximum size of the buffer is 10000 events. All events are stored in non-volatile memory inside the PowerLogic P7. SOE is stored in Data Object level. There may be multi Data Attribute status in one single SOE.

When the buffer is filled, the oldest event will be overwritten when a new event occurs. The shown resolution of a time stamp for an event is one millisecond, but the actual resolution depends on the particular function creating the event. For example, most protection stages create events with a 1 ms, 5 ms or 20 ms resolution. The absolute accuracy of all time stamps also depends on the protection relay's time synchronization.

Parameters

Table 338 - Status of the *GENGLOG*

Name	Short label	Infotip
Mod	Mode	Mode
SOENum	Total SOE	Total SOE

Table 339 - Control of the *GENGLOG*

Name	Short label	Infotip
ClrSOE	Clear SOE	Clear SOE

Operation log (*GENGLOG*)

Description

The PowerLogic P7 supports logging and recording of all IED operations including command, like:

- Operation (select, operate, select with value, cancel)
- Control block operation (active setting group (SG), edit SG, confirm, edit and enable GOOSE control block
- Setting change

Table 340 - Example of reset record log

Parameter	Value	Description
Date	2021-08-18	Time stamp of the log, date.
Time: hh:mm:ss.ms	16:45:51.000 ms	Time stamp, time of day.
Operation type	Operate	• *Select With Value* • *Select* • *Operation* • *Cancel* • *Active SG* • *Edit SG* • *Confirm Edit SG* • *GOOSE Enable* • *Edit Setting Value*
Operation status	Success	• *Initialize* • *Success* • *Failed*
Add cause	-	61850-7-2 table 54 Empty when operate success.
Label	IED_NameBayLD/ *DRRDRE*1.MemRs	Events.
Language reference	Reset Recorder Memory	Event simple text description.
Operation value	1	Operation value.

Table 341 - Example of disturbance recorder post trigger time change log

Parameter	Value	Description
Date	2021-08-18	Time stamp of the log, date.
Time: hh:mm:ss.ms	16:46:53.184 ms	Time stamp, time of day.
Operation type	Edit setting value	• *Select With Value* • *Select* • *Operation* • *Cancel* • *Active SG* • *Edit SG* • *Confirm Edit SG* • *GOOSE Enable* • *Edit Setting Value*
Operation status	Success	• *Initialize* • *Success* • *Failed*
Add cause	-	61850-7-2 table 54 Empty when operate success.
Label	IED_NameBayLD/ *DRRDRE*1.PstTmms	Event 61850 path.
Language reference	Pre-Trigger Time	Event simple text description.
Operation value	100	Operation value.

The IED operation logs can be read from the HMI under ☰ **> Logs > User operation log**.

The maximum size of the buffer is 500 logs. All operation logs are stored in non-volatile memory inside the PowerLogic P7. When the buffer is filled, the oldest entry will be overwritten by the new entry. The shown resolution of a time stamp for a log is one millisecond.

Parameters

Table 342 - Status of the *GENGLOG*

Name	Short label	Infotip
Mod	Mode	Mode
OperLogNum	Total operator records	Total operator records
MaxOperLog	Max operator records	Max operator records
OperStatus	Operation status	Operation status
OperAddcause	Operation addcause	Operation addcause
OperType	Operation type	Operation type

Table 343 - Control of the *GENGLOG*

Name	Short label	Infotip
ClrOperLog	Clear operator records	Clear operator records

Communication record

Description

The communication record function is used to capture network traffic of the Ethernet interfaces on the PowerLogic P7. The captured traffic can then be analyzed and help troubleshoot networking problems.

The capturing can only be manually triggered, either from the HMI under **Logs > Communication records > Status > Comms capture**, or by a control command from supported communication protocols. The Ethernet interface, protocols, and record time can be altered in the accompanying settings.

The size of one communication record is limited to 20 MB. When this limit is reached, the capturing process stops and generates a record file regardless of the configured record time. Otherwise, the capturing stops after the configured record time.

The generated communication records are PCAP files. Each interface can generate and store up to 3 records. Once this limit is reached, the oldest record will be overwritten by a new one.

NOTE:

- For HTTPS, the saved PCAP files are composed of raw TLS packets and a pre-master key file for decryption. The saved key file is limited to 64 KB.

Settings

Parameter	Description	Setting range	Step	Default value
Comms capture interface	Ethernet interface used to initiate the capture	• Redundant Ethernet • Single Ethernet	N/A	Redundant Ethernet
Protocol captured	Protocol(s) for the capture	• HTTPS (Webservice) • IEC 61850 MMS • DNP3 • Modbus • All protocols	N/A	All protocols
Comms capture time	Communication record duration	60...3600 s	10 s	60 s

Maintenance record

The PowerLogic P7 provides a detailed diagnostic record, which can be used by the Schneider Electric technical support team to investigate issues and troubleshoot the device.

The diagnostic record file can be downloaded from the PowerLogic Engineering Suite under **Device logs > Maintenance records > Diagnostic record**. This file in *.gz* format is encrypted and can only be read by the support team.

Disturbance record (*DRRDRE*)

Description

The PowerLogic P7 provides a disturbance recording with the sampled analog values of all used analog currents and voltages within a bay before, during and after a fault event.

Triggering the recording

The recording can be triggered by any start or trip signal from any protection stage, by a binary input, logic output or GOOSE signals. The triggering signal is selected in the matrix. The recording can also be triggered manually. All recordings are time-stamped. The record will start *Pre-trigger time* before the rise of the input and finish *Post-trigger time* after the fall of the input or expiration of *Max pulse length* timer or expiration of *Max record time* (whichever occurs first). Setting *Max pulse length* to zero provides fixed length records with a length of *Pre-trigger* + *Post-trigger* times.

The *Max record time* depends upon the storage rate and number of channels in the bay. It can be calculated by:
Max record time = 3275736000 / [(n + 3) × Storage rate]

Where n is the number of CT and VT channels mapped in the CT/VT groups.

Reading recordings

The recording is in COMTRADE format. This also means that other programs can be used to view and analyze the recordings made by the PowerLogic P7. The records are stored in *2013CFF* format with binary data.

Number of channels

A maximum of 200 records are stored with a mix of analog and binary signals:

- All analog channels used in the bay are recorded. Frequency and ROCOF are recorded. If differential elements are present, differential and bias values are recorded.
- All digital channels within the bay are recorded if they are active or changed during the recording period. All device binary signals (for example, binary input and output status) will also be included if active or changed during the recording period.

All records are stored in non-volatile memory in the PowerLogic P7.

When storage is full, the oldest record will be overwritten. (Max storage size is 300 MB).

Downloading disturbance records

The available disturbance records can be selectively downloaded to local PC from the PowerLogic Engineering Suite under **Bay 1 logs > Disturbance records**. Sorting options such as File name and Time stamp are provided to aid the selection process.

Disturbance record triggering matrix

With the PowerLogic Engineering Suite, navigate to **Bay 1 logs > Disturbance records** to set up the disturbance record matrix.

By default, the disturbance recorder is connected to the trip conditioner start signal to generate a record for any trip. It can also be connected to any other signal in the matrix to allow triggering for other conditions such as operation of other protection devices. The triggering signal is selected in the disturbance record triggering matrix.

Signals

Table 344 - Status of the *DRRDRE*

Name	Short label	Infotip
RcdStr	Recording started	Active when the trigger input is high
RcdMade	Recording made	High for 1s after a new record is available
FltNum	Number of records	Number of disturbance records available
MaxRcdTime	Max record time	= 3275736000 / [(n + 3) × Storage rate] where n is the number of CT and VT channels mapped in the CT/VT groups

Table 345 - Control of the *DRRDRE*

Name	Short label	Infotip
MemRs	Reset recorder memory	Delete all disturbance records
RcdTrg	Trigger recorder	Triggers the recorder with a 5ms pulse

Setting parameters

Table 346 - Settings of the *DRRDRE*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		On
PreTmms	Pre-trigger time	Record length before trigger goes high	10...1000000 ms	10 ms	100 ms
PstTmms	Post-trigger time	Record length after trigger goes low or max pulse time is reached	10...1000000 ms	10 ms	100 ms
PulTmms	Max pulse time	Maximum trigger pulse time. The DR will record for pre-time + post-time + trigger pulse time up to this maximum. If set zero the record length is fixed.	0...1000000 ms	10 ms	1000 ms
ReTrgModEx	Re-trigger mode	If the trigger operates during post-trigger time the record is extended	• Off • On		Off
StoRteDR	COMTRADE storage rate	14400Hz will record at 4800Hz if more than 18 local CTVT inputs or 4000Hz/5760Hz SV publishing are used. For 4000Hz/5760Hz SV publishing the actual storage rate is SV publishing rate/4800*COMTRADE storage rate. For example, with a SV publishing rate of 4000Hz and a COMTRADE storage rate set to 1200Hz the rate will be 4000/4800*1200=1000Hz	• 14400 Hz • 4800 Hz • 2400 Hz • 1200 Hz • 600 Hz		4800 Hz
ComtradRev	COMTRADE file revision	COMTRADE file revision	• 2013CFF		2013CFF
ComtradFmt	COMTRADE file format	COMTRADE file format	• Binary		Binary

Fault record (*TCRGLOG*)

Description

Fault record provides fault signals including the measured fault data captured during a fault sequence. The fault records are logged in chronological order with reference to the specific fault.

Each bay has independent fault record. The fault record is triggered by any start and any trip signals which are connected by default in the matrix to *PTRC*. The fault record details any protection operations when the *PTRC* is started.

When any start or any trip picks up, the fault record starts to record. A new fault record is generated if any protection function operates during the recording period. This record is discarded if no protection function operates during the recording period.

Table 347 - Example of fault record

Type	Parameters	Description	Value
General information	Date	Time stamp of the fault record, date.	2021-08-18
	Time	Time stamp, time of day.	16:46:53.184 ms
	Device name	Device name.	IED_2
	Bay name	Bay name.	Feeder1
	Fault duration	Fault duration. The time between first protection start and the last protection dropout.	200 ms
	Pre-fault data	General analog data 2 power cycles before the rising edge of any protection start.	Prefault IA: 0.74 A -109.2 deg Prefault IB: 0.00 A 0.0 deg Prefault IC: 0.00 A 0.0 deg Prefault IX: 0.00 A 0.0 deg Prefault VA: 0.00 V 0.0 deg Prefault VB: 0.00 V 0.0 deg Prefault VC: 0.00 V 0.0 deg Prefault VX: 0.00 V 0.0 deg
	Fault data	General analog data 1 power cycle after the rising edge of any protection operation.	Fault IA: 1.98 A -107.5 deg Fault IB: 0.00 A 0.0 deg Fault IC: 0.00 A 0.0 deg Fault IX: 0.00 A 0.0 deg Fault VA: 0.00 V 0.0 deg Fault VB: 0.00 V 0.0 deg Fault VC: 0.00 V 0.0 deg Fault VX: 0.00 V 0.0 deg
Event 1	Date	Time stamp of the fault record (date).	2021-08-18
	Time	Time stamp (time of day).	16:46:53.184 ms
	Active setting group/ ActSg	Active setting group of this function.	1
	Label	Event source.	IED_2BayLD/*PHPTOC*1.Str
	Event status	Full data attribute status of this event data object. This is depending on each function definition.	General: True Direction: Unknown Phase A: True Directional Phase A: Unknown Phase B: False Directional Phase B: Unknown Phase C: False Directional Phase C: Unknown
Event 2	Date	Time stamp of the fault record (date).	2021-08-18
	Time	Time stamp (time of day).	16:46:53.184 ms
	Active setting group/ ActSg	Active setting group of this function.	1
	Label	Event 61850 path.	IED_NameBayLD/*PHPTOC*1.Op

Table 347 - Example of fault record (Continued)

Type	Parameters	Description	Value
	Event status	Full data attribute status of this event data object. This is depending on each function definition.	General: True Phase A: True Phase B: False Phase C: False
	Function measurement	Actual measurements are detailed in the individual function sections.	I> Stage 1.1A FFT:1.98 A -107.5 deg I> Stage 1.1B FFT:0.000 0.0 deg I> Stage 1.1C FFT:0.000 0.0 deg

The fault record can be read from the HMI under ☰ **> Logs > Bay 1 > Fault records**.

The maximum size of the buffer is 50 fault records. All events are stored in non-volatile memory in the PowerLogic P7. When the buffer is full, the oldest record will be overwritten when a new record is generated. The resolution of time stamp for a fault event is one millisecond.

Signals

Table 348 - Status of the *TCRGLOG*

Name	Short label	Infotip
Mod	Mode	Mode
FltNum	Fault number	Fault number
FltTms	Fault duration	Fault duration
MaxFltRcd	Max fault records	Max fault records

Table 349 - Control of the *TCRGLOG*

Name	Short label	Infotip
FltClr	Clear fault records	Clear fault records

Fault locator (*RFLO*, ANSI 21FL)

Description

The Fault locator function is applied to determine the distance to the fault location. The fault locator samples data from the analog current and voltage inputs which is fixed to TCTT1/TVTT1 and writes it to a cyclic buffer until a fault condition is detected. The data in the input buffer is then held to allow the fault calculation to be made and to determine the distance to fault location. The calculated location of the fault is sent to the fault record for the fault.

Fault point scan

The fault locator stores the sampled data within a 20-cycle cyclic buffer at a resolution of 48 samples per cycle. The fault location is calculated based on the sampled data in the buffer. When the fault location calculation is triggered by the *Start* signal from the *PTRC*, the data in the buffer is frozen so that the buffer contains 10 cycles of pre-fault data and 10 cycles of post-fault data. Fault calculation starts shortly after this trigger point.

To identify the exact fault point, a total of four cycles of sample data will be scanned, which includes two cycles of pre-fault data and two cycles of post-fault data. If two consecutive sample points meet the following condition, the second sample point will be identified as the fault point.

$|i_{ph}(n) - i_{ph}(n–48)| \geq |0.125 \times i_{ph}(n-48)|$

Where:

$i_{ph}(n)$: Sample value of Phase A, B, C

$i_{ph}(n–48)$: Sample value of the previous cycle of Phase A, B, C

Faulted phase selection

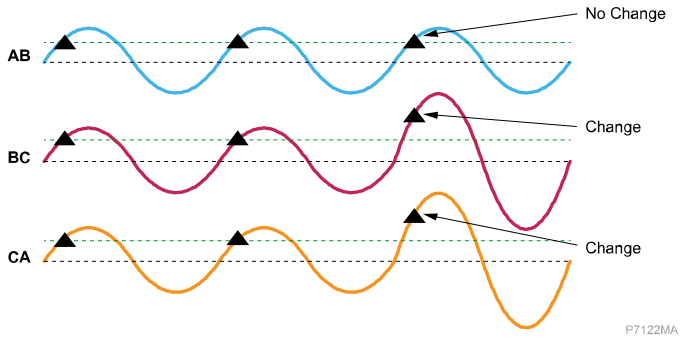
The selection of the faulted phase(s) is performed by comparing the magnitudes of the three phase-to-phase delta currents. The delta current is $FFT_{Post\text{-}fault}$ minus $FFT_{Pre\text{-}fault}$.

A single phase-to-ground fault produces the same delta currents on two of these signals and zero on the third. A phase-to-phase or double phase-to-ground fault produces one delta current which is larger than the other two. A three-phase fault produces three delta currents which are the same size. A delta current is deemed to be large enough to be included in faulted phase selection only when it's greater than 80% of the maximum delta current.

The following diagram takes a single phase-to-ground fault of Phase C as an example to show how the delta currents can be used to select the faulted phase (s), where,

$Delta_{BC} > 0.8 \times \max(Delta_{AB}, Delta_{BC}, Delta_{CA})$

$Delta_{CA} > 0.8 \times \max(Delta_{AB}, Delta_{BC}, Delta_{CA})$



From the diagram, $Delta_{BC}$ and $Delta_{CA}$ are considered in determining the faulted phase, and a single phase-to-ground fault of Phase C is identified.

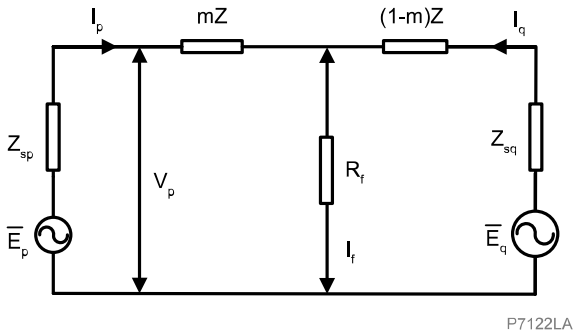
Fault location calculation

The calculation works by obtaining the vectors, estimating the phase of the fault current I_f, and solving Equation (1) for fault location in percentage m at the instant of time where $I_f = 0$.

Basic theory of fault location

A two-machine equivalent circuit of a faulted power system is shown below.

Figure 229 - Two-machine equivalent circuit diagram



From the diagram, the fault location in percentage *m* can be calculated by estimating the fault current I_f and solving the following equation for fault location.

$$V_p = I_p \times mZ + I_f \times R_f \quad (1)$$

Obtaining the vectors

Different sets of vectors are chosen depending on the type of fault identified by the phase selection algorithm. The calculation using Equation (1) is applied for either a phase-to-ground fault or a phase-to-phase fault.

- For phase-to-ground fault, take Phase A for example:

  $V_p = V_A$

  $I_p \times Z = I_A \times Z_1 + I_N \times Z_1 \times kZn$

  $I_f = \Delta I_A - 1/3 \times \Delta I_N$
- For phase-to-phase fault, take Phase A to Phase B for example:

  $V_p = V_A - V_B$

  $I_p \times Z = I_A \times Z_1 - I_B \times Z_1$

  $I_f = \Delta I_A - \Delta I_B$

Where:

- V_A, V_B, V_C: Phases voltage (Post-fault FFT value) detected
- I_A, I_B, I_C: Phases current (Post-fault FFT value) detected
- ΔI_A, ΔI_B, ΔI_C: Delta current of three phases, Post-fault FFT current minus Pre-fault FFT current
- $I_N = I_A + I_B + I_C$
- ΔI_N: Delta I_N, Post-fault FFT I_N minus Pre-fault FFT I_N
- Z_1: Positive sequence line impedance
- Z_0: Zero sequence line impedance
- $kZn = (Z_0 - Z_1)/3Z_1$: Residual compensating factor

Solving the equation for the fault location

When the sine wave of instantaneous fault current I_f passes through zero ($I_f R_f$=0), the instantaneous values of the sine waves V_p and I_p can be used to solve Equation (1) for fault location in percentage *m*. This is determined by shifting the calculated vectors of V_p and I_pZ by the angle I_f, and then dividing the imaginary component of V_p by the imaginary component of I_pZ.

$$V_p^{'} = V_p \times \frac{-\varphi\left(I_f\right)}{\left|I_f\right|}$$

E71200A

$$(I_p \times Z)' = (I_p \times Z) \times \frac{-\varphi(I_f)}{|I_f|}$$ E71201A

$$m = \frac{imag(V_p')}{imag((I_p \times Z)')}$$ E71202A

The fault percentage is then given by *m*. The fault location in impedance *FltZ* can be calculated by multiplying *m* by the line impedance setting Z_1. The fault location in distance *FltDiskm* can be calculated by multiplying *m* by the line length setting *LinLenkm*. *FltDisMile* is also provided to indicate the distance in miles.

FltZ = *m* × Z_1

FltDiskm = *m* × *LinLenkm*

FltDisMile = *0.62137* × *FltDiskm*

Example of setting line parameters

Assuming the following data for the protected line:

400 kV transmission line

CT ratio	=	1200/1
VT ratio	=	400,000/100
Line	=	10 km

Positive sequence line impedance Z_1	=	0.089 + *j*0.476 Ohms/km = 0.484 ∠79.4° Ohms/km
Zero sequence line impedance Z_0	=	0.34 + *j*1.03 Ohms/km = 1.085 ∠71.7° Ohms/km

The line impedance magnitude and angle settings are calculated as follows:

Ratio of secondary to primary impedance	=	CT ratio/VT ratio = 0.3
Positive sequence line impedance Z_1	=	0.3 × 10 × 0.484 = 1.45 Ohms (secondary value)
Per Unit value of Z_1	=	1.45/57.74 = 0.0251 pu

Therefore, set

Magnitude Z_1	=	0.025
Angle Z_1	=	79°

The zero sequence line impedance Z_0 is calculated in the same way:

Zero sequence line impedance Z_0	=	0.3 × 10 × 1.085 / 57.74 = 0.056 pu

Therefore, set

Magnitude Z_0	=	0.056
Angle Z_0	=	72°

Input and output signals

Table 350 - Input signals of the *RFLO*

Name	Short label	Infotip
Str	Start	Start signal from protection to initiate fault location

Table 351 - Output signals of the *RFLO*

Name	Short label	Infotip
FltPercent	% of line	% of line
FltDiskm	Distance in km	Fault distance in km
FltDisMile	Distance in miles	Fault distance in miles
FltZ	Impedance	Impedance
FltLoop	Fault loop	Faulted phase(s) loop

Setting parameters

Table 352 - Settings of the *RFLO*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Fault location	Enables fault location	• On • Off		Off

The *RFLO* takes the reference setting values from the *ZLIN*, where power overhead line settings are defined.

Table 353 - Settings of the *ZLIN*

Name	Short label	Infotip	Setting range	Step size	Default setting
LinLenkm	Line length	Line length	0.001...1000 km	0.001 km	10 km
ZPsMag	Z1 impedance	Z1 impedance	0.001...10 pu	0.001 pu	0.06 pu
ZPsAng	Z1 angle	Z1 angle	10...90 deg	1 deg	70 deg
ZZerMag	Z0 impedance	Z0 impedance	0.001...10 pu	0.001 pu	0.24 pu
ZZerAng	Z0 angle	Z0 angle	0...90 deg	1 deg	70 deg

Characteristics

Table 354 - Characteristics of the *RFLO*

Characteristics		Values
Fault location in impedance	Accuracy	±2%[15]

During testing, the fault values should be retained for >50 ms to simulate a breaker opening time and create the correct pre-fault and post-fault values for accurate fault location.

To improve the accuracy during transient state, the fault location value will be calculated several times (maximum 4 times). Each calculation of the fault location value is based on different Post-fault FFT values, each time moving 1 cycle to get

15. The performance here is in ideal sinusoidal wave condition. The actual performance will be affected by DC offset, CT saturation and fault resistance.

a new Post-fault FFT value. Only the final value with a deviation of less than 0.01 to the previous value will be considered a valid output.

Fault measurement (*RFMX*)

Description

The pre-fault data and fault data comes from the *RFMX*. Pre-fault data is the general analog data two cycles before the rising edge of any start. Fault data is the general analog data one cycle after the rising edge of any trip. A subsequent trigger is only possible when the record is complete. The fault record is generated and saved after any start and trip reset. Each fault record has a maximum of 50 protection events.

Input and output signals

Table 355 - Input signals of the *RFMX*

Name	Short label	Infotip
AnyStr	Start	Start signal used for timing if operation occurs
AnyTr	Operate	Operate signal used to generate fault record
TriVectorIn1	Phase current	Internal signal from PHTCTT1
TriVectorIn2	Phase voltage	Internal signal from PHTVTT1
FloatIn1	Frequency	Internal signal from FTGAPC1

Table 356 - Output signals of the *RFMX*

Name	Short label	Infotip
StartLog	Start log	Start log
FltA	Fault current	Fault current
FltPhV	Fault phase voltage	Fault phase voltage
FltHz	Fault frequency	Fault frequency

Alarm and trip (*CALH*)

Description

The PowerLogic P7 will turn on the Alarm LED and Trip LED on the front panel in the event of abnormal system condition or failures of the protection relay. The Alarm LED and Trip LED are affected by the alarm and trip status configured.

The alarm and trip function is modelled by Logical Node *CALH* in IEC 61850 to store the alarm and trip status, settings and control data objects.

Up to 128 alarm and 8 trip inputs are available for the user. An alarm and a trip can be given a category, severity and label. The behavior of each alarm and each trip depends on the settings and configurations in database. Each alarm and trip can be selected between self-reset and latched. can be selected, and can be controlled by command to reset status in latched mode separately or all together.

Input and output signals

Table 357 - Status of the *CALH*

Name	Short label	Infotip
AlmNum	Active alarms	Active alarms
AlmSt1	Alarm 1 status	Alarm 1 status
.....	.....	.....
AlmSt128	Alarm 128 status	Alarm 128 status
TripNum	Active trips	Active trips
TripSt1	Trip status 1	Trip status 1
.....	.....	.....
TripSt8	Trip status 8	Trip status 8

Table 358 - Control of the *CALH*

Name	Short label	Infotip
AlmAllRst	Reset all alarms	Reset all alarms
AlmRst	Reset alarm	Reset alarm
TripAllRst	Reset all trips	Reset all trips
TripRst	Reset trip	Reset trip

NOTE: The value of *AlmSt1* to *AlmSt128* and *TripSt1* to *TripSt8*:

- 0: The alarm is inactive.
- 1: The alarm condition is active and the alarm is not acknowledged.
- 4: The alarm condition is no longer met, the alarm is still active because it is latched, and it is not acknowledged.

Setting parameters

Table 359 - Settings of Alarm (*CALH*)

Name	Short label	Infotip	Setting range	Step size	Default setting
AlmSt1Cat	Alarm 1 category	Alarm 1 category	• Power system • Monitored device • Sensors • IED		Power system
.....	.....	.....	.....	.....	.....
AlmSt128Cat	Alarm 128 category	Alarm 128 category	• Power system • Monitored device • Sensors • IED		Power system
AlmSt1Sev	Alarm 1 severity	Alarm 1 severity	• Minor • Medium • Major		Minor
.....	.....	.....	.....	.....	.....
AlmSt128Sev	Alarm 128 severity	Alarm 128 severity	• Minor • Medium • Major		Minor
AlmSt1Lat	Alarm 1 latch	Alarm 1 latch	• true • false		true
.....	.....	.....	.....	.....	.....

Table 359 - Settings of Alarm (*CALH*) (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
AlmSt128Lat	Alarm 128 latch	Alarm 128 latch			true
AlmSt1Lab	Alarm 1 label	Alarm 1 label			Alarm1
.....	.....	.....	.....	.....	.....
AlmSt128Lab	Alarm 128 label	Alarm 128 label			Alarm 128
TripSt1Cat	Trip category 1	Trip category 1	• Power system • Monitored device • Sensors • IED		Power system
.....	.....	.....	.....	.....	.....
TripSt8Cat	Trip category 8	Trip category 8	• Power system • Monitored device • Sensors • IED		Power system
TripSt1Sev	Trip severity 1	Trip severity 1	• Minor • Medium • Major		Minor
.....	.....	.....	.....	.....	.....
TripSt8Sev	Trip severity 8	Trip severity 8	• Minor • Medium • Major		Minor
TripSt1Lat	Trip latch 1	Trip latch 1	• true • false		true
.....	.....	.....	.....	.....	.....
TripSt8Lat	Trip latch 8	Trip latch 8	• true • false		true
TripSt1Lab	Trip Conditioner 1	Trip Conditioner 1			Trip1
.....	.....	.....	.....	.....	.....
TripSt8Lab	Trip Conditioner 8	Trip Conditioner 8			Trip 8

NOTE: The setting *AlmStLab* is not configurable from the HMI and can only be configured by the PowerLogic Engineering Suite.

Monitoring functions

Trip conditioner (*PTRC*, ANSI 86)

Description

The Trip conditioner function provides the combination of all protection functions' start outputs and operate outputs to a general start and a general operate respectively, according to the start and operate I/O mapping of *PTRC* for each protection. The general operate will trigger the general trip signal which can be directly connected to a binary output to trip the breaker.

The trip signal has a settable minimum dwell or can be set to always latch. It also has a latch input which will force a latched trip if active with an operate input. A latched trip can be cleared by the reset button, or a matrix or control input providing the operate signal is not still active.

Trip conditioner matrix

The trip conditioner is used to group all the protection start and operate signals together to provide an overall start and trip signal for the bay. The start signal is normally connected to the fault log and disturbance recorder. The operate is also connected to the fault record as well as operating the trip LED. The start and operate signals directly follow the connected inputs. A trip output is also provided by the trip condition. This is for connection to circuit breaker trip coils and will provide a dwell or latch on according to settings and inputs. Setting the Lock out mode to enable will cause the trip output to latch for any element operation.

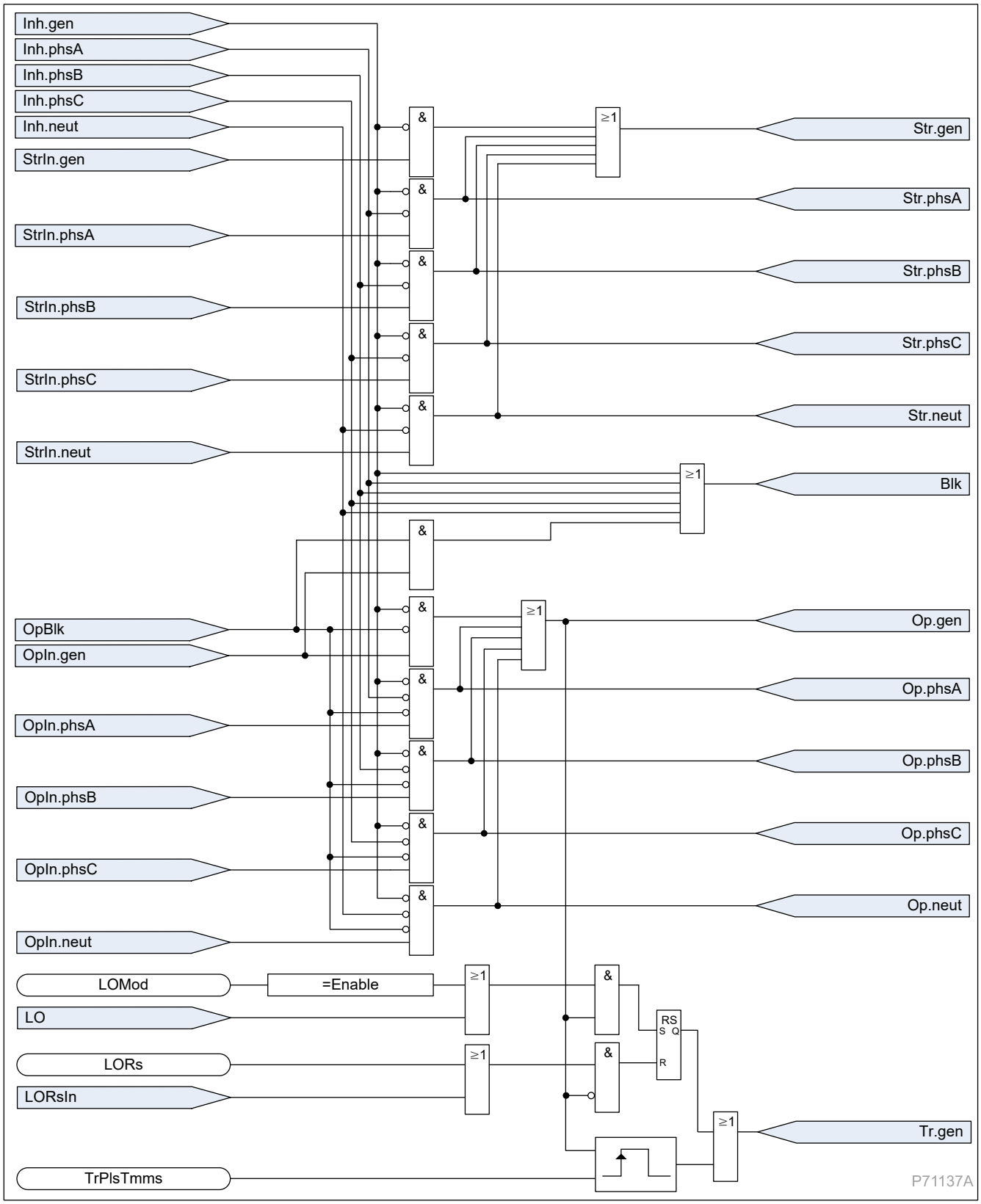
The start and operate input signals are linked by default to all the protection functions which are normally used for tripping. If a link is removed the element will still function but will not initiate trips through the conditioner. An additional lockout input is available which will latch the trip signal if present when the operate signal is active. This allows individual protection functions to latch the trip signal.

PTRC's block and reset input signals can also be connected through the matrix. The block input will block all PTRC's outputs. The reset input can reset lock out mode of PTRC trip output. The PTRC is also reset when the Reset button is pushed or a SCADA reset is issued. The trip LED also affects the display. If the display has timed out (is blank) it will turn on and display the virtual LED page. If the display is active when the trip LED turns on then the display will change to the virtual LEDs after the timeout period or a maximum of 15 minutes. When the trip LED is reset the display will time out if not being used.

With the PowerLogic Engineering Suite, expand **Bay 1 protection > Trip > Trip conditioner** to set up the PTRC matrix.

Block diagram

Figure 230 - Block diagram of the *PTRC*



NOTE: If the *Lockout* input is active with the operate from the protection functions, then the trip command will be set until the reset is received.

Input and output signals

Table 360 - Input signals of the *PTRC*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
OpBlk	Op block	Output blocked when active. This allows the output to be checked by another function
StrIn[general;phsA;phsB;phsC; neut]	Start	Initiates start output
OpIn[general;phsA;phsB;phsC; neut]	Operate	Initiates operate and trip outputs
LO	Lockout	Trip is locked out (latched) when this input is active providing the Operate input is also active
LORsIn	Reset LO	Reset lockout

Table 361 - Output signals of the *PTRC*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
Tr	Trip	Trip
Blk	Blocked	Blocked
LORs	Reset lockout	Reset lockout

Setting parameters

Table 362 - Settings of the *PTRC*

Name	Short label	Infotip	Setting range	Step size	Default setting
LOMod	Lockout mode	This forces the trip output to lockout for any connected operate signal. Individual signals can lockout via matrix input	• Off • On		Off
TrPlsTmms	Trip pulse time	This is the minimum trip pulse time (dwell) when a connected operate signal is active	0...10000 ms	1 ms	200 ms

Characteristics

Table 363 - Characteristics of the *PTRC*

Characteristics		Values
Minimum trip Pulse	Accuracy	±2% or ±10 ms

Current transformer supervision (*CTSSCTR*)

Description

The current transformer supervision (CTS) feature is included with each 3ph CT group and is used to detect failure of a phase current input to the protection device. Failure of a phase CT or an open circuit of the interconnecting wiring can result in:

- Incorrect operation of protection functions
- High CT secondary voltages

The CT connection types 3ph, 3ph+N and 2ph+N are monitored.

By default the CTS will mark all CT measurements as invalid. This is set via a matrix link between the CTS block (*CTSSCTRx.CTSBlk*) and the CT fault (*PHTCTTx.Fault*) input. This link can be removed and selected functions blocked if required. Elements to be blocked should have a minimum operate delay of at least 50 ms. CTS should not be applied to groups used for *HIZPDIF*. These elements have an inbuilt CTS function suited to this application. CTS can be applied to the bias differential element with instantaneous operation providing the *Saturation time constant* is set to at least 100 ms.

Supervision of the phase currents

The CT failure is detected when the following conditions are simultaneously present:

- The magnitude of one phase current falls below 1% In.
- The magnitude of the other two phase currents is within 5%...120% In.
- The angle between the other two phase currents is from 110° to 130°. The angle determination for phase loss detection is listed in the table below.

Table 364 - Angle determination for phase loss detection

Phase rotation	Loss of phase A	Loss of phase B	Loss of phase C
ABC	110° < φ (IB, IC) < 130°	110° < φ (IC, IA) < 130°	110° < φ (IA, IB) < 130°
ACB	110° < φ (IC, IB) < 130°	110° < φ (IA, IC) < 130°	110° < φ (IB, IA) < 130°

When the CT failure is detected without a blocking condition, the function issues a block signal after 20 ms and a delayed alarm after the operate delay has elapsed.

The CT failure alarm resets after 10 s if one of the following conditions applies:

- The maximum phase current falls below 10% In.
- The minimum phase current exceeds 10% In.

Supervision of the neutral current

If the delta IN operation mode *INdiffMod* is enabled and the CT connection type is 3ph+N, the CTS function triggers when the difference of the calculated neutral current and the measured neutral current exceeds the set threshold. This should only be enabled when IN is connected to a residual (Holmgren) connection of the three phase CTs.

Blocking conditions

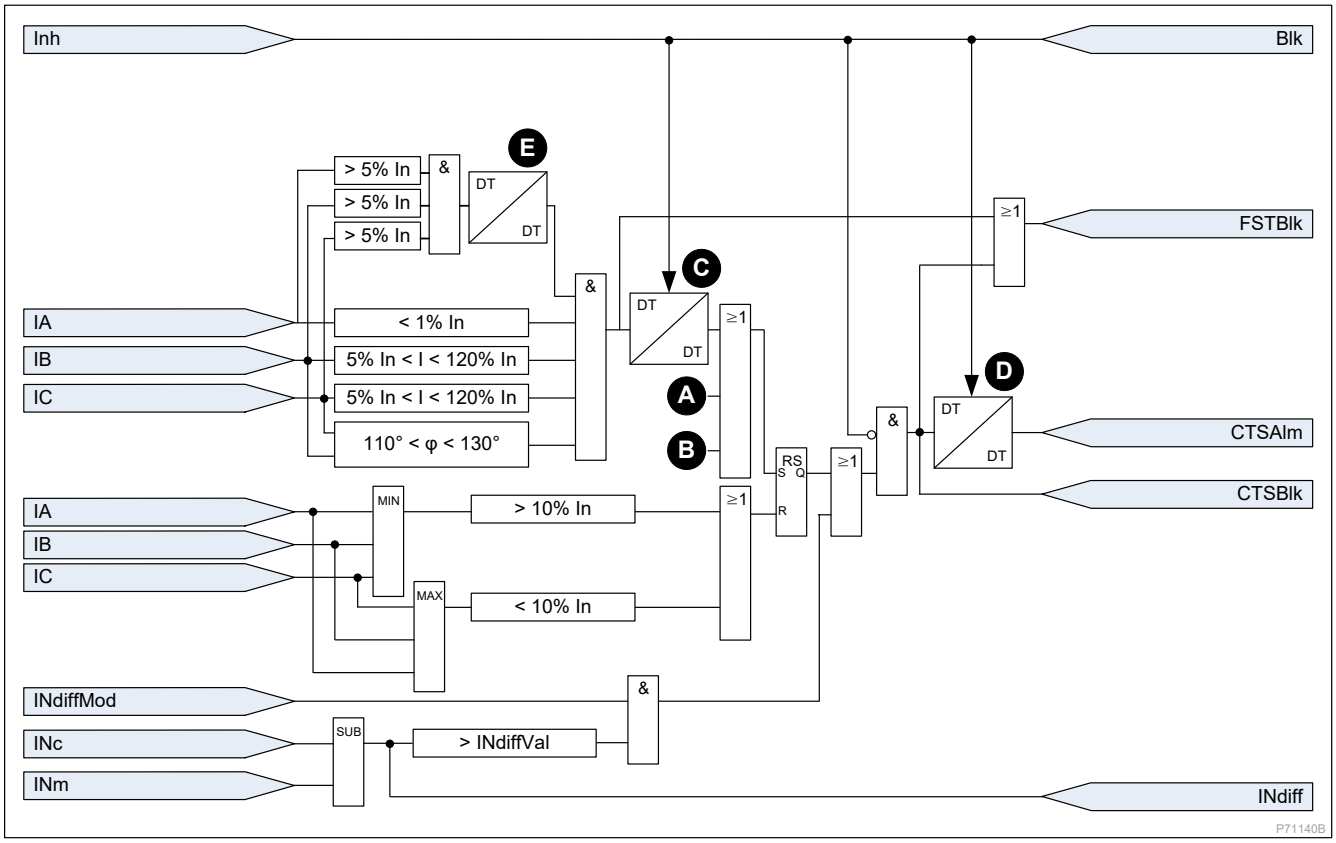
CTS will indicate a *Blocked* status when not fully functional under the following conditions:

- The *Inhibit* input is present.
- The CT connection type is 3ph and *INdiffMod* is enabled.
- The CT connection type is 2ph+N and *INdiffMod* is enabled.
- The CT connection type is 2ph and *INdiffMod* is enabled.

Block diagram

When the CT failure is detected without a blocking condition, the function issues a block signal and a delayed alarm after the operate delay has elapsed.

Figure 231 - Block diagram of the *CTSSCTR*



A	Loss of phase B	B	Loss of phase C	C	Operate delay: 20 ms Reset delay: 0 ms
D	Operate delay: *OpDITmms* Reset delay: 10 s	E	Operate delay: 0 ms Reset delay: 1 s		

Input and output signals

Table 365 - Input signals of the *CTSSCTR*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function

Table 366 - Output signals of the *CTSSCTR*

Name	Short label	Infotip
CTSBlk	Block	Block
FSTBlk	Fast block	Fast block

Table 366 - Output signals of the *CTSSCTR* (Continued)

Name	Short label	Infotip
CTSAlm	Alarm	Alarm
Blk	Blocked	Blocked
INdiff	IN diff	IN diff

Setting parameters

Table 367 - Settings of the *CTSSCTR*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	The function will operate when one current is lost while the other two currents are in the normal load range	• On • Off		Off
OpDlTmms	Alarm delay	Time delay from Block to Alarm output activation. Alarm has 10s fixed reset	0...10000000 ms	1 ms	5000 ms
INdiffMod	IN diff mode	When the CT mode is IA IB IC IN this compares the measured IN to IA + IB + IC	• Off • On		Off
INdiffVal	IN diff start value	IN differential above this level will operate CTS	0.001...40 pu	0.001 pu	0.1 pu

Characteristics

Table 368 - Characteristics of the *CTSSCTR*

Characteristics		Values
IN diff start value	Accuracy	±3%
	Reset ratio	98% ± 2%
Operate delay	Accuracy	±2% or ±10 ms
Reset delay (fixed)	DT timer – Accuracy	±10 ms
Characteristic time	Disengaging time	< 60 ms

Voltage transformer supervision (*VTSSVTR*, ANSI 60FL)

Description

The voltage transformer supervision (VTS) feature is included with each 3ph VT group and is used to detect failure of the voltage inputs to the protection device. If there is a fuse in the voltage transformer circuitry, the blown fuse prevents or distorts the voltage measurement. Therefore, a VTS alarm should be issued. Furthermore, in some applications, protection functions using voltage signals should be blocked to avoid false tripping.

- Neutral overvoltage and directional ground fault overcurrent using calculated neutral voltage
- Phase undervoltage
- Directional phase overcurrent
- Directional overpower and underpower

VT failure is detected for the following conditions:

- Loss of one or two phase voltages (for 2pp+N, 3ph and 3ph+N VT connection types)

  The VTS feature operates on detection of the presence of negative sequence voltage and the absence of negative sequence current. The following conditions are simultaneously present:

  - No block V2 input
  - V2 exceeds the relevant threshold
  - Bay I2 below the relevant threshold
  - Maximum bay phase current exceeds the *IminStrVal* setting
- Loss of all three phase voltages under load conditions or upon line energization (for 2pp+N, 3ph and 3ph+N VT connection types)

  When the maximum phase bay current is above *IminStrVal* but below *ImaxStrVal*, and the three phase-to-phase voltages are less than *VmaxStrVal*, a VT failure is detected.

  NOTE: When *ImaxStrVal* is set to 0, 3ph loss detection is disabled.
- Supervision of the neutral voltage (for 3ph+N VT connection type)

  If the *VN diff mode* is enabled, the VTS function triggers when the difference of the calculated neutral voltage and the measured neutral voltage exceeds the set threshold.
- DI for external VT failure indication (for all VT connection types)

When the VT failure is detected without an inhibit input, the function issues a block signal and a delayed alarm after the operate delay has elapsed.

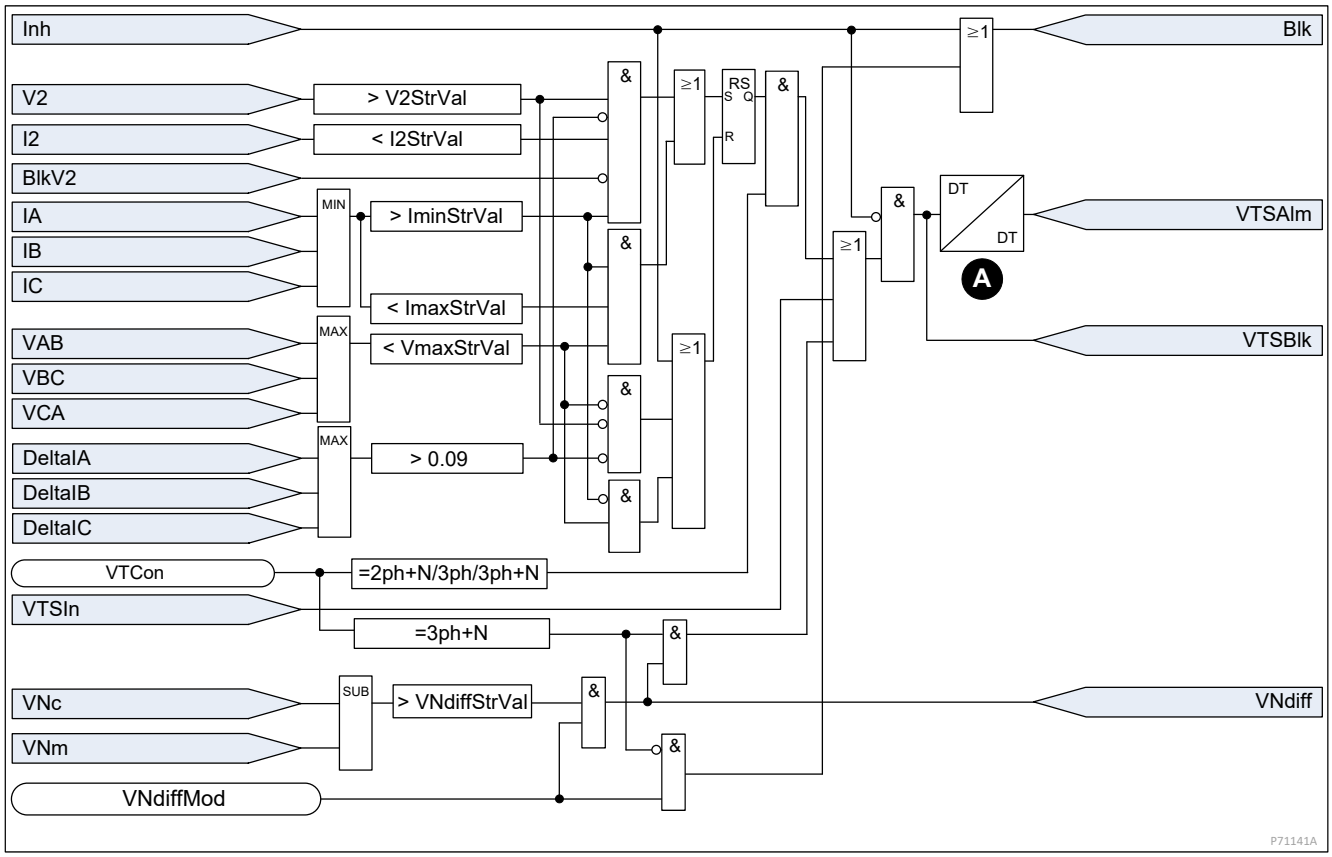
By default the VTS will mark all VT measurements as invalid. This is set via a matrix link between the VTS block (*VTSSVTRx.VTSBlk*) and the VT fault (*PHTVTTx.Fault*) input. This link can be removed and selected functions blocked if required.

The VTS alarm (caused by V2 and loss of all three phase) resets after 10 s if one of the following conditions applies:

- The inhibit input is present.
- The maximum phase current falls below the load current and the maximum phase-to-phase voltage is below *VmaxStrVal*.
- The V2 falls below the relevant threshold and the maximum phase-to-phase voltage is above *VmaxStrVal*.

Block diagram

Figure 232 - Block diagram of the *VTSSVTR*



A Operate delay: *OpDITmms*
Reset delay: 10 s

Input and output signals

Table 369 - Input signals of the *VTSSVTR*

Name	Short label	Infotip
Inh[general]	Inhibit	Inhibit function
BlkV2	V2 block	Block VTS V2/I2 operation (1 pole open)
VTSIn	MCB	External VTS initiation (MCB)
IAIBIC	Phase current	Internal signal from PHTCTT1
I2	I2	Internal signal from PHTCTT1

Table 370 - Output signals of the *VTSSVTR*

Name	Short label	Infotip
VTSBlk	Block	Block
VTSAlm	Alarm	Alarm
Blk	Blocked	Blocked
VNdiff	VN diff	VN diff

Setting parameters

Table 371 - Settings of the *VTSSVTR*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
OpDITmms	Operate delay	Time delay from Block to Alarm output activation. Alarm has 10s fixed reset	0...10000000 ms	1 ms	5000 ms
IminStrVal	Min current check value	This current must be present for operation except for VN diff	0.005...40 pu	0.001 pu	0.05 pu
V2StrVal	Neg seq OV start value	Negative sequence voltage above this level without blocking current will operate NPS VTS	0.1...2 pu	0.001 pu	0.2 pu
I2StrVal	Neg seq OC block value	Negative sequence current above this level will block NPS VTS	0.005...40 pu	0.001 pu	0.05 pu
VmaxStrVal	3ph UV start value	All phases below this level without blocking current will operate 3ph VTS	0.1...2 pu	0.01 pu	0.1 pu
ImaxStrVal	3ph OC block value	All phases above this level will block 3ph VTS	0...40 pu	0.001 pu	10 pu
VNdiffMod	VN diff mode	When the VT mode is VA VB VC VN this compares the measured VN to VA + VB + VC	• Off • On		Off
VNdiffStrVal	VN diff start value	VN differential above this level will operate VTS	0.1...2 pu	0.01 pu	0.1 pu

Characteristics

Table 372 - Characteristics of the *VTSSVTR*

Characteristics		Values
Neg seq OV start value	Accuracy	±2%
	Reset ratio	98% ± 2%
Neg seq OC block value	Accuracy	±5%
	Reset ratio	105% ± 2%
Min current check value	Accuracy	±5%
	Reset ratio	95% ± 2%
3ph OC block value	Accuracy	±5%
	Reset ratio	105% ± 2%
VN diff start value	Accuracy	±2%
	Reset ratio	98% ± 2%
Block	Block time accuracy	< 30 ms
	Reset time accuracy	< 30 ms
	Accuracy	±2% or ± 0.001 pu
Operate delay	Accuracy	±2% or ±10 ms
Reset delay (fixed)	DT timer – Accuracy	±10 ms
Characteristic time	Disengaging time	< 60 ms

Circuit breaker supervision (*CBSCBR*)

Description

Periodic maintenance of Circuit Breakers (CB) is necessary to ensure that the trip circuit and mechanism operate correctly and the interrupting capability is uncompromised due to the previous fault interruptions. The circuit breaker supervision function is included in each CB package and records various statistics related to each CB operation, allowing an accurate assessment of the CB condition. Statistics are recorded to allow the evaluation of both the electrical wear of the breaker contacts and the mechanical wear of the breaker mechanism.

Electrical wear

Cumulative broken current

The cumulative broken current function calculates the accumulated fault current following the trip order input per phase basis if CB is open later. The calculation formula is ΣI^{y}, the factor *y* depends on the type of the CB.

The greatest broken current of three-phase is used as the operation quantity. If the operation quantity is greater than the warning threshold, this function will issue warning signals. If the operation quantity is greater than the alarm threshold, this function will issue alarm signals.

When the broken current threshold for warning is set to *0*, the warning function is disabled.

When the broken current threshold for alarm is set to *0*, the alarm function is disabled.

Mechanical wear

CB open counter

The CB open counter is to record the number of CB close to open.

Protection trip counter

The protection trip counter is to record CB open times issued from global trip.

Open time and close time

- Open time is the time interval between general trip signal is valid or the control opening is successful and CB status is open.
- Close time is the time interval between close signal is valid and CB status is close.

Days without operation

The days without operation is calculated as the total days the CB remains closed from its last operation or since PowerLogic P7 power up.

All statistics are not incremented when the PowerLogic P7 is in test mode. The CB supervision data are managed as follows:

- Cumulative broken current: not incremented
- CB open counter: not incremented
- Protection trip counter: not incremented
- Operating time (open and close time): recorded
- Days without operation: unaffected

For **CB open counter**, **protection trip counter** and **open time and close time**, two thresholds can be set on each of them. One threshold is to produce a warning

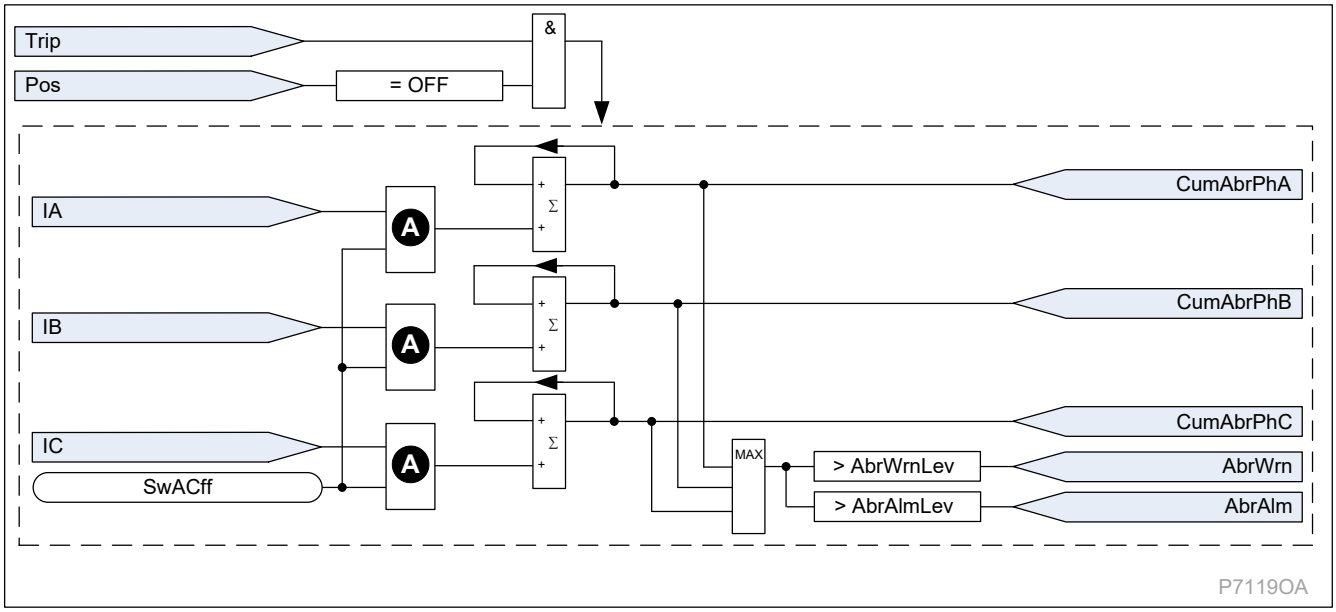
for maintenance purpose and the other is to produce an alarm for lock out purpose.

For **days without operation**, the threshold for alarm can be set on each of them.

NOTE: Each one of these warnings and alarms will raise a CB maintenance general status information.

Block diagram

Figure 233 - Cumulative broken current block diagram of the *CBSCBR*



A Accumulated energy

Input and output signals

Table 373 - Input signals of the *CBSCBR*

Name	Short label	Infotip
IAIBIC	Phase current	Phase current
Pos	Position	Internal singal from CBXCBR
Trip	Trip	Internal singal from CBXCBR
Opn	Open	Internal singal from CBXCBR
Cls	Close	Internal singal from CBXCBR

Table 374 - Output signals of the *CBSCBR*

Name	Short label	Infotip
OpCntWrn	Operations warning	Operations warning
OpCntAlm	Operations alarm	Operations alarm
TrCntWrn	Trip count warning	Trip count warning
TrCntAlm	Trip count alarm	Trip count alarm
ColOpn	Open success	Pulses if the position is Open after an open command.
OpTmOpnWrn	Open time warning	Open time warning

Table 374 - Output signals of the *CBSCBR* (Continued)

Name	Short label	Infotip
OpTmOpnAlm	Open time alarm	Open time alarm
OpTmClsWrn	Close time warning	Close time warning
OpTmClsAlm	Close time alarm	Close time alarm
AbrWrn	Abrasion warning	Abrasion warning
AbrAlm	Abrasion alarm	Abrasion alarm
NoOpAlm	Inactivity alarm	Inactivity alarm
OpCntRs	Operation count	Operation count
TrCntRs	Trip count	Trip count
OpTmOpn	Opening time	Opening time
OpTmCls	Closing time	Closing time
CumAbrPhA	Cumulated abrasion A	Cumulated abrasion A
CumAbrPhB	Cumulated abrasion B	Cumulated abrasion B
CumAbrPhC	Cumulated abrasion C	Cumulated abrasion C
NoOpTm	Inactivity time	Inactivity time

Setting parameters

Table 375 - Settings of the *CBSCBR*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		On
SwACff	Abrasion exponent (y)	This is used to measure the abrasion in A^y. y is usually 2 and accumulates at each opening	1...4	0.1	2
AbrWrnLev	Abrasion warning value	The warning value is the summated abrasion in A^y	0...65000 pu²	1 pu²	0 pu²
AbrAlmLev	Abrasion alarm value	The alarm value is the summated abrasion in A^y	0...65000 pu²	1 pu²	0 pu²
OpWrnNum	Operations warning value	This counts both control open and trip operations	0...10000	1	0
OpAlmNum	Operations alarm value	This counts both control open and trip operations	0...10000	1	0
TrWrnNum	Trip count warning value	This only counts trip operations	0...10000	1	0
TrAlmNum	Trip count alarm value	This only counts trip operations	0...10000	1	0
OpOpnWrnTm	Open time warning value	The output will be set if the measured time exceeds this value. The time is from the open signal to the change of position	0...10000 ms	1 ms	0 ms
OpOpnAlmTm	Open time alarm value	The output will be set if the measured time exceeds this value. The time is from the open signal to the change of position	0...10000 ms	1 ms	0 ms
OpClsWrnTm	Close time warning value	The output will be set if the measured time exceeds this value. The time is from the close signal to the change of position	0...10000 ms	1 ms	0 ms

Table 375 - Settings of the *CBSCBR* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
OpClsAlmTm	Close time alarm value	The output will be set if the measured time exceeds this value. The time is from the close signal to the change of position	0...10000 ms	1 ms	0 ms
NoOpAlmTm	Inactivity alarm value	The output will be set when the breaker has not operated for a period exceeding this time. Useful for older breakers whose first operation will slow over time	0...10000 days	1 days	0 days

Characteristics

Table 376 - Characteristics of the *CBSCBR*

Characteristics		Values
Cumulative broken current	Accuracy	± 2%
Operate delay	Accuracy	10 ms

NOTE: The operate delay in above table is based on the function without the delay caused by the physical contact. The relay contact operate time is 4 ms.

Trip circuit supervision

Description

Trip circuit supervision (TCS) monitors the trip circuit to detect open circuit trip coils or broken wiring. The trip circuit is monitored by connecting one of the relay opto inputs in series with the trip coil. Various schemes are available to allow TCS to work in open or closed position as well as with latched trip contacts.

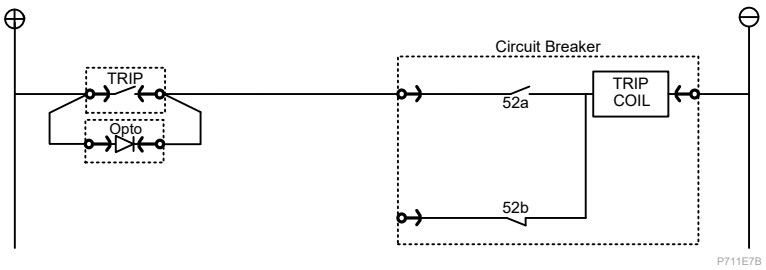
TCS schemes

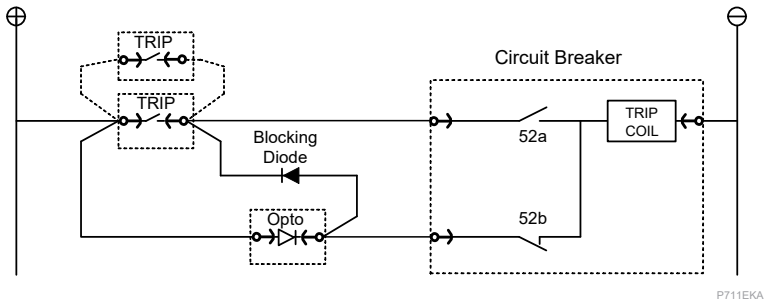
Two schemes are available:

- One-input schemes are straightforward and look for an energized input and sometimes are blocked by the trip signal or breaker position.
- Two-input schemes can simply provide the same logic as a one-input scheme with the two optos ORed avoiding the need to block the element for beaker position or tripping.

Position is provided from the XCBR. The inclusion of breaker position is beneficial if TCS is arranged as follows.

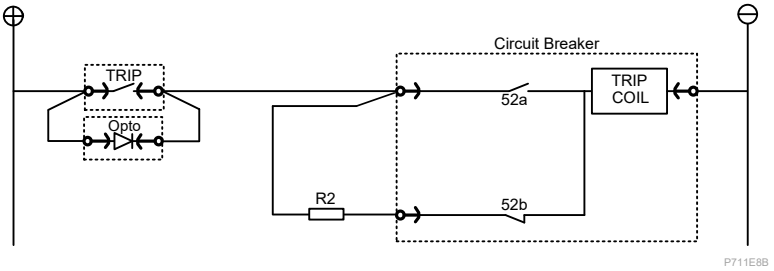
Figure 234 - Basic TCS scheme





In this use case, the TCS will start whenever the trip contact is operated, or the breaker is open. The TCS mode can be set to *Block by state* which will block the TCS if the breaker is open or being opened/tripped. With this setup, the trip circuit is only monitored when the breaker is closed.

Figure 235 - TCS scheme with single opto and open/closed monitoring

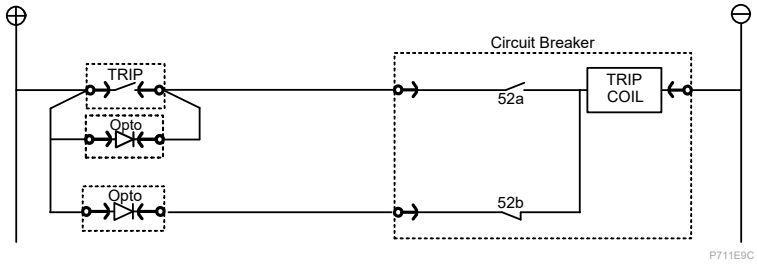


During tripping, this scheme will start but the TCS timer is set to avoid operation. For latched trips, the TCS mode can be set to *Block by trip* to avoid operation when the trip contact is closed.

A second opto will avoid operation during trips. The available TCS schemes are as follows:

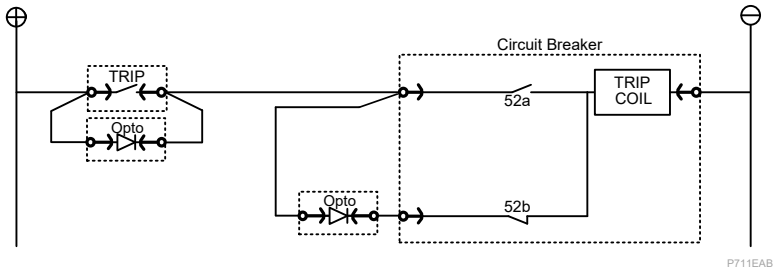
- When the opto is in parallel with the trip contact opto.

Figure 236 - TCS scheme with two optos



- When the opto is in series with the trip contact opto.

Figure 237 - TCS scheme with series optos



The TCS scheme with series optos has the advantage of supervising more of the circuit in the open state. With this connection both optos may not always pick up and the de-energized opto will have a voltage drop of up to 5 V. This does not affect operation but for 24 V schemes the opto pickup ratio should be reduced to allow for the lower voltage that will be seen by the opto that is energized.

Both of these schemes are not affected by the trip contact operation and will not be blocked for CB status or tripping, and the *TCS mode* can be set to *On*. All of the above schemes use a single *Trip healthy* input which can be linked to multiple opto inputs in the matrix.

Close circuit supervision (CCS) has the same operation as TCS except that CCS Modes are the inverse of TCS. *Block by state* will block CCS when closed/closing and *Block by close* will block whenever the close command is present. The TCS can be linked to the CB proxy CB warn input to block closing. TCS and CCS alarms are added as additional inputs to the CB alarm.

TCS wiring

The PowerLogic P7 includes a TCS opto input directly across the first 3 output relays on the power supply auxiliary module (TIO) in slot Y. These contacts can be used for tripping (or closing) which has the advantage of supervising the full trip circuit. It is not mandatory to use these inputs for the TCS function. The output contact and TCS binary input are independently linked to functions in the matrix. If only the TCS binary input is required, then TIO.BO1 should not be assigned in the matrix.

- For breakers with electronic trip circuits.

  These inputs are very low burden and normal optos will often not see enough current for pickup. All binary inputs have a TCS setting to allow operation with these units. It has a constant current of approximately 1 mA and a nominal voltage of 19 V.

  The settings are susceptible to interference in substation environments. This generally has little impact on TCS where a delay can be added if required, however the TCS setting should not be used for any input linked to a protection function.

Resistor values for TCS schemes

Many legacy TCS schemes have a series resistor R1 to limit current to less than 60 mA to avoid tripping if the coil/opto input is shorted. This is extremely unlikely and is usually only applied for consistency with legacy schemes. In these schemes the series resistor needs to be bypassed during tripping, so the dedicated TCS outputs cannot be used. Typical resistor values are shown below.

Figure 238 - TCS scheme with a series resistor R1

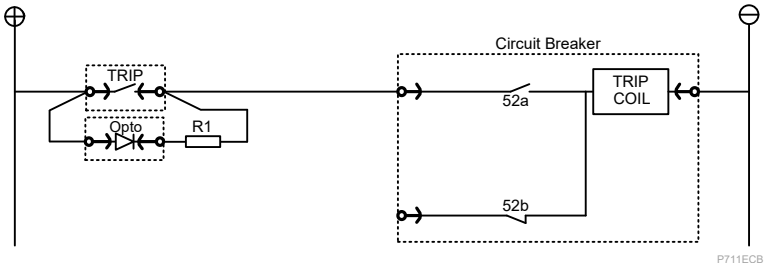


Table 377 - R1 values for TCS scheme

Power Supply (V DC)	Resistance (Ω)	Power (W)
24	600	2
48	1200	4
110	2500	10
220	5000	20

If R2 is used, with or without R1, its value is chosen such that the trip coil will not operate through 52b. This is typically calculated from coil resistance and input voltage requirements.

Table 378 - Typical R2 resistor values

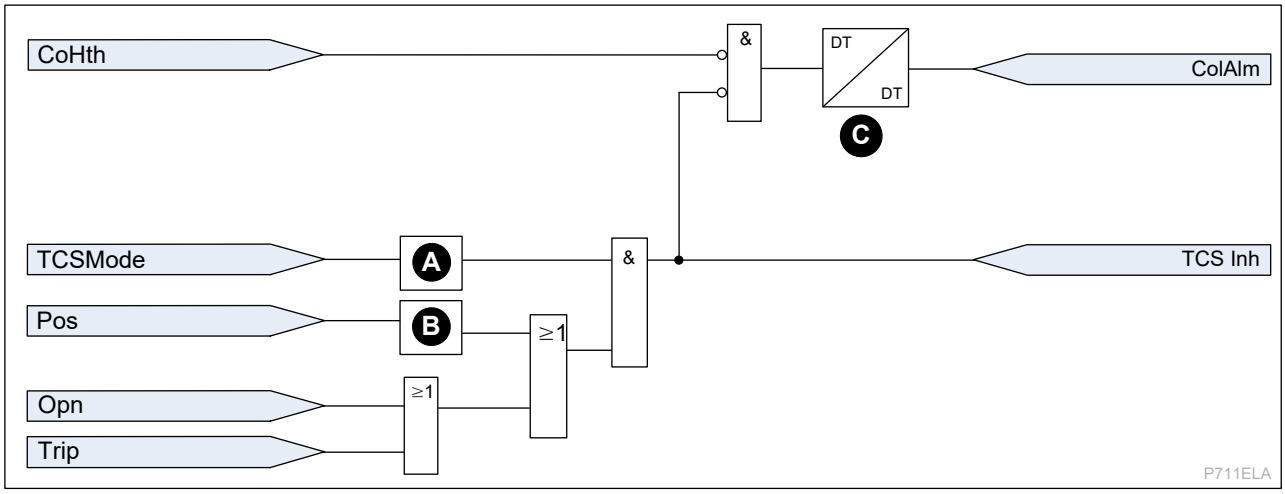
Power Supply (V DC)	Resistance (Ω)	Power (W)
24	1000	2
48	10000	2
110	25000	5
125	25000	5
220	50000	5

The standard opto inputs draw a 30 mA pulse and is not suited to series resistors.

A blocking diode can be applied in preference to R2 to allow a single opto to be used for both open and closed monitoring. As this diode is normally placed between the opto and the trip contact, the TCS outputs cannot be used for both tripping and TCS input.

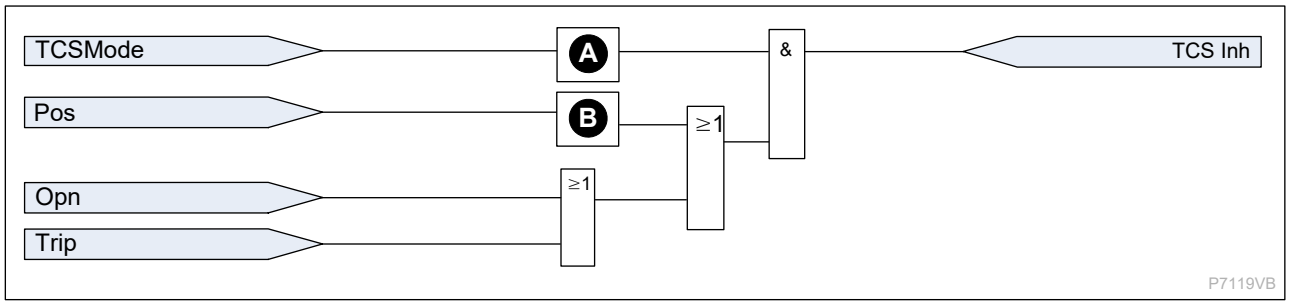
Block diagram

Figure 239 - Block diagram of the TCS



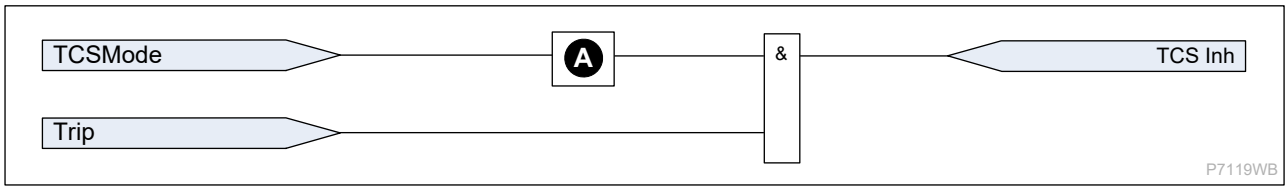
A Blocked by status B Open C *TCSTmms*: 10000 ms

Figure 240 - Block diagram of the TCS mode blocked by status



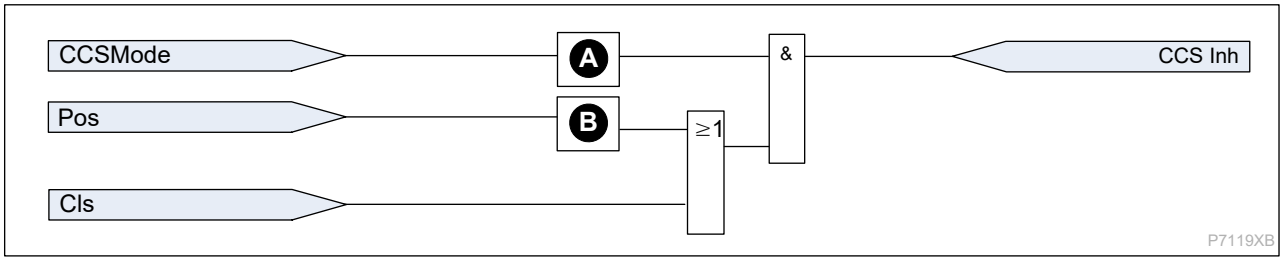
A Blocked by status B Open

Figure 241 - Block diagram of the TCS mode blocked by trip



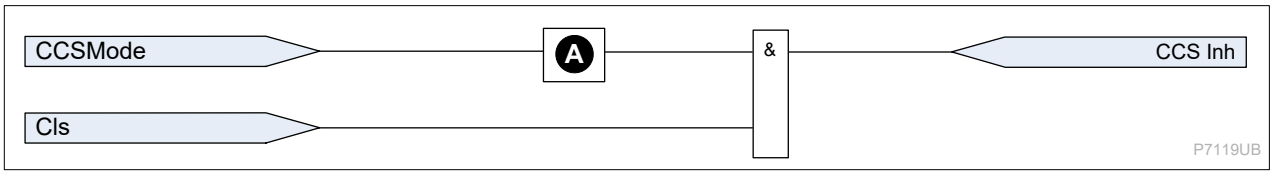
A Blocked by trip

Figure 242 - Block diagram of the CCS mode blocked by status



A Blocked by status B Close

Figure 243 - Block diagram of the CCS mode blocked by close



A Blocked by close

Input and output signals

Table 379 - Input signals of the TCS

Name	Short label	Infotip
Trip	Trip	Internal singal from CBXCBR
Opn	Open	Internal singal from CBXCBR
Cls	Close	Internal singal from CBXCBR
Pos	Position	Internal singal from CBXCBR
CoHth	Trip healthy	Trip circuit healthy for TCS
CColHth	Close healthy	Close circuit healthy for CCS

Table 380 - Output signals of the TCS

Name	Short label	Infotip
ColAlm	TCS alarm	TCS alarm
CColAlm	CCS alarm	CCS alarm
ColCls	Close success	Pulses if the position is Closed after a close command.

Setting parameters

Table 381 - Settings of the TCS

Name	Short label	Infotip	Setting range	Step size	Default setting
TCSMode	TCS mode	Block by state is used when 52b is not in circuit and will block when the breaker is open or being opened/tripped. Block by trip is normally used with latched tripping with a single opto monitoring both CB states.	• Off • On • Block by state • Block by trip		Off
TCSTmms	TCS operate delay	In single opto schemes this is set longer than the CB open/trip pulse. In multiple opto schemes this is set longer than the 52a/52b intermediate state	0...10000000 ms	1 ms	1000 ms
CCSMode	CCS mode	Enables Close Circuit Supervision (CCS). Block by state is used when 52a is not in circuit and will block when the breaker is closed or being closed. Block by close can be used when a single opto monitoring both CB states.	• Off • On • Block by state • Block by close		Off
CCSTmms	CCS operate delay	In single opto schemes this is set longer than the CB close pulse. In multiple opto schemes this is set longer than the 52a/52b intermediate state	0...10000000 ms	1 ms	1000 ms

Characteristics

Table 382 - Characteristics of the TCS

Characteristics		Values
Close success Operate delay	Accuracy	< 5 ms
Close success Reset time	Accuracy	< 5 ms
TCS alarm or CCS alarm Operate delay	DT accuracy	±2% or ±10 ms
TCS alarm or CCS alarm Reset time	Accuracy	10 s ± 100 ms

Switch supervision (*SWSSWI*)

Description

Periodic maintenance of the switch is required to ensure correct operation. Switch supervision is included with each switch package and includes the following information related to the switch operation:

- Number of the switch close to open.
- Switch open time and close time.

Mechanical wear

Switch open counter

The switch open counter is to record the operate number of the switch close to open.

NOTE: The supervision value of the switch open counter can be set to a custom value when the PowerLogic P7 is replaced by a legacy IED that monitors a switch in service.

Switch open time and close time

- Switch open time is the time interval between the open signal is valid and the switch status is open.
- Switch close time is the time interval between the close signal is valid and the switch status is close.

NOTE: Both of the switch open time and the switch close time can be reset.

All statistics are not incremented when the PowerLogic P7 is in test mode. The SW supervision data are managed as follows:

- SW open counter: not incremented
- Operating time (open and close time): recorded

On each of the switch supervision data, two thresholds can be set . One is to produce a warning for maintenance purpose, the other is to produce an alarm for lock out purpose. Each of these warnings and alarms will raise a switch maintenance status information.

Input and output signals

Table 383 - Input signals of the *SWSSWI*

Name	Short label	Infotip
Pos	Switch position	Internal signal from SWXSWI
Opn	Switch open command	Internal signal from SWXSWI
Cls	Switch close command	Internal signal from SWXSWI

Table 384 - Output signals of the *SWSSWI*

Name	Short label	Infotip
OpCntWrn	Operations warning	Operations warning
OpCntAlm	Operations alarm	Operations alarm
OpTmOpnWrn	Open time warning	Open time warning
OpTmOpnAlm	Open time alarm	Open time alarm
OpTmClsWrn	Close time warning	Close time warning
OpTmClsAlm	Close time alarm	Close time alarm

Setting parameters

Table 385 - Settings of the *SWSSWI*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		On
OpWrnNum	Operations warning value	Sets the operation warning output when the opening count exceeds this value	0...10000	1	0
OpAlmNum	Operations alarm value	Sets the operation alarm output when the opening count exceeds this value	0...10000	1	0
OpOpnWrnTm	Open time warning value	Sets the open time warning output when the time from the open command to position change exceeds this value	0...100000 ms	1 ms	0 ms
OpOpnAlmTm	Open time alarm value	Sets the open time alarm output when the time from the open command to position change exceeds this value	0...100000 ms	1 ms	0 ms

Table 385 - Settings of the *SWSSWI* (Continued)

Name	Short label	Infotip	Setting range	Step size	Default setting
OpClsWrnTm	Close time warning value	Sets the close time warning output when the time from the close command to position change exceeds this value	0...100000 ms	1 ms	0 ms
OpClsAlmTm	Close time alarm value	Sets the close time alarm output when the time from the close command to position change exceeds this value	0...100000 ms	1 ms	0 ms

Characteristics

Table 386 - Characteristics of the *SWSSWI*

Characteristics		Values
Operate delay	Accuracy	10 ms

NOTE: The operate delay in above table is based on the function without the delay caused by the physical contact. The relay contact operate time is 4 ms.

DC battery voltage monitoring (*ZBAT*)

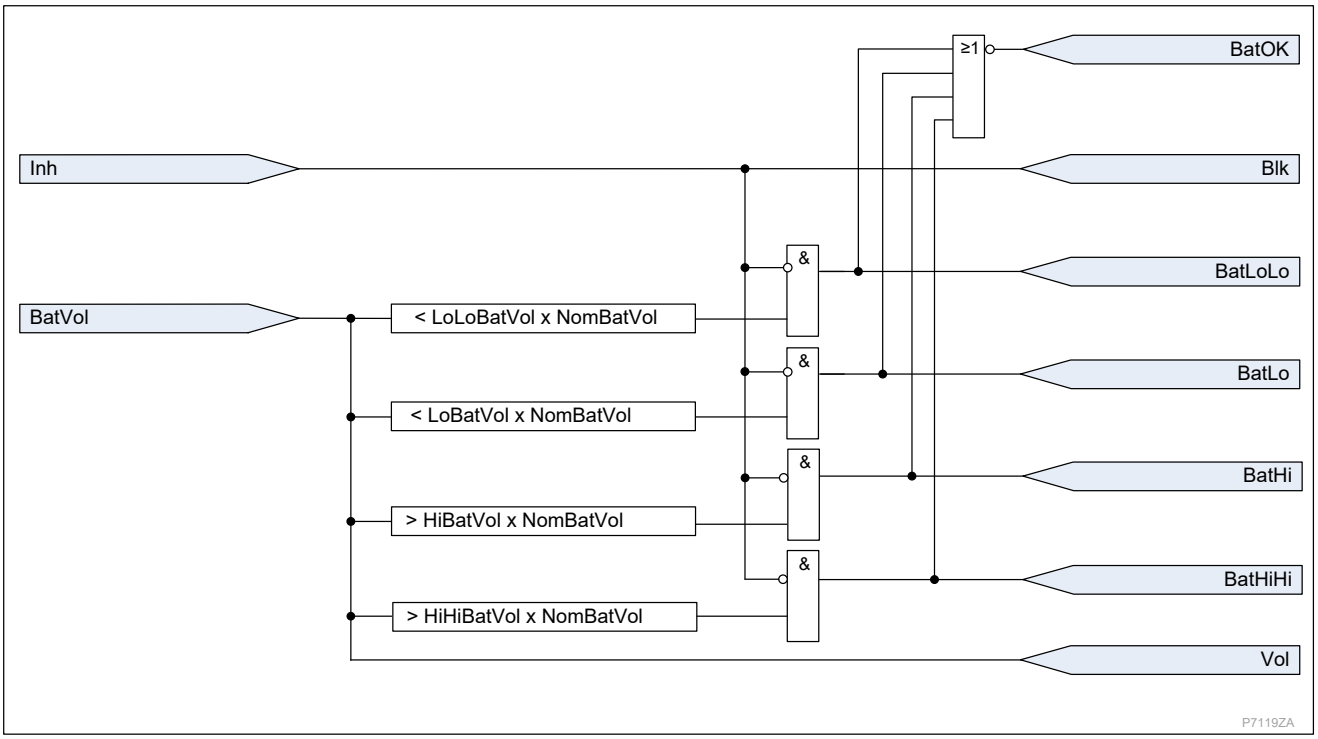
Description

The DC battery voltage monitoring function is used to monitor the DC voltage of the PowerLogic P7 and helps to detect issues such as battery charger failures.

The DC battery voltage monitoring function provides four alarm signals when the auxiliary DC voltage input exceeds or falls below the corresponding set thresholds.

Block diagram

Figure 244 - Block diagram of the *ZBAT*



Input and output signals

Table 387 - Input signals of the *ZBAT*

Name	Short label	Infotip
BatVol	Voltage	Voltage measurement from PSU
Inh[general]	Inhibit	Inhibit function

Table 388 - Output signals of the *ZBAT*

Name	Short label	Infotip
Vol	Auxiliary voltage	Auxiliary voltage
BatOK	Voltage OK	Voltage OK
BatLo	Low alarm	Low alarm
BatLoLo	Low low alarm	Low low alarm
BatHi	High alarm	High alarm
BatHiHi	High high alarm	High high alarm
Blk	Blocked	Blocked

Setting parameters

Table 389 - Settings of the *ZBAT*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
NomBatVol	Nominal DC	Nominal battery voltage. Float voltage can also be used and alarm values varied to suit	24...250 V	1 V	110 V
LoBatVol	Low alarm value	Low alarm value	0.8...1 pu	0.01 pu	0.8 pu
LoLoBatVol	Low low alarm value	Low low alarm value	0.8...1 pu	0.01 pu	0.8 pu
HiBatVol	High alarm value	High alarm value	1...1.35 pu	0.01 pu	1.2 pu
HiHiBatVol	High high alarm value	High high alarm value	1...1.35 pu	0.01 pu	1.2 pu

NOTE: *ZBAT* is only for battery voltage monitoring and not applicable for monitoring the AC supply. The recommended set thresholds should depend on the float voltage of the battery. The function may not work when the relay auxiliary is below 80% of the minimum voltage of the range and exceeds 120% of the maximum auxiliary voltage of the range for each level.

- Low level: 24...34 V
- Middle level: 48...125 V
- High level: 110...250 V

Characteristics

Table 390 - Characteristics of the *ZBAT*

Characteristics		Values
Voltage	Accuracy	±5% or ±0.05 V
Overvoltage	Reset ratio	98% ± 5%
Undervoltage	Reset ratio	102% ± 5%

Bay dead (*PDGAPC*)

Description

The bay dead function is applied to give an indication if all phases of the line are dead. A bay dead condition is determined by monitoring the status of the CBclosed input and by measuring the phase currents and voltages.

The output signal *BayDead* is asserted when one of the following conditions applies.

- Current quality is invalid.

  CBclosed is inactive.
- Current quality is valid.

  CBclosed is inactive.

  None of the three phase currents exceeds the current threshold.

- Current and voltage quality are valid.

  None of the three phase currents exceeds the current threshold.

  None of the three phase-to-phase voltages exceeds the voltage threshold.

  The duration time is more than 20 ms.
- Current and voltage quality are invalid.

  CBclosed is inactive.

  NOTE:
  - It is recommended to configure the CBclosed input to all CB positions in the bay via matrix. When all CB positions are in open position, CBclosed is set to inactive.
  - When the CBclosed input is not configured via matrix, the default value of CBclosed is inactive.

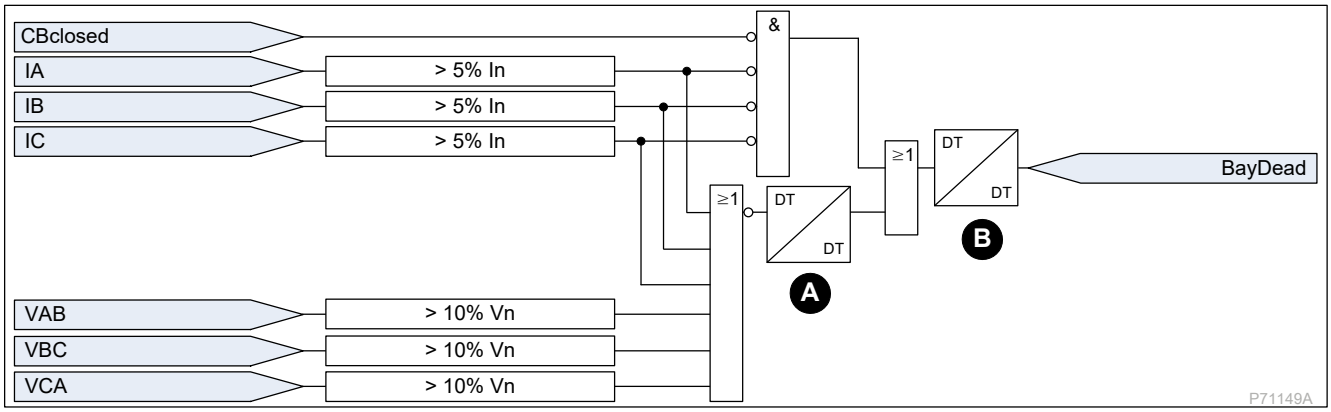
Bay dead matrix

With the PowerLogic Engineering Suite, locate to the **Bay 1 configuration > Bay dead** to set up the bay dead matrix.

Configure the **CB closed** input to all CB positions in the bay through the bay dead matrix. When there is no CBs in the bay, an opto or other signal representing the bay alive information can be used as the **CB closed** input in the matrix. If no **CB closed** signal is available then the bay dead indication is based on the bay current and voltage measurements.

Block diagram

Figure 245 - Block diagram of the *PDGAPC*



A	Operate delay: 20 ms Reset delay: 0 ms	B	Operate delay: 0 ms Reset delay: 20 ms

Input and output signals

Table 391 - Input signals of the *PDGAPC*

Name	Short label	Infotip
UABUBCUCA	Line voltage	Line voltage
IAIBIC	Phase current	Phase current

Table 392 - Output signals of the *PDGAPC*

Name	Short label	Infotip
BayDead	Bay dead	Bay dead

Characteristics

Table 393 - Characteristics of the *PDGAPC*

Characteristics		Values
Phase current (fixed)	Accuracy	±0.005 In
	Reset ratio	95% ± 2%
Line voltage (fixed)	Accuracy	±0.002 Vn
	Reset ratio	98% ± 2%
Operate delay (fixed)	Accuracy	±20 ms
Characteristic time	Start time	< 40 ms

Temperature (*RTDTTMP*)

Description

This function gives the temperature value measured by resistance temperature detectors (RTDs):

- Platinum Pt100 (100 Ω at 0°C or 32°F) in accordance with the IEC 60751 and DIN 43760 standards.

The PowerLogic P7 supports one MET148-2 module with up to eight RTD channels. This module communicates with the PowerLogic P7 through the Controller Area Network (CAN) link. Ambient is fixed to RTD number 8 on the first MET module.

The function also indicates RTD faults:

- RTD disconnected (t > 201°C or t > 393.8°F)
- RTD shorted (t < -31°C or t < -23.8°F).

Each output signal of the temperature measurement for RTD fault indicates one of four meanings:

1. RTD measurement is in normal range.
2. Short Circuit (t < -31°C or t < -23.8°F).
3. Open Circuit (t > 201°C or t > 393.8°F).
4. RTD board is disconnected.

In the event of a fault, the display of the value is set to -32768 for open circuit and 32767 for short circuit with invalid quality. The associated monitoring function generates a failure status.

The measurements and RTD health may be accessed via:

- On the HMI, under **General > Device config > Slot A > RTDs**

  NOTE: If the *STMP* function is enabled, then the measurements are also shown on the HMI under **Measurements > Bay x > Temperature**. The RTD name and function can be set with *STMP*.

- The communication link

Output signals

Table 394 - Output signals of the *RTDTTMP*

Name	Short label	Infotip
MTmp1	RTD1 temperature	RTD1 temperature
MTmp2	RTD2 temperature	RTD2 temperature
MTmp3	RTD3 temperature	RTD3 temperature
MTmp4	RTD4 temperature	RTD4 temperature
MTmp5	RTD5 temperature	RTD5 temperature
MTmp6	RTD6 temperature	RTD6 temperature
MTmp7	RTD7 temperature	RTD7 temperature
MTmp8	RTD8 temperature	RTD8 temperature
RTDFail1	RTD1 health	RTD1 health
RTDFail2	RTD2 health	RTD2 health
RTDFail3	RTD3 health	RTD3 health
RTDFail4	RTD4 health	RTD4 health
RTDFail5	RTD5 health	RTD5 health
RTDFail6	RTD6 health	RTD6 health
RTDFail7	RTD7 health	RTD7 health
RTDFail8	RTD8 health	RTD8 health

Setting parameters

Table 395 - Settings of the *RTDTTMP*

Name	Short label	Infotip	Setting range	Step size	Default setting
RTDTyp	RTD type	RTD type	• Pt100		Pt100

Characteristics

Table 396 - Characteristics of temperature measurement

Characteristics	Values
Range	-30°C...+200°C (-22°F...+392°F)
Resolution	1°C/min (1.8°F/m)
Accuracy	±1°C for +20°C...+140°C (±1.8°F for +68°F...+284°F); ±2°C for -30°C...+20°C (±3.6°F for -22°F...+68°F); ±2°C for +140°C...+200°C (±3.6°F for +284°F...+392°F)
Refresh interval	5 seconds (typical)

Voltage variation (*QVVR*)

Description

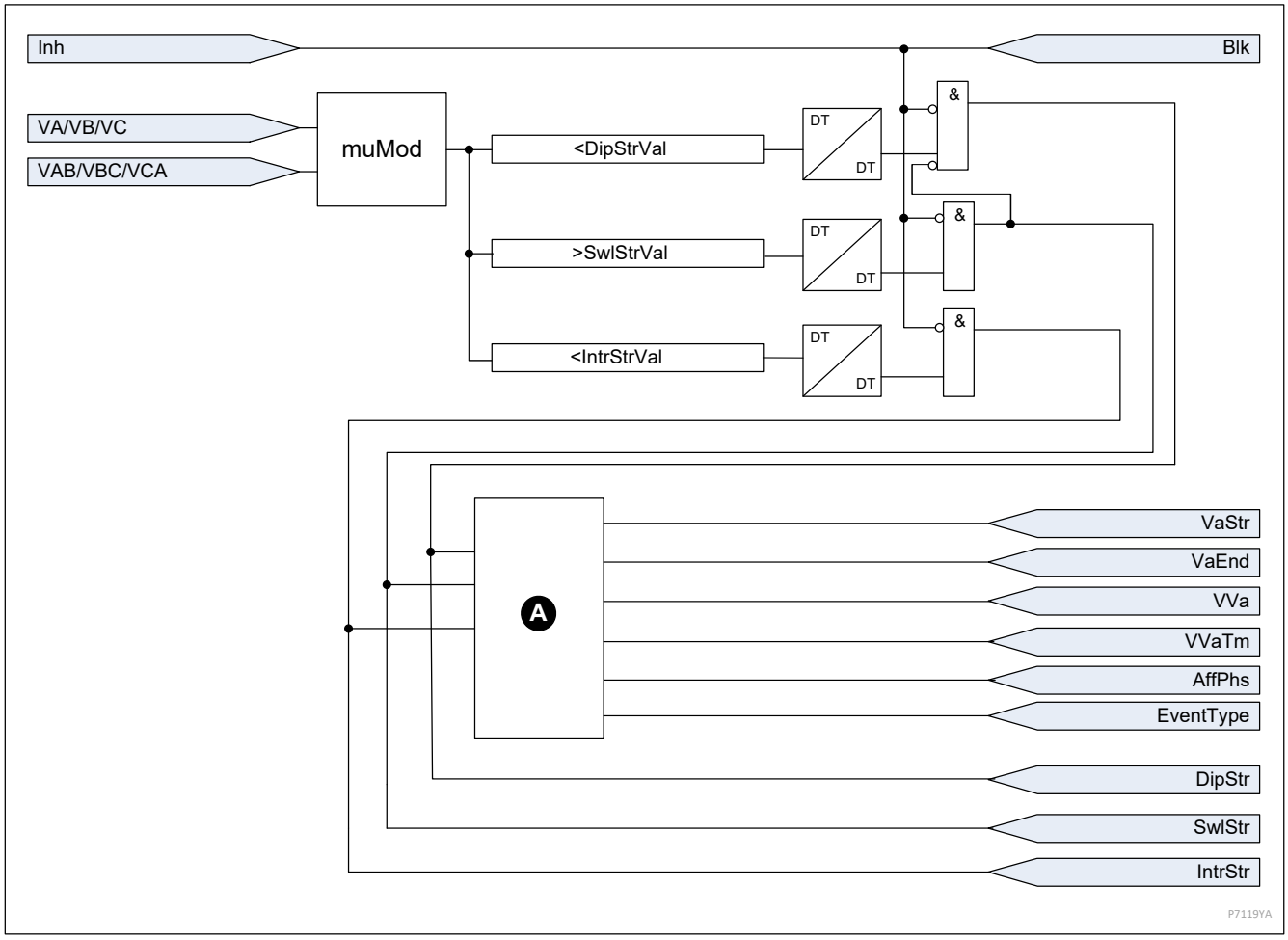
The voltage variation function is applied to monitor and analyze voltage quality. Voltage can have disturbances such as periods of voltage swell, voltage dip, or voltage interruption, which can cause equipment damage. This function has three parts, each of which corresponds to one of the aforementioned voltage disturbances.

This function measures the three-phase RMS voltage including harmonics up to 20th order and supports measurement modes of phase-to-phase and phase-to-ground. If, for a configured duration, the measured voltage exceeds the swell start value, drops below the dip start value, or has an interruption, the corresponding voltage swell, dip, or interruption is logged as an event. Each of those event logs includes phase, start time, duration, maximum or minimum voltage.

NOTE: Three counters are available to separately record the number of voltage swell, voltage dip, and voltage interruption events. All the event logs and counters are accessible from the HMI, the PowerLogic Engineering Suite, and the communication ports.

Block diagram

Figure 246 - Block diagram of the *QVVR*



A Power quality record

Input and output signals

Table 397 - Input signals of the *QVVR*

Name	Short label	Infotip
Inh[general;phsA;phsB;phsC]	Inhibit	Inhibit function
VAVBVCRMS	VAVBVCRMS	Internal signal from TVTT1
UABUBCUCARMS	VABVBCVCARMS	Internal signal from TVTT1
RstCnt	Reset Counters	Reset Counters

Table 398 - Output signals of the *QVVR*

Name	Short label	Infotip
DipStr	Dip	Dip
SwlStr	Swell	Swell
IntrStr	Interruption	Interruption
DipCnt	Dip counter	Dip counter
SwlCnt	Swell counter	Swell counter
IntrCnt	Interruption counter	Interruption counter
VVa	Max variation voltage	Max variation voltage
Deviation	Deviation	Deviation
VVaTm	Event duration	Event duration
AffPhs	Affected phase	Affected phase
EventType	Event type	Event type
VaStr	Variation start	Variation start
VaEnd	Variation end	Variation end
RstCntCtrl	Reset counters	Reset counters
Blk	Blocked	Blocked

Setting parameters

Table 399 - Settings of the *QVVR*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
DipStrVal	Dip start value	Dip start value	0.1...1.2 pu	0.01 pu	0.9 pu
SwlStrVal	Swell start value	Swell start value	0.1...1.5 pu	0.01 pu	1.1 pu
IntrStrVal	Interruption start value	Interruption start value	0.01...1.2 pu	0.01 pu	0.05 pu
DipDlTmms	Dip operating delay	Dip operating time delay	10...1000 ms	10 ms	10 ms
SwlDlTmms	Swell operating delay	Swell operating time delay	10...1000 ms	10 ms	10 ms
IntrDlTmms	Interruption operating delay	Interruption operating time delay	0...1000 ms	10 ms	10 ms
MuMod	Measurement mode	Measurement mode	• Phase-phase • Phase-neutral		Phase-neutral

Characteristics

Table 400 - Characteristics of the *QVVR*

Characteristics		Values
Dip	Accuracy	±2% or ±0.01 pu
	Reset ratio	102% ± 2%
	Start time	< 30 ms
	Reset time	< 25 ms
Swell	Accuracy	±2% or ±0.01 pu
	Reset ratio	98% ± 2%
	Start time	< 30 ms
	Reset time	< 25 ms
Interruption	Accuracy	±2% or ±0.01 pu
	Reset ratio	102% ± 2%
	Start time	< 30 ms
	Reset time	< 25 ms

Current loop (mA) input (*CLTGSN*)

Description

The current loop (mA) input function is used together with the Current Loop Input/Output (CLIO) module to accommodate a variety of transducer types and measurement ranges.

Four analog or current loop inputs are provided for transducers. These inputs interface with different types of transducers that monitor and control systems. Various transducers can be rotor earth resistance measurement, tap position indicators, vibration monitors, tachometers and pressure transducers.

The supported ranges on the device are:

- 0-1 mA
- 0-10 mA
- 0-20 mA
- 4-20 mA

Function overview

- Linear current conversion: The *CLTGSN* performs a linear conversion on the small current signals received from the CLIO module, presenting the channel input values along with the converted channel values. The converted values can be used in programmable stage.
- Connection and communication status: The function verifies the connection between the device interface and the CLIO module, reporting the channel communication and output health.
- Input range specification: Provides the specific range selection for CLIO module inputs as well as the corresponding range of linear converted values.
- Control of CLIO board input channels: Provides the management of four input channels available on a CLIO module, each channel is associated with a dedicated *CLTGSN*.

- Definition of value units and descriptions: A label can be provided for the values obtained after the linear conversion process. The label should include any units and/or multipliers. For example, *Resistance* (kohm) or *Pressure* (hPa).

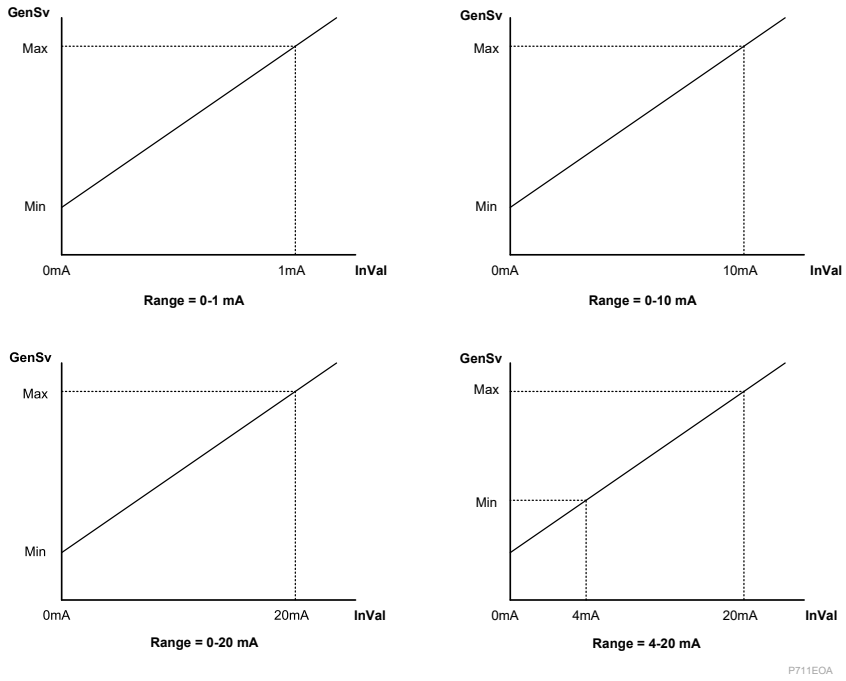
On the HMI, the status and settings of each current loop input can be viewed at:

General > Device config > Slot A > CL inputs #

Channel value conversion

The linear relationship between *Channel input* (*InVal*) and *Channel output* (*GenSv*) is shown as follows:

Figure 247 - Relationship between channel input and channel output



The linear relationship can be calculated using the formula:

$$GenSv = \frac{Max - Min}{RtgCLI_{Max} - RtgCLI_{Min}} \times InVal + \left(Min - \frac{Max - Min}{RtgCLI_{Max} - RtgCLI_{Min}} \times RtgCLI_{Min} \right)$$ E71208A

Where,

- $RtgCLI_{Max}$: The upper limit of *RtgCLI*.
  - *1 mA* in the range *0-1 mA*
  - *10 mA* in the range *0-10 mA*
  - *20 mA* in the range *0-20 mA*
  - *20 mA* in the range *4-20 mA*
- $RtgCLI_{Min}$: The lower limit of *RtgCLI*.
  - *0 mA* in the range *0-1 mA*
  - *0 mA* in the range *0-10 mA*
  - *0 mA* in the range *0-20 mA*
  - *4 mA* in the range *4-20 mA*

  NOTE: If the *Max* set is less than the *Min*, the slope will be negative. This is because the mathematical relationship remains the same irrespective of how they are set. For example, for *4-20 mA* range,*Max* always corresponds to 20 mA and*Min* corresponds to 4 mA.

The range of *Min* and *Max* values is constrained between *-9999* and *+9999* in *0.001* steps to allow the converted value to be displayed on the mimic.

NOTE: To display larger or smaller values, scale the input and display the factor in the label. For example, an hours run indication can be scaled in *days*, *weeks*, *months*, years or *×100 hours*.

Channel input for different ranges

The quality of the input signal will depend on the input range.

- Within 20% of the expected range, the input and the converted output will be marked as *questionable*.
- Above 20% range, it will be marked as *invalid*.

  NOTE: Where the range starts at zero, the measurement is *questionable* above -0.1 mA and *invalid* below this value.
- Between *Min* and *Max* values, the input and output values have *good* quality.

NOTE: If communications to the CLIO module is lost, the measurements will report zero with *invalid* quality.

RtgCLI	Questionable range	Invalid range
0-1 mA	-0.1...0 mA 1...1.2 mA	< -0.1 mA > 1.2 mA
0-10 mA	-0.1...0 mA 10...12 mA	< -0.1 mA > 12 mA
0-20 mA	-0.1...0 mA 20...24 mA	< -0.1 mA > 24 mA
4-20 mA	3.2...4 mA 20...24 mA	< 3.2 mA > 24 mA

Channel supervision

In addition to changing the measurement quality, two health signals are also available.

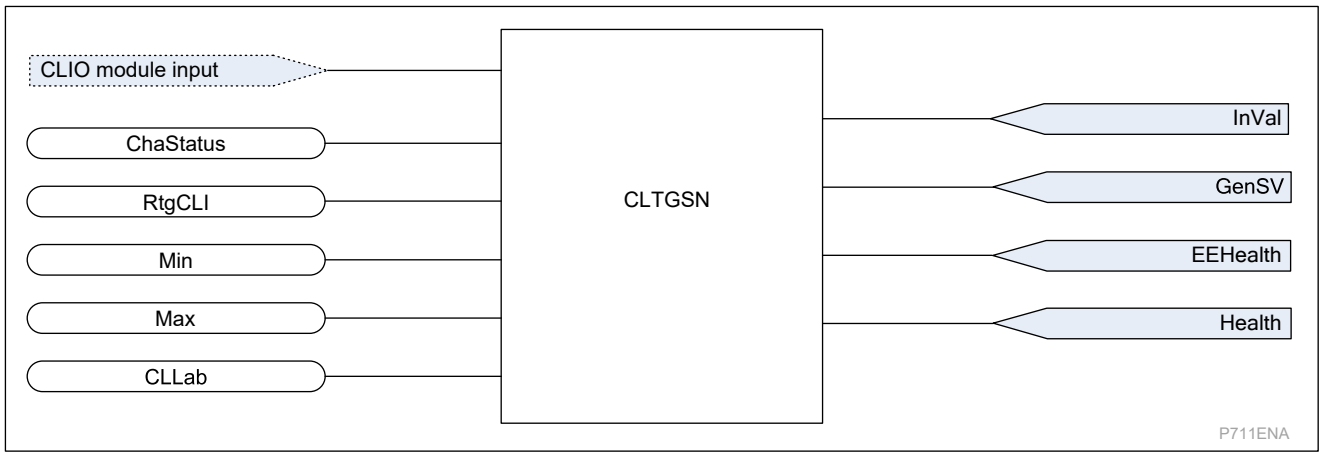
- *Health* indicates whether communication is available to the module providing the input channel measurement. If *comms* are healthy, the health is *OK*, otherwise it is *Alarm*.
- *EEHealth* indicates the health of mA signal being measured. It follows the measurement quality issuing a warning if the measurement is *questionable* and an alarm if the measurement is *invalid*.

Channel	Channel health		*InVal*		*GenSv*		*EEHealth*		*Health*	
			Value	Quality	Value	Quality	Value	Quality	Value	Quality
On	No connection		0	Invalid	0	Invalid	Alarm	Good	Alarm	Good
	Connected	RtgCLI	InVal	Good	converted value	Good	OK	Good	OK	Good
		Within 20% range	InVal	Questionable[16]	converted value	Questionable[16]	Warning	Good	OK	Good
		Above 20% range	InVal	Invalid[16]	converted value	Invalid[16]	Alarm	Good	OK	Good
Off	Connected		0	Invalid	0	Invalid	OK	Invalid	OK	Invalid

16. Out of range

Block diagram

Figure 248 - Block diagram of the *CLTGSN*



Input and output signals

Table 401 - Output signals of the *CLTGSN*

Name	Short label	Infotip
InVal	Measured value	The mA measured on the CLIO module for this channel
GenSv	Calculated value	Calculated value from linear conversion
EEHealth	mA signal health	Health of the measured value. It will indicate questionable if the value is out of range and invalid if significantly out of range or comms are lost
Health	CLIO health	This indicates an Alarm state if communications is lost to the CLIO module

Setting parameters

Table 402 - Settings of the *CLTGSN*

Name	Short label	Infotip	Setting range	Step size	Default setting
ChaStatus	Status	Status	• Off • On		Off
RtgCLI	Range	Range of the mA sensor	• 0-1 mA • 4-20 mA • 0-20 mA • 0-10 mA		4-20 mA
Min	Output minimum	Output value at range minimum	-9999...9999	0.001	0
Max	Output maximim	Output value at range maximim	-9999...9999	0.001	100
CLILab	Label	Label			CLILab

Characteristics

Table 403 - Characteristics of the *CLTGSN*

Characteristics		Values
Channel input	Accuracy	±0.1 mA
Channel output	Accuracy	±5%

Programmable stage (*PSGAPC*)

Description

The programmable stage function is used to map the measured input values from CLI channels to dedicated protection or monitoring stages.

The function allows the stage to perform the defined mathematical calculation on the measured input value from *InVal1* and a reference value. The reference value is from the setting *Fixed value* (*FixVal*).

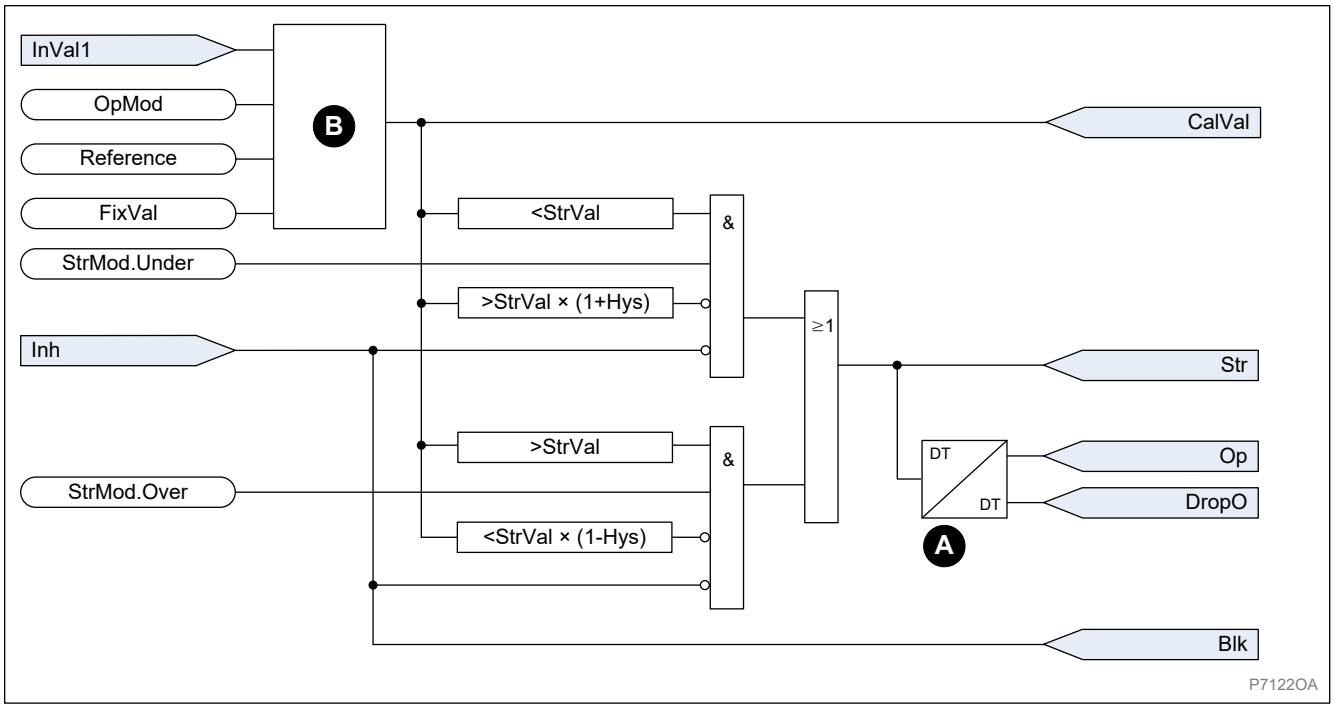
The stage compares the *Calculated value* against the *Start value*. The *Start* signal is issued when the *Calculated value* meets the *Start value*. The *Operate* signal is issued when the *Start* signal is active and the *Operation delay* has elapsed.

The mathematical calculation is defined by the setting *Operation mode* (*OpMod*). The mathematical calculations available for the measured input value are as follows:

- Input 1
- Input 1 + Reference
- Input 1 - Reference
- Reference - Input 1
- |Input 1 - Reference|
- Input 1 × Reference
- Input 1 / Reference
- Reference / Input 1

Block diagram

Figure 249 - Block diagram of the *PSGAPC*



A	Operate delay: *OpDITmms* Reset delay: *RsDITmms*	B	Mathematical calculation

Input and output signals

Table 404 - Input signals of the *PSGAPC*

Name	Short label	Infotip
InVal1	Input 1	Input 1
Inh[general]	Inhibit	Inhibit

Table 405 - Output signals of the *PSGAPC*

Name	Short label	Infotip
Str	Start	Start
Op	Operate	Operate
DropO	Drop out	Drop out
Blk	Blocked	Blocked
CalVal	Calculated value	Calculated value

Setting parameters

Table 406 - Settings of the *PSGAPC*

Name	Short label	Infotip	Setting range	Step size	Default setting
SetMod	Function status	Function status	• On • Off		Off
Reference	Reference value	This detemines whether the reference is input 2 or the fixed value.[17]	• Fixed		Fixed
FixVal	Fixed value	When the reference is set to fixed this value is used	0.001...1e+07 pu	0.001 pu	1 pu
StrMod	Start mode	Start mode	• None • Over • Under		None
StrVal	Start value	Start value	0.001...10000 pu	0.001 pu	10 pu
OpDlTmms	Operation delay	Operation time delay	0...10000000 ms	1 ms	0 ms
RsDlTmms	Reset delay	Reset time delay	0...10000000 ms	1 ms	0 ms
Hys	Hysteresis	When the start mode is over the element will drop out at this % under the threshold. If the start mode is under it will drop out at this % over the threshold	0...10 %	0.1 %	5 %

Characteristics

Table 407 - Characteristics of the *PSGAPC*

Characteristics		Values
Start time	Accuracy	< 25 ms[18]

17. Input 2 cannot be selected in the current firmware version, will be available in the upcoming version.
18. The stage performance is independent of the sensor performance. The performance here is a start delay of less than 25 ms after the calculated value meets the threshold.

Maintenance

PowerLogic P7 devices together with communication accessories and cabling, require maintenance in work according to their specification. Keep a record of the maintenance actions. The maintenance can include, but is not limited to, the following actions.

Safety instructions

This page contains important safety instructions that must be followed precisely before attempting to install, repair, service or maintain electrical equipment. Carefully read and follow the safety instructions described below.

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

- NEVER work alone.
- Turn off all power supplying this equipment before working on or inside it.
- Verify that all power is off using a properly rated voltage sensing device.

Failure to follow these instructions will result in death or serious injury.

NOTE: Consider all sources of power when turning off the power supply, including the possibility of backfeeding.

⚠DANGER

FIRE HAZARD

- Apply proper tightening torque to all wire connections.
- Disconnect the power supply before removing or replacing a module.
- Never touch electronics parts.
- In case of module replacement, perform the commissioning operations before using the protection and control device.

Failure to follow these instructions will result in death or serious injury.

⚠WARNING

UNINTENDED DEVICE OPERATION

Replace the terminal blocks in the correct locations after removing them for wiring or testing.

Failure to follow these instructions can result in death, serious injury, or equipment damage.

⚠CAUTION

RISK OF SETTING CHANGES ERASED

Never plug in or draw out the communication modules while the PowerLogic P7 is in service.

Failure to follow these instructions can result in injury or equipment damage.

Self-monitoring

Watchdog relay

The PowerLogic P7 is equipped as standard with a watchdog relay (in Slot Z). This is a changeover relay which is kept permanently in the on-position by the device.

In the event of the protection and control device failure, or if the auxiliary power supply fails, the watchdog relay reverts to the off position.

Maintenance LED

The maintenance LED (see Using the HMI, page 125) is on when any of the following cases happen:

- The embedded self-tests detected one hardware or firmware failure. In this case the device is no longer fully operational.
- The device is in *Test* or *Test-blocked* mode. In this case the LED will be flashing.
- The device is in Safe mode. In this case the device is no longer operational.
- The device is being energized during the start phase. This case is normal and does not indicate any internal failure. When the start phase of the device is completed, the LED is off if no internal failure is detected.

When the maintenance LED is on, a icon will appear on the top right corner of the HMI (when fitted). Tap this icon to view the current device maintenance information.

NOTE: The maintenance status is also indicated on the rear LEDs. See Physical LEDs on the CPU board, page 127 for details.

Self-tests

The PowerLogic P7 runs a series of self-diagnostic tests for hardware and software in boot sequence and also performs runtime check. These self-tests detect any failure and can avoid random PowerLogic P7 behavior. The main purpose is to avoid an unwanted tripping or failure to trip in the event that it occurs on the power system or on the equipment to protect.

The PowerLogic P7 can detect two types of internal failure:

- A major failure when the protection functions cannot be processed properly or can initiate an unwanted trip. In this case, the PowerLogic P7 will go into the fallback position:
  - The output relays are in the off position.
  - Watchdog relay (on slot Z) goes into the off position.
  - LED, LED, and the virtual configurable LEDs are off.
  - ON LED of the front panel is on.
  - LED of the front panel is on.

    NOTE: Tap on HMI to go to the maintenance panel which shows the HW/FW healthy status.
  - The communication is inoperative.
  - The communication with the PowerLogic Engineering Suite is inactive depending on the type of internal failure.

- A minor defect is a malfunction of components (hardware or firmware) that are not directly used by protection functions (i.e. memory, used for logging emergency events, communication channels, etc.). It shall not result in loss of the PowerLogic P7 operability.
  - The output relays stay in their current status.
  - Watchdog relay (on slot Z) stays energized.
  - ⓘ LED, ⚡ LED, and the virtual configurable LEDs stay in their current position.
  - ON LED of the front panel is on.
  - 🔧 LED of the front panel is off.
  - An alarm message is displayed on the front panel to highlight the origin of the issue.

    NOTE: Press the R button to remove the message. The alarm message is logged in the Alarm message list.
  - The communication is still operational depending on the type of the internal failure.
  - The communication with the PowerLogic Engineering Suite, on the front panel is active depending on the type of internal failure.

List of self-tests

The self-tests are described in the table below.

Table 408 - List of self-tests

Name	Execution Period
Hardware configuration versus the product model number	On energization and during operation
Power supply	
RTD presence (MET148-2)	
Micro processor	
Firmware (system and application) and setting consistency	
Binary inputs	
Binary outputs	

IED mode

The PowerLogic P7 has following main modes:

- **Startup**: This state is transient between **PowerOn** and **Normal** or **Safe** or **Default** mode. The Device can also enter **FactoryReset** mode after startup.
- **Normal**: This state is stable. The device normally works in this mode. In this mode, the IED has several sub states:
  - **Test**: The state is stable. When LD0/LLN0.Mod is changed to *Test*, the IED will work in this state and the binary output relays can still operate in this mode.
  - **TestBlocked**: The state is stable. When LD0/LLN0.Mod is changed to *TestBlocked*, the IED will work in this state except for output relays which will not operate.
  - **Degrade**: The state is transient. When some nonfatal errors occur, the IED continues running as long as the protection domain works normally. The fault situation can be observed by HMI maintenance LED, SOE, system event log or LPHD1/PhyHealth in database.
  - **Safeguard**: The state is transient between **Normal** and **Safe** mode.

- **Safe**: When supervision initialization fails, or fatal errors occur from the protection, the IED enters this state. In this state, the PowerLogic P7 is no longer operational and all the device's output relays are forced into the off position, thus the power system is no longer protected. If the auxiliary power supply disappears, the PowerLogic P7's contact relays are also in the off position.

  Meantime, the HMI still provides the maintenance work, for example, view the software version and error cause. Besides, Web Service is available for updating configuration files and switching back to **Normal** mode by Engineering Suite.
- **FactoryReset** (**Default**): This state is stable. When IED state is **Normal**, the IED can enter this mode after reboot by factory reset operation from HMI. Once any setting is changed or configuration file is downloaded, the IED will enter **Normal** mode.

The device states information including protection, binary outputs, front panel and communication status are shown as follows:

Table 409 - Status information

IED state	Protection	Watchdog relay	Output relays	Front panel HMI	Communication status	Data reference
Startup	OFF	Not energized	De-activated	Splash screen	Not available	Not available
Safe	OFF	Not energized	De-activated	Safe mode screen	Web Service	LD0/LPHD1. ledMode
Factory reset	OFF	Energized	Application dependent	Welcome screen	Web Service	LD0/LPHD1. ledMode
Normal	Application dependent	Energized	Application dependent	Application dependent	61850 and/or legacy protocols	LD0/LPHD1. ledMode
Degrade	Application dependent	Not energized	Application dependent	Application dependent	61850 and/or legacy protocols	LD0/LPHD1. PhyHealth
Test/ TestBlocked	Application dependent	Energized	Unblocked relay/ Blocked relay	Application dependent	61850 and/or legacy protocols	LD0/LLN0.Beh

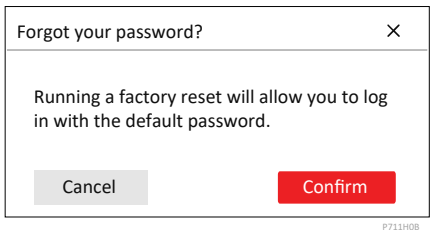
Performing factory reset

Factory reset function is to make the IED recover the factory default configuration and settings with the proper access right. This function can be executed from the front panel HMI only when the IED is in **Normal** mode. After the factory reset, the IED will enter **Default** mode. For the IED mode introduction, please refer to IED mode, page 460. For authorization information, please refer to User accounts and rights, page 111.

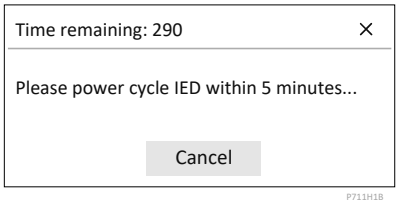
To perform factory reset operation, three entrances are available:

- **When in Auto-login or logout status**

1. From **Login** page, tap **Forgot your password?**.
2. From the pop-up window, tap **Confirm**.



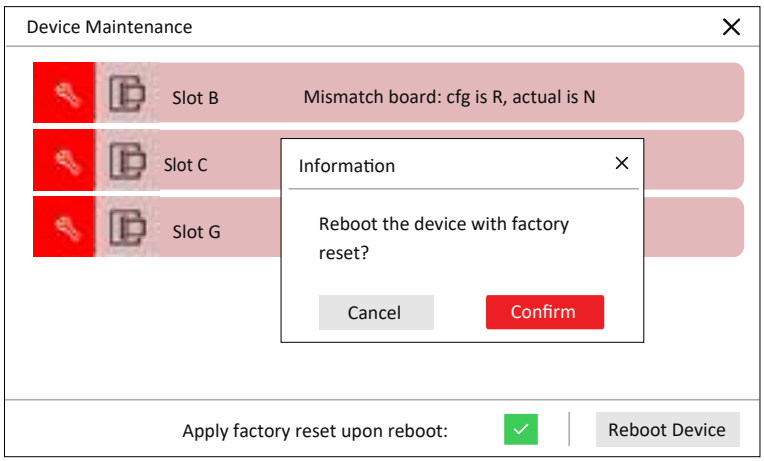
3. A pop-up window indicates the time remaining to reboot the IED. Manually reboot the IED or tap **Cancel** to cancel the factory reset operation.



NOTE: A 5-minute timer is started to permit to cancel the factory reset function. If timeout, the function is cancelled automatically and the IED remains the original mode; otherwise, the IED can be manually rebooted and enter **Default** mode.

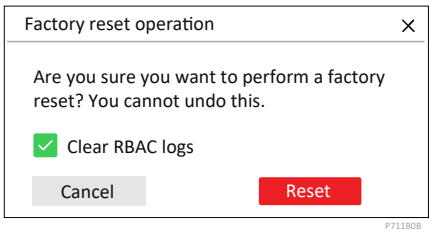
- **When in login status**

1. From **Login** page, tap  at the top right corner.
2. From **Device maintenance** page, select the checkbox **Apply factory reset upon reboot** and tap **Reboot device**.
3. From the pop-up window, tap **Confirm** to reboot the device or **Cancel** to cancel the operation.



- **When in Auto-login or login status**

1. From **Menu** page, expand ☰ **> General > System info**.
2. From the **Settings** tab, tap **Click to start** in the **Factory reset** field.
3. From the pop-up window, select or clear the checkbox **Clear RBAC logs** to reset or reserve the RBAC logs during the factory reset operation.
4. Tap **Reset** to enable the factory reset function within 1 minute or tap **Cancel** to cancel the factory reset operation.



NOTE: The passwords can be reset after the factory reset operation. The operation will result in loss of all device configuration and stored data, the device will reboot and operate the watchdog contact.

Preventive maintenance

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION, OR ARC FLASH

- Apply appropriate personal protective equipment (PPE) and follow safe electrical work practices.
- Do not use the arc fault system as a substitute for proper PPE when working on or near equipment being monitored by the system.
- Only qualified personnel can install and service this equipment. Read this entire set of instructions and check the technical characteristics of the device before performing such work.
- Perform wiring according to national standards (NEC) and any requirements specified by the customer.
- Observe any separately marked notes and warnings.
- NEVER work alone.
- Before performing visual inspections, tests, or maintenance on this equipment, disconnect all sources of electric power.
- Assume all circuits are live until they are completely de-energized, tested, and tagged.
- Pay particular attention to the design of the power system.
- Always use a properly rated voltage sensing relay to ensure that all power is off.
- Properly ground the equipment.
- Connect the device's protective ground to functional earth according to the connection diagrams presented in this document.
- Do not physically open the device.
- Install all components before powering this device.

Failure to follow these instructions will result in death or serious injury.

NOTE:

- See NFPA 70E, NOM-029-STPS-2011, or CSAZ462 for more information about safe electrical work practices.
- Consider all sources of power when turning off power supply, including the possibility of backfeeding.

⚠WARNING

UNINTENDED EQUIPMENT OPERATION

- Periodically perform system testing according to the testing recommendation in this manual.
- Perform system testing after changing the protection system scheme.

Failure to follow these instructions can result in death, serious injury, or equipment damage.

To obtain the maximum availability of the installation, it is essential to ensure that the PowerLogic P7 is operational at any time.

The PowerLogic P7's internal self-tests, the watchdog relay, and the LED alert the user in case of internal device failure. However, elements outside the PowerLogic P7 are not subject to the self-tests. Therefore, it is necessary to perform regular preventive maintenance.

Visually check the PowerLogic P7 and pay attention to dirty components, loose wire connections, damaged wiring, user interface screen and LEDs, and other mechanical connections.

Then, perform all the recommended commissioning tests. First test all the binary inputs and outputs involved in tripping the circuit breaker. A test of the complete chain including the circuit breaker is also recommended.

Recommended intervals

Test the PowerLogic P7 periodically according to the end user's safety instructions and national safety instructions or law.

The necessary time between visual inspections and functional checks depends on the installation operating conditions. Generally, we recommend to carry out periodic checks or tests every six (6) years. In corrosive or harsh offshore environments, functional testing should be carried out more often; we recommend every three (3) years.

For the testing procedures, see Commissioning, page 81.

The table below summarizes the recommended intervals.

Test	Recommended intervals
User interface check	1 year
Relay health check	6 years
Date and time synchronization check	6 years
Wiring and connections check	6 years
Analog inputs operation check	6 years
Binary inputs wiring and operation check	6 years
Binary outputs wiring and operation check	6 years

Preventive maintenance tasks

Checking device health

⚠CAUTION

UNINTENDED EQUIPMENT OPERATION

Periodically check the health condition of the device according to the site maintenance plan.

Failure to follow these instructions can result in injury or equipment damage.

- Check that the different currents and voltages measured by the PowerLogic P7 are appropriate for the load being powered.
- Check that the PowerLogic P7 🔧 LED is off and no maintenance message displayed on the front panel.
- Check the health of boards and modules. See Slot health, page 86 for more information.

Checking date and time synchronization

Check the status of main synchronization source and backup synchronization source from the HMI.

Checking the wiring and connection

⚠⚠DANGER

HAZARD OF ELECTRIC SHOCK, EXPLOSION OR ARC FLASH

Turn off all power supply to the equipment before working.

Failure to follow these instructions will result in death or serious injury.

- Check that the connections, including the ground terminal and the CT connections, are tight and free from corrosion.

  If the CT connections are not tightened properly, this generates excessive heat rise which can lead to the destruction of CT/VT analog input module connector and the CTs.
- Check the wiring connections in the rear panel: for the type of screws, screwdriver to be used, and torque (see Installation, page 34).

  In addition to the periodic wiring and connections check, a thermal measurement with thermal camera is recommended to make visible any warm points of the installation so that loose connections could be detected and corrected before a real issue occurs.
- Check the ground connection.

Checking analog input operation

Check current transformers (CTs), voltage transformers (VTs), and, if used, core balanced CTs connection. Check that measured analog values and angles are correct on the front panel.

Checking binary input wiring and operation

- Check that physical inputs states are correct, according to normal input configuration and wirings.
- Check binary inputs status from the HMI. See Slot health, page 86Binary inputs, page 85 for more information.

Checking binary output wiring and operation

- If accessible, check physical binary outputs position (continuity tester).
- Check binary outputs status from the HMI. See Binary outputs , page 86 for more information.

Checking the trip chain

Check regularly that the complete trip chain, from the CTs to the PowerLogic P7 and through to the trip coil, is always operational.

The complete protection chain is validated during the simulation of a fault that causes tripping of the switchgear by the PowerLogic P7. Simply testing one function can demonstrate that the whole system is working correctly, provided it has been installed correctly.

To validate the complete protection chain, proceed as follows:

1. Select one of the protection functions that trips the switchgear.
2. Depending on the function(s) selected, inject a current or a voltage corresponding to a fault and note whether the switchgear trips.

Troubleshooting

Troubleshooting the PowerLogic P7

If nothing happens when the PowerLogic P7 is switched on, troubleshoot the device according to Troubleshooting the PowerLogic P7 when no signs of energizing, page 466 below:

Table 410 - Troubleshooting the PowerLogic P7 when no signs of energizing

LED indication	Possible causes	Actions
All LEDs are off. Nothing is displayed on the screen.	PSU not fully inserted.	Fully insert the PSU.
	PSU inserted in wrong slot.	Put PSU in the correct position (slot Z).
	PSU polarity reversed on terminals.	Check that the + polarity is on terminal 4 and the - polarity is on terminal 2 for DC/AC power.
	PSU internal failure.	Contact Schneider Electric, replace new board.

If something happens when the PowerLogic P7 is switched on, it can be detected and reflected in the Data Object **SlotHlthX**. The error information is stored in the data object. For example, slot A occurred an error, the error is stored in **SlotHlthA. StVal**.

Table 411 - Troubleshooting the PowerLogic P7 with front panel indications

Front panel indications	Possible causes	Actions
Maintenance LED is in red. Device enters into maintenance mode. IED_2/LD0/FMON1.FWHlth1 stVal: 0 or 3[19]	Mismatch between hardware configuration and product model number.	Check the model number.
Maintenance LED is in red. IED_2/LD0/HMON1.SlotHlthX (A to Z) stVal: 0 or 3[19]	Hardware failure detected when the device is powered on. The message specifies the board impacted by the defect.	Check if the board is in the correct slot or the board is plugged in correctly.
Maintenance LED is in red. Device enters into maintenance mode. IED_2/LD0/FMON1.FWHlth1 stVal: 3[20]	Major issue on the CPU board of the device.	Check configuration and related version.
Maintenance LED is in red. IED_2/LD0/HMON1.SlotHlthX (B-C and D-E) stVal: 0 or 3[19]	Connection issue from CT/VT transformer to the device.	Check the connection from CT/VT to the analog input of the device. Switch off/on the device. If the failure is persistent, change the CT/VT board.
Maintenance LED is in red. Device enters into maintenance mode. IED_2/LD0/FMON1.FWHlth1 stVal: 0 or 3[19]	Incompatible firmware or hardware versions: • Application's version or name is incompatible. • Error for no version information.	Check the firmware or hardware version.
Maintenance LED is in red. Device enters into maintenance mode. IED_2/LD0/FMON1.FWHlth1 stVal: 0 or 3[19]	Device is in test mode/maintenance mode/ out of service.	Download configuration files.
Maintenance LED is in red. Device enters into maintenance mode. IED_2/LD0/FMON1.FWHlth1 stVal: 3[20]	The service of protocol was detected failure/ pending.	Check the configuration.
Maintenance LED is in red. IED_2/LD0/HMON1.SlotHlthX (D to G) stVal: 0 or 3[19]	MIO polarity reversed on terminals.	Check if the MIO module is correctly installed and wired. Refer to Wiring on the rear panel, page 53 for more details.
Sequence of event (Channel Status).	Hardware failure detected on the communication ports on CPU board when the device is powered on.	Check the connection of communication ports on CPU board.

19. 0: NonExist 3: Alarm
20. 3: Alarm

Table 411 - Troubleshooting the PowerLogic P7 with front panel indications (Continued)

Sequence of event (RTDFailX (1 to 8)).	The RTD number X on the MET148-2 board is disconnected or short circuited.	As the message is common to the RTD channels of the MET148-2 board, check **Measurement > Bay 1 > Thermal** to determine which RTD is affected by the defect. Measurement displayed: • MTmpX = -32768 °C RTD disconnected. T > 200 °C (392 °F) • MTmpX = 32768 °C RTD short circuited. T < -30 °C (-22 °F) Then check the connection of the RTDs.
Unable to log in.	CS certificate expired or CS configuration was potentially inconsistent.	Contact Schneider Electric Customer Care Center.
Message box prompts the user to log in.	The user did not log in with the EngineerLevel.	Use the EngineerLevel to log into the device.

Troubleshooting optional SFP modules

Issues	Possible Causes	Actions
Loose of communication during operation.	• Change of parameters. • Connection issue. • Hardware issue. • SFP is not suitable.	• For Ethernet board, check the traffic with the LEDs embedded on the RJ45 connectors. • Check all the information and parameters at SCADA level. • Check all the parameters at the device level. • Check all intermediate devices (switches, etc.) installed between SCADA and the device. • Check the connections. • Replace the SFP. • Use Schneider Electric approved SFP.

Troubleshooting the MET148-2 module

LED Indication	Possible Causes	Actions
The MET148-2 module green LED and red LED are both off.	Faulty wiring.	Verify that the RJ45 connector of the connection cord is correctly inserted into the socket.
The MET148-2 module red LED is off while the MET148-2 green LED is on.	No response from the MET148-2 module.	Check the position of the module number selection jumper: • MET1 for first MET148-2 module (temperatures T1 to T8). • If the jumper position needs to be changed, reboot the MET148-2 module (by unplugging and plugging the connection cord). • Change the MET148-2 module.
The MET148-2 module red LED is flashing irregularly.	Faulty wiring MET148-2 is powered but loss of dialogue with the base unit.	Check module connections: • Verify that the RJ45 connector of the connection cord is correctly inserted into the socket. • If the MET148-2 module is the last module in the daisy chain loop, check that the line terminating jumper is in the **Rc** position. In all other cases, verify that the jumper is in the position marked Rc.
	Connection issue	Unplug and plug the CAN cable on the EXT port of the PowerLogic P7 or the CAN cable on the EXT OUT port of the IRIG-B module (if used).
The MET148-2 module red LED is on.	More than two remote module are connected.	Remove extra remote module from the loop.
	The MET148-2 module internal failure.	Change the MET148-2 module.

Troubleshooting IRIG-B module

LED Indication	Possible causes	Actions
The device configured with IRIG-B synchronization source cannot be synchronized with IRIG-B source.	• The wire connection is loose. • Hardware issue.	• Check the traffic with the LEDs embedded on the IRIG-B connector. • Check the IRIG-B state from the HMI under ☰ > **General** > **System clock** > **Time source** > **Status** to check whether IRIG-B signal exists or not.

Troubleshooting CLIO module

LED Indication	Possible Causes	Actions
The CLIO module power LED is off.	Power failure	Reconnect the power supply for the CLIO module.
The CLIO module LINK LED is flashing irregularly.	Connection issue	1. Verify that the RJ45 connector of the connection cord is correctly inserted into the socket. 2. Unplug and plug the CAN cable on the EXT port of the PowerLogic P7 or the CAN cable on the EXT OUT port of the IRIG-B module (if used).

Troubleshooting serial ports

LED Indication	Possible Causes	Actions
The communication channel always cannot be built.	• The Rx/Tx wires are reversely connected. • Hardware issue	Check the wire connection.
Loose of communication during operation.	• The wires connection is loose. • Hardware issue.	• Check information and parameters at SCADA level. • Check the communication parameters, such as Baud Rate, Parity and Stop Bit.

Firmware update

The firmware update feature of the PowerLogic P7 provides the function to update the firmware of the device through the PowerLogic Engineering Suite.

Reasons for updating firmware:

- New functionality
- Security patches
- Correction of product behavior

Prerequisites

- The PowerLogic Engineering Suite is connected to the device to be updated.
  - Through the mini-USB port on the front panel.
  - Through one of the rear Ethernet ports.
  - The device is in offline status.

- You must have access to the zip file containing the firmware version you wish to update to.

  NOTE: This file typically has the format *P7.Vxx.xxx.xxx.zip*. Contact Schneider Electric Customer Care Center to get the package. Be aware that the contents of this file must come from Schneider Electric and the firmware signature will be checked to ensure that it has come from a genuine source before the product is updated.

Procedure for upgrading firmware

NOTICE
LOSS OF DATA • Save configuration files, disturbance records and events before upgrading the firmware. • Connect to the device and retrieve all configurations using the PowerLogic Engineering Suite after upgrading the firmware. • Rebuild the logics and matrix. **Failure to follow these instructions can result in permanent loss of data.**

To update the firmware of the PowerLogic P7:

1. Connect to the PowerLogic P7 using the PowerLogic Engineering Suite and log in with **EngineerLevel**.
2. From the application, click ⋮ on the device header bar and select **Update device firmware** from the drop-down.
3. Select the new firmware package from the folder where you saved the package.
4. From the **Connect to device** pop-up window, click **Connect**.

   The application will perform the following operations before starting the update:

   a. Check the user's rights.

   b. Check the available memory size.

   c. Copy the firmware to the device.

   d. Check the firmware and the hardware version compliance.

   NOTE: If every check is passed, the application gets ready to update the firmware and prompts the user to confirm.
5. From the **Authentication required** pop-up window, enter the username and password and click **Authenticate** to start the process of sending firmware files to device.
6. From the **Sending firmware files to device** pop-up window, click **Next** to start the process of updating firmware.

   After firmware update, the HMI on device will enter **Default mode** page indicating the firmware update is successful and the new firmware will take effect.

Replacing the modules

Identification of the modules

The PowerLogic P7 is a modular protection and control device. The modules fitted on all slots can be replaced individually.

To access the identification of the modules:

- From the HMI of the PowerLogic P7, expand ☰ **> General > Device config** to locate to the desired slot, navigate to **Version info** or **Slot info**.
- From the PowerLogic Engineering Suite, expand **Device configuration** to locate to the desired slot, navigate to **Basic info**.

NOTE: Slot A represents the CPU module.

Replacing the CPU module

⚠CAUTION

RISK OF SETTING CHANGES ERASED

- Never plug in or draw out the boards while the PowerLogic P7 is in service.
- Verify that the board is secured.

Failure to follow these instructions can result in injury or equipment damage.

To access the identification of the CPU module, see Identification of the modules, page 469 for more information.

Diagnosis for replacement

Check the following items on the device:

- The status of the watchdog relay on slot Z.
- The status of ON and LED indicators on the front panel.
- The status of ⓘ and LED indicators on the front panel.
- Tap LED to review the virtual configurable LEDs on HMI.
- Tap ALM to review the **Alarm list** page on HMI, if shown.
- Tap to review the **Device maintenance** page on HMI, if shown.

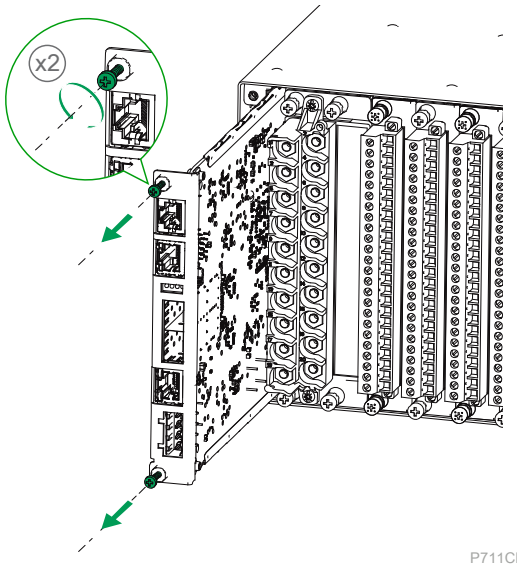
Preliminary operations

1. Power off the PowerLogic P7.
2. Check if there is enough space (> 35 cm or 13.78 in) to extract the module. If there is not enough space, remove the device from its mounting.
3. Check if the external signals are disconnected from the device.
4. Remove the wires, external modules, SFP modules and serial port terminal block connected to CPU module (see Changing a SFP module, page 474 for removing SFP modules).

Removal

1. Unscrew the retaining screws that fix the CPU module to the device.

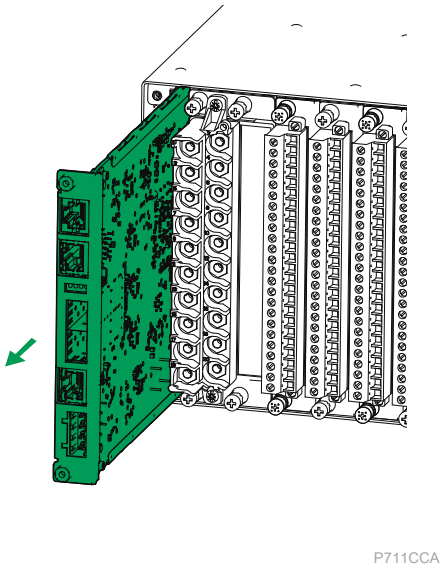
Figure 250 - Unscrew the CPU module retaining screws



Screws	Two screws on the top and bottom ends of the module
Tools	#2 Phillips screwdriver

2. Pull out the CPU module to detach it from the device with the help of the retaining screws.

Figure 251 - Removing the CPU module



Installation

1. Visually check the cleanliness and state of the place where the CPU module is to be installed before replacing the CPU module.
2. Insert the CPU module into the device case.

3. Tighten the screws to connect the CPU module to the device case.

Tools	#2 Phillips screwdriver
Tightening torque	0.6...0.8 N · m (5.31...7.08 lb-in)

Subsequent operations

After installing the CPU module, verify that it is operating correctly by completing the following steps:

1. Insert wires, external modules, SFP modules and serial port terminal block into location (see Changing a SFP module, page 474 for installing SFP modules).
2. Power on the PowerLogic P7.
3. Verify that the module is detected.
4. Verify that the ON LED is on, the LED is off, and the icon is not shown on the HMI.

Replacing other modules

⚠CAUTION

RISK OF SETTING CHANGES ERASED

- Never plug in or draw out the boards while the PowerLogic P7 is in service.
- Verify that the board is secured.

Failure to follow these instructions can result in injury or equipment damage.

NOTICE

EQUIPMENT DAMAGE DUE TO ELECTROSTATIC DISCHARGE (ESD)

Wear an ESD wrist strap to keep grounded before replacing the board.

Failure to follow these instructions can result in equipment damage.

To access the identification of the modules, see Identification of the modules, page 469 for more information.

Diagnosis for replacement

Check the following items on the device:

- The status of the watchdog relay on slot Z.
- The status of ON and LED indicators on the front panel.
- The status of and LED indicators on the front panel.
- Tap to review the virtual configurable LEDs on HMI.
- Tap to review the **Alarm list** page on HMI, if shown.
- Tap to review the **Device maintenance** page on HMI, if shown.

Preliminary operation

Before replacing a module:

1. Power off the PowerLogic P7.
2. Verify that there is enough space (> 35 cm or 13.78 in.) to extract the module. If there is not enough space, remove the device from its mounting.
3. Check if the external signals are disconnected from the device.

Removal

NOTE: If the PSU module is to be replaced, remove the ground lug prior to extraction of the PSU module. See Connecting ground, page 65 for details.

1. Unscrew the retaining screws that fix the terminal block (if fitted) to the device.

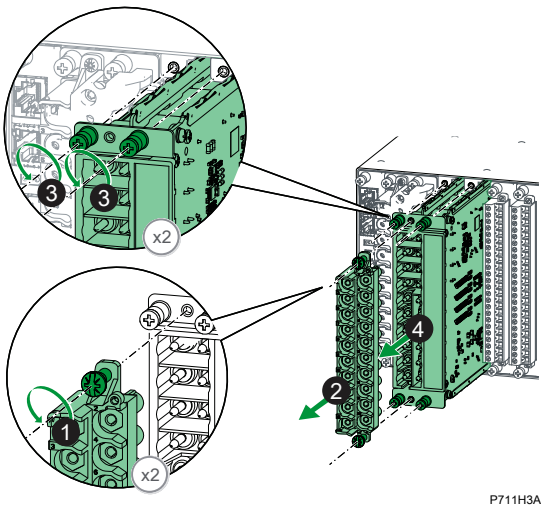
Screws	Two screws on the top and bottom ends of terminal block
Tools	• For CT/VT terminal block, (-) 6.5 mm (1/4 in.) or (+) PZ2 screwdriver • For other terminal blocks, (-) 3.5 mm (9/64 in.)

2. Pull out the terminal block (if fitted) to detach it from the module.
3. Unscrew the retaining screws that fix the module to the device.

Screws	Two screws on the top and bottom ends of the module
Tools	PH2 screwdriver

4. Pull out the module to detach it from the device with the help of the retaining screws.

Figure 252 - Removing the module



Installation

1. Visually check the cleanliness and state of the place where the module is to be installed before replacing the module.
2. Insert the module into the device case with the help of the guiding rails in the case.
3. Tighten the retaining screws to fix the module to the device case.

Tools	PH2 screwdriver
Tightening torque	0.6...0.8 N·m (5.31...7.08 lb-in)

4. Insert the terminal block into location.
5. Tighten the retaining screws to connect the terminal block to the module.

Tools	• For CT/VT terminal block, (-) 6.5 mm (1/4 in.) or (+) PZ2 screwdriver • For other terminal blocks, (-) 3.5 mm (9/64 in.)
Tightening torque	0.5...0.6 N·m (4.4...5.3 lb-in)

NOTE: After replacing the PSU module, connect the PowerLogic P7 device to the local ground bar using the M4 ground stud on the faceplate of PSU module. See Connecting ground, page 65 for details.

Subsequent operation

After installing the module, verify that it is operating correctly by completing the following steps:

1. Power on the PowerLogic P7.
2. Verify that the module is detected.
3. Verify that the ON LED is on, the LED is off, and the icon is not shown on the HMI.

Replacing a SFP module

⚠CAUTION

RISK OF SETTING CHANGES ERASED

- Never plug in or draw out the SFP modules while the PowerLogic P7 is in service.
- Verify that the SFP module is locked.

Failure to follow these instructions can result in injury or equipment damage.

The SFP modules can be replaced individually.

To access the identification of the module:

- From the HMI, expand ☰ **> General > Device config**.
- From the PowerLogic Engineering Suite, expand **Device configuration > Slot A**.

Preliminary operation

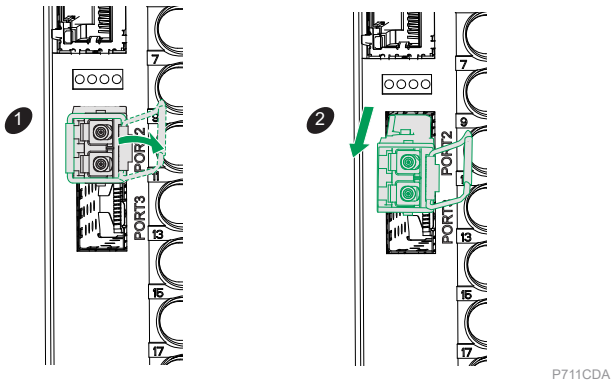
Before replacing a SFP module:

- Power off the PowerLogic P7.

Removal

1. Open the bale clasp locker.
2. Gently pull out the SFP module.

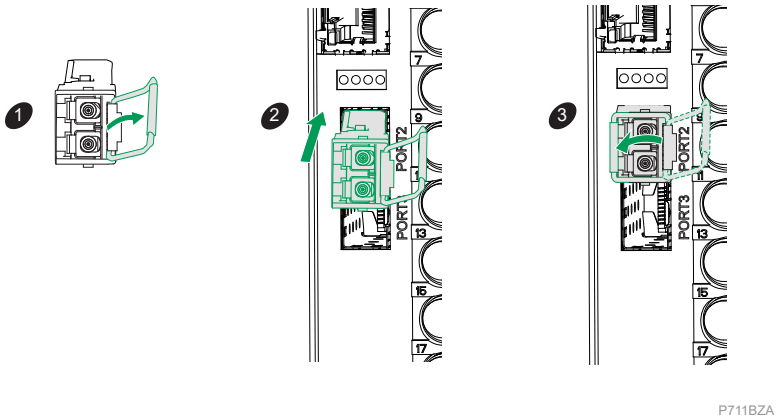
Figure 253 - Remove the SFP module



Installation

1. Open the bale clasp.
2. Insert the module into its location till the module locks itself in final place.
3. Lock the bale clasp. A click is heard when the locker is locked.

Figure 254 - Install the optional SFP module



Subsequent operation

After installing the module:

1. Visually check that the module is locked.
2. Power on the PowerLogic P7.
3. Verify that the module is detected:
   - From the HMI, expand ☰ **> General > Device config > Slot A** to check the module.
   - From the the PowerLogic Engineering Suite, expand **Device configuration > Slot A** to check the module.

Returning for expert assessment

To return the PowerLogic P7 for expert assessment, use the original packaging if possible.

PowerLogic P7 must be returned accompanied by its settings sheet and the following information:

- Name and address of the initiator
- PowerLogic P7 type and serial number
- Date of the incident
- Detailed description of the incident
- LED status and message displayed at the time of the incident
- List of stored events
- Repair and Modification Authorization (RMA) form which is from the country organization

End of life

At end of life of the PowerLogic P7, Schneider Electric's Green Premium program helps decrease the amount of waste and allow recovery of the product components and materials. Please refer to the Product Environmental Profile and the End of Life instructions documents available on SE website: https://www.se.com/ww/en/work/support/green-premium/.

Dispose the device according to the legislation of the country when decommissioning the device. It helps prevent potential disclosure of data contained in the device that was not removed.

NOTICE
UNAUTHORIZED OR UNINTENDED ACCESS TO CONFIDENTIAL DATA • Verify that all data from the device was saved and erased. • Perform a factory reset to recover the device's default configuration. **Failure to follow these instructions can result in permanent loss of data.**

Revision history

Document version	Description	
P7/EN M/02-002A 2024-09	Firmware version	V02.002
	Release/Build	V02.002.001
	Configuration tool	PowerLogic Engineering Suite V2.13.0
	Description of changes	Stand Alone Merging Unit (SAMU) application created.
		SV publishing/subscription on redundant (SFP) interface added.
		64 Fast Scheme Logic (FSL) pages added.
		Switch-onto-fault function added.
		Underfrequency load shedding function added.
		PHPDIF CT requirements reduced.
		PHRDIR and *EFRDIR* measured angle added.
		PTUF, *PTOF* frequency elements reset delay added.
		PTUF settable hysteresis added.
		TCTT/*TVTT*/*TCTS*/*TVTS* include *TCTR*/*TVTR* in the SCL files.
		1ph CT group changed from *TCTR* to *TCTS* and 1ph VT group changed from *TVTR* to *TVTS*.
		Language selection capability in the login view on HMI added.
		Block remote settings added.
		Fault locator function added.
		CPU memory increased for data storage with SOE to 10000 entries and the total storage space of DR to 300 MB.
		User maintenance record added.
		Test and Blocked inputs added in LLN0.
		Communication record added (3 PCAP files per interface).
		Modbus flexible communication mapping added.
		Network supervision added.
		IEC 61850 SCD roundtrip supported for SV configuration.
		Support for Cybersecurity SL2 added.
		PowerLogic P7 rack mounting option added.
		Current Loop Input/Output (CLIO) module added.
		Alignment of LED behaviors on PowerLogic P7 and SAMU added.
		1 Gbps Ethernet support on redundant (SFP) interface added.
		Current loop (mA) input function added.
		Programmable stage function added.
	Identified and fixed	Not possible to download logs when the PowerLogic P7 is in safe mode.
		System time sync - the timestamp in Linux side does not change after enable/disable local time flag on HMI panel.
		SOE sometimes cannot refresh.

Document version	Description	
		LTMS1.TmSyn status does not switch from GLOBAL to LOCAL.
		Equivalent heating current calculation are not as expected.
		TRxPDIF fault data incorrect.
		DMC board identification not correct with CTR and DIO.
		HMI time cannot be set when SNTP configured as backup time source.
		Size limitation of DR files for Modbus protocol.
		PHPTOC directional operation time delay is abnormal.
		Truck cannot be displayed on Mimic panel.
		The IED may enter safe mode when download complex SCD.
		Time synchronization still works via SNTP when SNTP status is set to Off.
		RSYN using pu values which did not work with 1ph VT group set with ph-ph values.
		TRxPDIF CT requirements incorrect.
		Current and voltage measurement accuracy claims improved to match device performance.
P7/EN M/22A 2024-01	Firmware version	V02.001
	Release/Build	V02.001.001
	Configuration tool	PowerLogic Engineering Suite V2.0.0
	Description of changes	Feeder application created.
		Transformer application created.
		Transformer differential added.
		Directional phase overcurrent added.
		Directional ground overcurrent added.
		Angle correction added to 1ph CT.
		Directional sensitive ground fault added.
		Ground admittance added.
		Frequency rate of change added.
		Recloser added.
		Restricted ground fault added.
		Positive sequence overvoltage added.
		Harmonics added.
		Voltage variation (Dips, Swells, Interruptions) added.
		Synchro-check added.
		Support of Direct Motor Control (DMC) module added.
		IP20 cover for CT/VT ring terminal block added.
		Thermal overload added.
		Flexible Modbus register mapping added.
		Overfluxing added.

Document version	Description	
		Machine unbalance added.
		Polarity added to CTs.
		Logging of local *RBAC* changes.
		Inter-turn overvoltage added.
		Start current and duration added for Motor monitoring.
		Equipment control enhanced (disable multiple control).
		Dynamic active indication added.
		Multiple mimics added.
		Widget color change added.
		Maintenance record added.
		Data object values display on mimic.
		Switchgear motor direct control.
		Centralized authentication added.
		Functional routing added.
		Three position switch added to mimic.
		Mimic SLD color added.
		Local bypass added.
	Identified and fixed	FSL and matrix not correctly managing inputs which are in test mode.
		Pulse control may not return to false automatically after switching setting group.
		GOOSE data from FSL not updated.
		ActSetGrp status may not change when setting group changes.
		The device not responding properly after a cancel request failed on *DOCtrl*.
		GOOSE cannot be sent out if configure *PTOC.str* or *Op* to GOOSE dataset.
		The device cannot receive normal GOOSE message after publisher stops sending GOOSE with wrong *numDatSetEntries*.
		OperatorLevel unable to connect PowerLogic Engineering Suite to device.
		VN calculation may not be correct when changing VT ratio in 3ph.
		HMI does not have timeout.
		FSL not following quality rules when GOOSE lost.
		Active group cannot be changed by PowerLogic Engineering Suite.
		Missing GOOSE subscriptions incorrect when device is set to Test.
		Quality of some Data Attribute (DA) in *SWXSWI* always be invalid.
		Measurement frequency value of *3phVT2* not correct.
		Motor Start Supervision not using FLA for Start current.
NA	Firmware version	V01.002
	Release/Build	V01.002.002

Document version	Description	
	Configuration tool	PowerLogic Engineering Suite V1.7.4
	Identified and fixed	The energized Binary Input (BI) status may be displayed as false after a device reboot.
		Time offset may not work after a reboot if the device is synchronized with SNTP.
P7/EN M/11B 2023-05	Firmware version	V01.002
	Release/Build	V01.002.001
	Configuration tool	PowerLogic Engineering Suite V1.7.4.
	Description of changes	Control inputs added.
		Function input inversion added.
		Function key size increased.
		Vector diagram added to vector page.
		French, Chinese and German language options added.
		Range Data Object (DO) added to measurements.
		Invalid measurements shown in gray.
		Range alarms added to measurements.
		Annunciator widget added to mimic.
		Measurement meter widget added to mimic.
		Menu navigation path added.
		FSL gate input and output inversion added.
		FSL latches added.
		STMP hysteresis reduced.
		TCS added.
		TCS input mode added to all binary inputs.
		Menu text improvements.
		Open and close pulse times extended.
		Default DNP3 analogue values changed to class 3.
		Peak to peak measurement mode added to *HIZPDIF*.
		CB supervision defaults changed.
		Stall defaults changed.
		AddCause reported for unsuccessful controls via HMI.
		RMS harmonic range improved.
		600 Hz storage rate added to disturbance records.
		Matrix reset added to demand measurements.
		Matrix and control reset added to motor restart inhibit.
		Close success added to CB supervision.
		ColOpn changed to indicate open success.
P7/EN M/11A 2022-10	Firmware version	V01.001
	Release/Build	V01.001.001

Document version	Description	
2023-02 reprint	Configuration tool	PowerLogic Engineering Suite V1.0.0
	Description of changes	First edition for initial product release.

Order information

When ordering, please state:

- Product code
- Quantity
- Accessories

PowerLogic P7 protection and control device	P7	M	4	0	-	1	C	R	5	R	6	N	M	N	N	N	N	N	N	N	N	N	-	T	M	B
Main Application																										
Motor		M																								
Generator		G																								
Feeder		F																								
Transformer		T																								
SAMU		S																								
Case Size																										
40TE			4																							
Application Level																										
Level 0 - Basic functions				0																						
Level 1 - Standard functions				1																						
HMI																										
Wall or flush mounting with status indication (SAMU only)						0																				
Flush mounting with 7" color touchscreen						1																				
Hardware Slot							A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P		Y	Z	
Optional boards are fitted in order R5/R6/N/M														Only available in 80TE case												
CPU with RJ45 + 2 SFP (see accessories) + EXT (see accessories)							C																			
Ring terminal 5 CT (1 core balance) + 4 VT (max 2 analog modules)								R	5	R	5	R	5	R	5	R	5	R	5	R	5					
Ring terminal 6 CT + 3 VT analog (max 2 analog modules)								R	6	R	6	R	6	R	6	R	6	R	6	R	6					
Direct motor control board with 7 BI + 2 DTNO + 2 Motor + HSHB								N	N	D	D	D	D	N	N	N	N	N	N	N	N	N				
Mixed card - 8 BI + 6 NO								M	M	M	M	M	M	M	M	M	M	M	M	M	M					
PSU auxiliary card - 8 BI (or 6 BI with speed) + 3 TCS + 3 NO																								T		
24...34 V DC supply + 2 DPCO + WD CO																									L	
48...125 V DC supply + 2 DPCO + WD CO																									M	
110...250 V DC/AC supply + 2 DPCO + WD CO																									H	
Firmware Compatibility																										
Revision A																										A
Revision B																										B

Accessories	
SFP accessories	
- Ethernet communication module RJ45 (max 100 m)	(REL70062)
- Ethernet communication module 100 Mbps multimode (max 2 km)	(REL70063)
- Ethernet communication module 100 Mbps singlemode (max 40 km)	(REL70064)
EXT accessories	
- IRIG-B modulated or demodulated module (max 10 m from the PowerLogic P7)	(REL51045)
- 8 RTD module (max 10 m from the PowerLogic P7)	(REL59641)
- CLIO module (max 10 m from the PowerLogic P7)	(REL70071)
- Frame for 19" rack mounting	(REL70076)
- Blankplate for slot (not installed)	(REL70179)
- 24-way pin terminal connector	(REL70181)
Ring terminal for auxiliary supply + 2 DPCO + WD CO[21]	

21. Contact your local Schneider Electric for availability.

Abbreviations

Table 412 - Abbreviations used in the manual

Acronyms	Indication
Ø	Diameter
AC, DC	Alternating Current, Direct Current
ACSI	Abstract Communication Service Interface
ANSI	American National Standards Institute
AI, AO	Analog Input, Analog Output[22]
ARC	Arc Sensor Input module with HSHB Binary Outputs
BayLD	Bay Logical Device
BI	Binary Input
BO	Binary Output[23]
CA	Certificate Authority
CAE	Cybersecurity Admin Expert
CAN	Controller Area Network
CB	Circuit Breaker
CCS	Close Circuit Supervision
CID	Configured IED Description
CLIO	Current Loop Input/Output
CPU	Central Processor Module
CT	Current Transformer
CTL	Isolator Motor Control Module
CTS	Current Transformer Supervision
DIN rail	Deutsches Institut für Normung rail[24]
DMS	Distribution Management System
DPCO	Double Pole ChangeOver contact
DT	Definite Time
DNP3	Distributed Network Protocol 3
DPWS	Device Profile for Web Services
DO	Data Object
DA	Data Attribute
EMC	Electro Magnetic Compatibility
EMF	Electro Motive Force
ETH	Ethernet Module
FCD	Functional Constrained Data
FCDA	Functional Constrained Data Attribute
FIB	Fiber Interface Module for Serial and/or Current differential
FO	Fiber Optics
FSL	Fast Scheme Logic
GOOSE	Generic Object Oriented Substation Events[25]
HMI	Human Machine Interface

22. Refer to current loop (4...20 mA) signals used to represent analog values.
23. Used in connection with the number of inputs and output contacts within the device and with the slot letter.
24. Standard metal rail used to mount equipment inside electrical cabinet.
25. in IEC 61850, type of generic substation event, for a peer-to-peer communication over Ethernet.

Table 412 - Abbreviations used in the manual (Continued)

Acronyms	Indication
HSR	High availability Seamless Redundancy
HTTP	Hyper Text Transfer Protocol
ICD	IED Capability Description
IDMT	Inverse Definite Minimum Time
IEC	International Electrotechnical Commission[26]
IED	Intelligent Electronic Device
I/O	Input/Output[27]
INP	Digital Input Module
IRIG-B	Inter-Range Instrumentation Group time code B[28]
IP	Internet Protocol
JTAG	Joint Test Action Group
LAN	Local Area Network
LC	Lucent Connector[29]
LD	Logical Device
LDAP	Lightweight Directory Access Protocol
LPAI	System (L) Physical Analog Input
LPDI	System (L) Physical Digital Input
LPDO	System (L) Physical Digital Output
LED	Light Emitting Diode
LV, MV, HV	Low Voltage, Medium Voltage, High Voltage
L/R	Local/Remote
MCB	Miniature Circuit Breaker
MIO	Mixed binary Input/Output module
Max.	Maximum
NERC	North American Electric Reliability Corporation
OUT	Binary Output Module
OTP	One Time Password
PCT	Protective Conductor Terminal ground
PLC	Programmable Logic Controller
PRP	Parallel Redundancy Protocol
PSL	Programmable Scheme Logic
PSU	Power Supply Unit[30]
PTP	Precision Time Protocol[31]
QR code	Quick Response code[32]
RADIUS	Remote Authentication Dial In User Service
RBAC	Role Based Access Control[33]
RCA	Relay Characteristic Angle

26. Prepares and publishes international standards for electrical and electronics technology.
27. Used in connection with the number of inputs and output contacts within the device (e.g. 8I6O: 8 inputs, 6 outputs).
28. Standard for time transfer.
29. Type of optical connector.
30. Power Supply Module with Binary Outputs.
31. IEEE 1588
32. Two-dimensional barcode.
33. Provides a restricted access to authorized users only (Cybersecurity).

Table 412 - Abbreviations used in the manual (Continued)

Acronyms	Indication
RH	Relative Humidity
RJ45	Registered Jack 45[34]
RMS	Root Mean Square
EIA-485 (RS485)	Electronic Industry Association-485[35]
RSTP	Rapid Spanning Tree Protocol[36]
RTC	Real Time Clock
RTD	Resistance Temperature Detector
RTU	Remote Terminal Unit
RMA	Repair and Modification Authorization
SAM	Security Administration Manager
SCADA	Supervisory Control And Data Acquisition
SCD	System (Substation) Configuration Description
SFP	Small Form-factor Pluggable communication modules
SFTP/FTP	Secured File Transfer Protocol/File Transfer Protocol
SOL	Selective Overcurrent Logic
ST (BFOC)	Straight Tip (Bayonet Fiber Optic Connector)[37]
STB	Smart Switchgear and Terminal Block Module
THD	Total Harmonic Distortion
TIO	Auxiliary power supply module
TCS	Trip Circuit Supervision[38]
SNTP	Simple Network Time Protocol
USB	Universal Serial Bus
UDP	User Datagram Protocol
VLAN	Virtual Local Area Network
VT	Voltage Transformer
VTS	Voltage Transformer Supervision
WD	Watch Dog
ω	Motor rotation speed
ω_{NOM}	Rated motor rotation speed

34. Standardized type of connector (eight-wire connector) used for Ethernet networking.
35. Standard defining the electrical characteristics of a robust serial communication interface using differential signals for the transmission.
36. Redundancy communication protocol.
37. Type of optical connector.
38. NO contact with BI.

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